# A New Isolated DC-DC Converter Based-on MMC for High Voltage Applications

**Tuan-Vu Le, Ji-Hoon Yang, Seong-Mi Park, Sung-Jun Park**

***Abstract Background/Objectives:*** ***In recent years, the demand for power converters in high voltage applications such as wind power, electric locomotive, BESS, HVDC has been increasing rapidly. However, there is a big challenge in high voltage application is from the limited ability of power electronics. Hundreds of studies have been conducting in order to figure out solutions which are able to increase working voltage of new semiconductor power switching devices.***

***Methods/Statistical analysis:*** ***This paper proposes an effective circuit configuration of isolated DC-DC converter for medium voltage applications. Since the operating voltage range of the switching devices is limited, few researches of DC-DC configuration operating at high voltage are conducted. This is the main motivation for us to research the configuration of DC-DC converter operating at high voltage. The proposed configuration in this paper is divided two parts, the high voltage side is made up of serial modular multilevel converter (MMC), the other one is low voltage which is rectifier diode bridge, and both are linked by a high frequency transformer.***

***Findings:*** ***A new configuration of DC-DC converter for high voltage applications is mentioned in this research. It is divided into two parts, the high voltage part is the MMCs while the low one is the H-bridge rectifier, and the high frequency transformer links these two parts. The output of the proposed converter independent on both ratio of transformer and switching algorithm. The configuration of the circuit, along with pulse-width-modulation (PWM) will be presented and verified by simulation and experimental results that can possibly prove practicality of the new topology.***

***Improvements/Applications:*** ***The suggested converter is suitable for high voltage application with a high step ratio and isolation characteristics between source and load. A PWM based-on phase-shifted algorithm is presented to control the output voltage. Cell-rotated selection is applied to achieve a self-balanced capacitor voltage levels.***

***Keywords: Modular multilevel converter (MMC), DC/DC converter, High voltage, BESS, HVDC***

## I. INTRODUCTION

In recent years, the demand for power converters in high voltage applications such as wind power, electric locomotive, BESS, HVDC has been increasing rapidly [1-5]. However, there is a big challenge in high voltage application is from the limited ability of power electronics. Hundreds of studies have been conducting in order to figure out solutions which are able to increase working voltage of new semiconductor power switching devices. On the other hand, multilevel configuration is found to be effective to enhance the rated voltage with the existing power switches [6]. Modular structures [8-10] are shown by the conventional multilevel converters such as flying capacitor, diode-clamped [7], or cascade H-bridge. Nowadays, multilevel configuration for DC-DC converter is the trend in high voltage application fields. That kind of converter is probably used for either step-up or step-down, however the higher the step ratio is, the larger size the topology causes.

A new configuration of DC-DC converter for high voltage applications is mentioned in this research. It is divided into two parts, the high voltage part is the MMCs while the low one is the H-bridge rectifier, and the high frequency transformer links these two parts. The proposed converter is suitable for high voltage application with a high step ratio and isolation characteristics between source and load. A PWM based-on phase-shifted algorithm is presented to control the output voltage. Cell-rotated selection is applied to achieve a self-balanced capacitor voltage levels. The configuration of the circuit, along with pulse-width-modulation (PWM) will be presented and verified by simulation and experimental results that can possibly prove practicality of the new topology.

## II. MATERIALS AND METHODS

### 2.1 Fundamental MMC Cell

Fig. 1(a) presents fundamental MMC cell which the switching devices in each cell are determined by a switching function G that has 2cases,

$$G = \begin{cases} 1 \\ 0 \end{cases} \quad (1)$$

In case G = 1, $S_{up}$ is close but $S_{down}$ is open. On the contrary, when G = 0, $S_{up}$ is open but $S_{down}$ is close. Assuming that the voltage on capacitor C is constant and equals $V_C$, the output voltage results:

$$V_{PN} = GV_C \quad (2)$$

There are 2 voltage levels of fundamental cell formed by G. Level 0 (cell OFF) specifies a 0V output voltage while level 1 (cell ON) specifies an output voltage equal to $V_C$. Fig. 1(b) shows a switching

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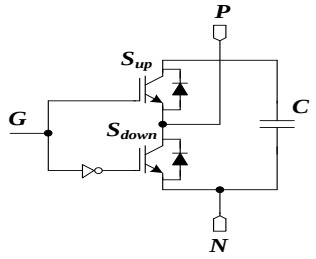
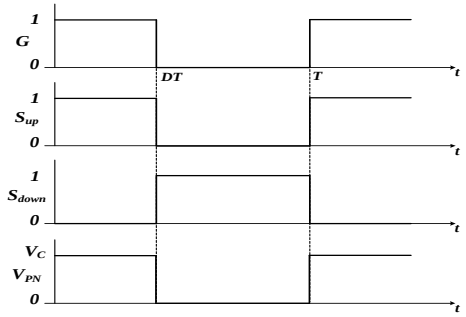
pattern of the cell, along with corresponding output voltage.




**(a) Topology**




**(b) Switching pattern**

**Figure 1. Fundamental MMC and switching pattern**

### 2.2. Configuration of Proposed DC-DC Converter

The configuration of suggested converter is shown in Fig.2. For the high voltage side, it has N cells MMC in the upper group (C_U1, C_U2,…, C_UN) and N cells MMC in the lower group (C_D1, C_D2,…, C_DN) and both have series connection. All elements in the circuit are supposed to be ideal and its operation is in steady state. The voltage across the capacitors is the same. At A-linking point of upper group and lower group, we can generate larger voltage levels, smaller voltage levels or equal to the voltage level at B-neutral point of the source. Therefore, the voltage between A and B can be negative, positive or zero voltage.

The instantaneous voltage on the cell is slightly different from the voltage across $C_{up}$, $C_{down}$. Therefore, small inductors $L_{up}$, $L_{down}$ are needed to decrease circulating current. The low voltage part is composed of the H-bridge rectifier and a low pass filter Lf, Cf would normally be present at the output of the converter. In addition, a high frequency transformer is used not only to transfer energy between the high and low side but also isolate the two sides. In general, the operation of the proposed converter is similar to an isolated DC-DC converter. In which, the high voltage side with a series of MMCs represent the half-bridge configuration, while the low one is the H-bridge rectifier. Control methods of the proposed topology are the same and based on phase-shift PWM mechanism. But inside the MMCs, with special the PWM algorithm not only to ensure the phase-shift PWM mechanism but also to stabilize the capacitor voltage balancing of MMCs. These PWM algorithms will be presented in the sections below.

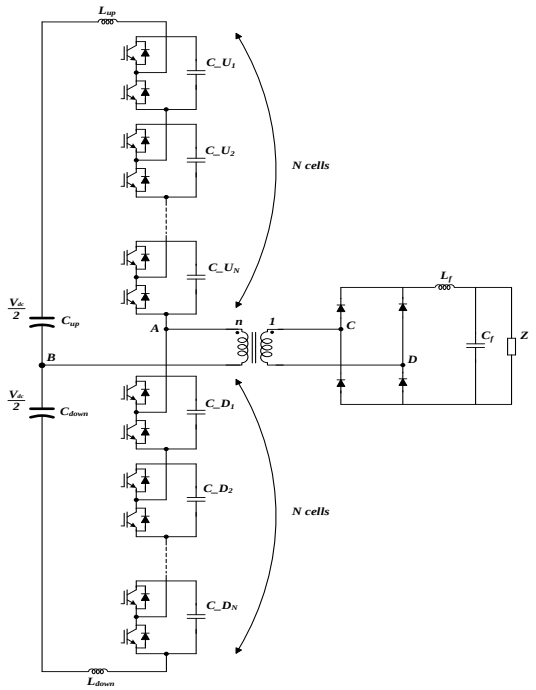



**Figure 2. Topology of proposed converter**

### 2.3. Switching Pattern for Proposed Topology

The MMC cell numbers of upper group and lower group are in the form 2k where k is the natural number and greater than 1.

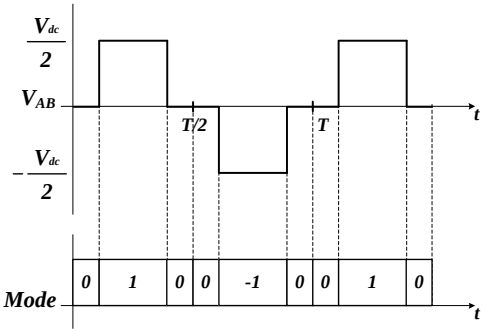
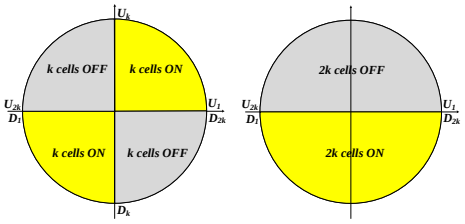



**Figure 3. Input waveform of primary windings and corresponding modes of even topology.**

To facilitate this, Fig.3 shows each switching mode for producing three levels, and the detailed circular diagrams in Fig. 4 explains how the modes work following




**(a) Mode 0** **(b) Mode 1**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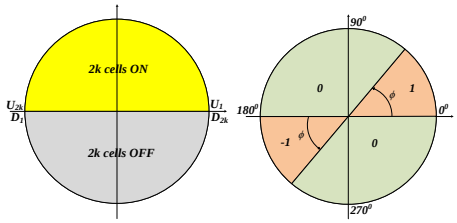



**(c) Mode -1** **(d) Phase-shift control**

**Figure 4. Operational modes in one cycle of the proposed topology**

Each operating mode ensures that 2k cells are turned on. All elements in the circuit are supposed to be ideal and its operation is in steady state, every capacitor voltage equals $V_{dc}/2k$. Note that the voltage at point B is $V_{dc}/2$, so by changing the voltage at point A we can obtain three level voltages in the input primary voltage wave corresponding to three operational modes in one cycle.

Mode 0: Fig. 4(a) shows the ratio of cell ON, cell OFF of the two groups upper and lower. The upper group has k cell ON and k cell OFF, same for lower group. Therefore, the voltage at point A is equal to half the voltage of the source, $V_{dc}/2$, lead to 0V level in the input primary voltage.

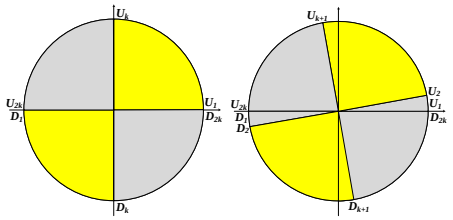
Mode 1: Fig. 4(b) shows that all cell of the upper group are turned OFF and all cell of the lower group are turned ON. Thus, the voltage at point A is $V_{dc}$ and then we have $V_{dc}/2$ level in the input primary voltage.

Mode -1: in Fig. 4(c), all cell of the upper group are turned ON and all cell of the lower are turned OFF. Therefore, the voltage at point A is 0 and then we obtain $-V_{dc}/2$ level in the input primary voltage.

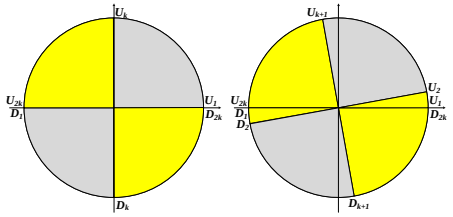
The voltage applied to the primary windings of the transformer must be equal to the positive and negative symmetry. This means that the period time of mode 1 and mode -1 are equal. Therefore, the output voltage of the converter is determined by the ratio of modes 1,-1 compared to mode 0 in one cycle. Fig. 4(d) shows that variable controls the output voltage of the proposed converter:

$$\overline{|V_{AB}|} = \frac{\phi}{360} V_H \qquad (3)$$

whereas n is the ratio of transformer and .




**(a) T1** **(b) T2**




$$v_{ref1}(t) = \left(1 - \frac{\phi}{360}\right)\left[d(t) - d(t-2T)\right] + \frac{\phi}{360}\left[d(t-2T) - d(t-4T)\right] \qquad (4)$$

**(c) $T_k$** **(d) $T_{k+1}$**

**Figure 5. Cell-rotated selection of the proposed topology**

In mode 0, each upper and lower group has k cells ON. Choosing k cells randomly without any rule will lead to the timing of the capacitors charging and discharging unequally, thus causing an imbalance in the voltage across the capacitors. To avoid this, it is necessary to have an algorithm that controls how much charge and discharge are on the same capacitors. In this paper, the cell-rotated selection algorithm is applied, as shown in Fig.5. Details of the algorithm are that, in the first cycle, k cells from $U_1$ to $U_k$ in upper group are turned ON, and same for $D_1$ to $D_k$ in lower group as shown in Fig. 5(a). In the 2nd cycle, shown in Fig. 5(b), k cells ON in upper group are $U_2$ to $U_{k+1}$, and k cells ON in lower group are $D_2$ to $D_{k+1}$. And the same for the $k^{th}$ cycle, shown in Fig. 5(c), $U_k$ to $U_{2k}$ in upper group are selected for turning ON, $D_k$ to $D_{2k}$ in lower group are choose for turning ON. Fig. 5(d) shows for the next cycle. The algorithm goes on and goes back to its origin state in the cycle of $(2k+1)^{th}$.

To illustrate this control algorithm, Fig. 6 shows the switching pattern of the proposed topology with N equal to 4. It uses a carrier ($v_{car}$) and four reference waves $v_{ref1}$~$v_{ref4}$. Every reference wave is compared to the carrier, then it generates switching signals ($U_n$ and $D_n$).

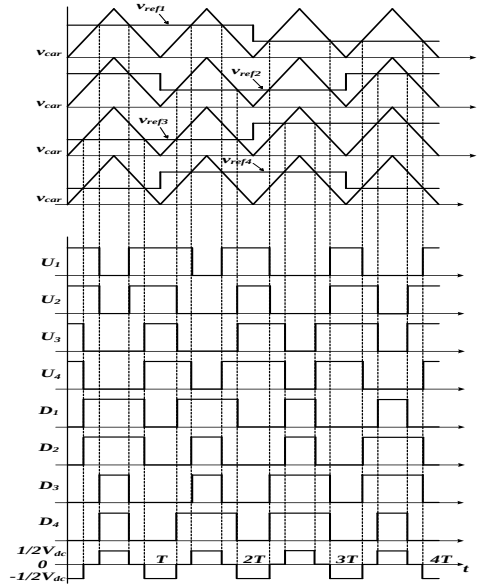



**Figure 6. Switching pattern of the proposed topology when the cell of upper/lower group are 4**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$$v_{ref\,2}(t)=\left(1-\frac{\phi}{360}\right)\left[d(t)-d(t-T)+d(t-3T)-d(t-4T)\right]+\frac{\phi}{360}\left[d(t-T)-d(t-3T)\right] \quad (5)$$

$$v_{ref\,3}(t)=\left(1-\frac{\phi}{360}\right)\left[d(t-T)-d(t-2T)\right]+\frac{\phi}{360}\left[d(t)-d(t-2T)\right] \quad (6)$$

$$v_{ref\,4}(t)=\left(1-\frac{\phi}{360}\right)\left[d(t-T)-d(t-3T)\right]+\frac{\phi}{360}\left[d(t)-d(t-T)+d(t-3T)-d(t-4T)\right] \quad (7)$$

$$d(t)=\begin{cases}1 & t\geq 0\\ 0 & t<0\end{cases} \quad (8)$$

## III. SIMULATION AND EXPERIMENTAL RESULTS

### 3.1. Simulation results

Validity of the proposed converter is verified by using PSIM simulation. The input DC voltage is ready at 10kV, the number of cells in each group is 4. Hence, each capacitor voltage is divided into 2.5kV. The transformer ratio is set to 5:1. The switching frequency is set to10kHz. The inductors $L_{up}$ and $L_{down}$ are set to 10uH, the Lf Cf low-pass filter are set to 2mH and 680uF, respectively. The capacitors of cells are set to different value to verify the PWM algorithm:

$$C_{U1}=125uF, C_{U2}=100uF, C_{U3}=150uF, C_{U4}=150uF$$

$$C_{D1}=100uF, C_{D2}=120uF, C_{D3}=100uF, C_{D4}=130uF$$

Simulation result of the capacitor voltage is given in Fig.7. From top to bottom: Vp is primary voltage, VM_U1, VM_U2, VM_U3, VM_U4 are the capacitor voltages in upper group, VM_D1, VM_D2, VM_D3, VM_D4 are the capacitor voltages in upper group. The capacitor voltages are balance which the value is at 2.5kV.

Through Fig. 8, the simulation result of voltage and current waveforms can be seen. From top to bottom: Vp is primary voltage, Vs is secondary voltage, It is primary current and Vo is output voltage.

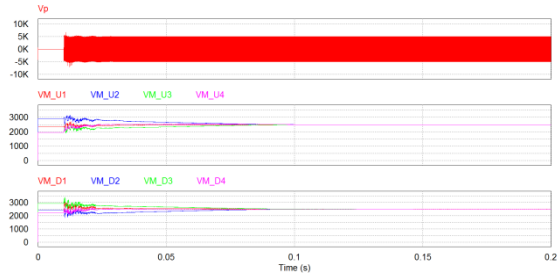


**Figure 7. Simulation results of capacitor voltage waveforms of cells**

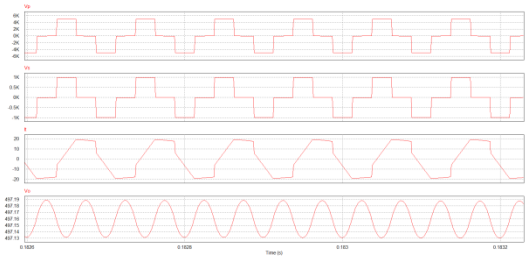

**Figure 8. Simulation results of voltage and current waveforms**

### 3.2.Experimental results

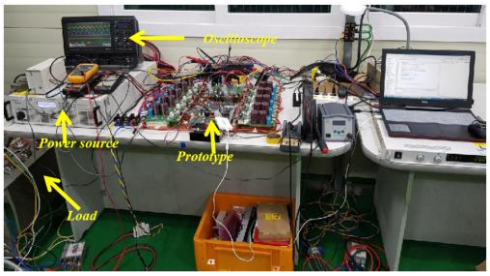


**Figure 9. Experiment setting table**

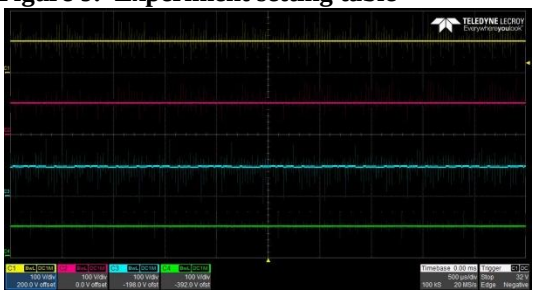

**Figure 10. Experimental results of capacitor voltage waveforms of cells in upper group**

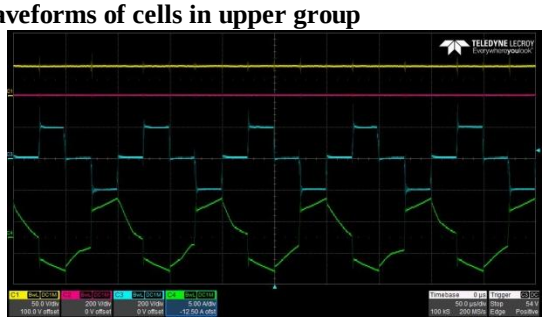

**Figure 11. Experimental results of voltage and current waveforms**

Fig. 9 presents the experiment setting table. The load is set to 5ohm, input voltage set to 400V, and the turn ratio of transformer is set to 2:1. The values of capacitor of cells are set to:

$$C_{U1}=100uF, C_{U2}=136uF, C_{U3}=168uF, C_{U4}=68uF$$

$$C_{D1}=100uF, C_{D2}=100uF, C_{D3}=136uF, C_{D4}=168uF$$

Fig. 10 shows the experimental result of capacitor voltages. From top to bottom are the capacitor voltages of cell U1, U2, U3, and U4 which have the value at 100V.

Fig. 11 figures out the experimental result of voltage as well as current waveforms. From top to bottom: Channel 1 is the output voltage, channel 2 is the

input voltage, channel 3 is the primary voltage and channel 4 is the primary current of transformer.

## IV. CONCLUSION

We proposed a DC-DC converter that can effectively operate at high voltage. After theoretical analysis, we simulated and experimented to verify the validity of the proposed approach. Below are advantages of the proposed converter:

- Solving the problem of limiting the voltage capability of semiconductor switching devices
- The proposed topologies are based on the series-connection of sub module, which each contain both of the core components of any voltage source converter. Therefore, they can be connected into strings to handle higher voltage
- The proposed PWM cell-rotated selection control algorithm can solve capacitor voltages balance problem without voltage sensors on sub-modules

## ACKNOWLEDGMENT

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