

Design of the High-speed Error-Trapping Decoder for the (693, 676) Fire Code

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Abstract: In this paper, we design the decoder of (693, 676) Fire code for correcting burst-error which often occurs in wireless communication and storage system.

Methods/Statistical analysis: The code length is determined by the generator polynomial which is based on the irreducible polynomial over Galois Field. Two shift registers for trapping error is included in an alternate (693, 676) Fire code decoding circuit, the error-tracking register and the error-pattern register based on the irreducible polynomial. The syndromes are calculated in the shift registers using irreducible polynomials, respectively.

Findings: The prerequisites for code design are described first, and the Fire code for simple single burst error correction is mentioned. The high speed error trapping technique is suggested in the decoding system, and the operation of error pattern register and error tracking register is stated.

Improvements/Applications: The speed and simplicity cannot be achieved at the same time, some trade-off must be made. The syndrome calculation can be achieved in the designed decoder by the simple cyclic shifts.

Index Terms: Fire code, Burst error correction, Error trapping decoder, Error tracking technique, irreducible polynomial.

I. INTRODUCTION

In certain digital communications or computer storage systems, we can observe that errors occur in the form of shorter or longer bursts[1]. This same kind of phenomenon occurs as a result of telephone line surges, intentional jamming of spread-spectrum systems, and fading effects in microwave and radio links[2].

In a burst-error environment, selecting the code that has the interleaving technique for correcting random error is often desirable[3][4]. An interleaver is a system that can reorder sequences of digits by interleaving members of two other sequences in alternation. A deinterleaver is a device that, through inverse rearrangement of received words, reestablishes the received data stream to its initial sequence. Because of this, this way affects mixing the coded stream of data before transmission, followed by unscrambling the sequence after reception in order to spread the consecutive error pattern process. Pseudorandom and periodic characteristics are the both estate of interleaving technique.

Cyclic codes, especially Fire codes, is usually adopted to amend long error sequences and has an ability to decode by

using the error-trapping technique. A number of collective and consecutive errors can be noticed by Reed-Solomon decoding technique which mixes and spreads digits to correct multiple long bursts. Threshold decoding of burst-error-correcting convolutional codes allows long bursts to be corrected through the use of guard space[5][6]. Another type of error-burst problem occurs in Gaussian noise channels that has contaminated noise signals due to interference and results many burst errors, which may happen in intended disturbing channel circumstances. A related problem is coding for spread-spectrum systems[7][8].

II. BURST ERROR CORRECTION FOR BLOCK CODES

A. Prerequisite Consideration

The best correcting techniques for consecutive errors have been searched by computer, which is dissimilar with comparing the codes for correcting scattered errors[9][10]. Nevertheless, before discussing these codes for correcting consecutive errors, it is worthwhile to consider the following theorems. Ordinarily, if b is the consecutive error length, it means the nonzero components in the code sequences that is in successive bits. The first bit and the last bit are nonzero.

Some facts described below must be considered before the design of Fire code.

- An (n, k) linear block code that has no burst of length b or less as a code word must have at least b parity-check bits.
- If we consider the code with the ability to correct the consecutive errors that has a length b , then there is not the consecutive errors which is less than $2b$ as a code word.
- The number of parity-check digits in any linear (n, k) block code that corrects all bursts of length b or less is bounded by the following inequality:

$$n - k \geq b - 1 + \log_2(n - b + 2) \quad (1)$$

B. Single-Burst Correction by Fire Codes

The first class of cyclic codes, which is constructed systematically for correcting a single burst of errors, is the Fire codes. Fire codes can be decoded by the error-trapping technique. It has been shown that a primitive polynomial $p(x)$ of degree m is a factor of $x^e + 1$, where $e = 2^m - 1$. This positive integer e is called the

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period of $p(x)$ because e is the order of the root α of $p(x)$ because $\alpha^e = \alpha^{2^m-1}$. Consider an $(n, n-2b-m+1)$ Fire code that is generated by $g(x) = p(x)(x^{2b-1} + 1)$ and that can correct any consecutive errors with the length less than b . Here $b \leq m$, and $2b - 1$ cannot be divided by e . The code length n can be calculated by the LCM of $2b - 1$ and e , such that $n = LCM(e, 2b - 1)$.

C. High-Speed Error-Trapping Decoder

Consider a Fire code over GF(2) that can be produced by the polynomial equation below:

$$(2) \quad \begin{aligned} g(x) &= (1 + x + x^6)(1 + x^{11}) \\ &= 1 + x + x^6 + x^{11} + x^{12} + x^{17} \end{aligned}$$

This code is of length $n = LCM(63, 11) = 693$ and can correct any consecutive error with length b less than 6. A conventional decoder for this Fire code consists of a 17-stage syndrome register with $n - k = 17$ digits, which is the degree of $g(x)$, a 693-bit buffer register, and some logics for decision and connections for the feedback, and is similar to the decoders. This conventional decoders are fitted to the systems that have no need of considering speed problem. However, the computing speed is an important consideration in designing the suitable code for digital systems, any meaningful time delay may not be allowed to decode the received code word. Therefore, the object of this section is to investigate a method for fast decoding of codes for correcting consecutive errors. Designing the decoders for correcting consecutive errors are usually performed by detecting the error pattern and cyclic shifting. In view of the fast decoding required, devising the new decoding algorithms is advisable and it can achieve the procedure for decoding at the higher speed with some aids of calculation.

A fast error-trapping decoder for a class of Fire codes is a (693, 676) Fire code with the generator polynomial $g(x) = (1 + x + x^6)(1 + x^{11})$. Two shift registers for trapping error is needed for composing an alternate (693, 676) Fire code decoding circuit, one is the error-pattern register founded by the element $1 + x^{11}$ and the other is the error-tracking register founded by the element $p(x) = 1 + x + x^6$. However, if no computation facility is provided for this alternate decoder, its speed will be the same as the conventional decoder in the typical Fire codes. Both registers operates in synchrony for detecting errors and computing syndrome. An alternate circuit for fast computation for a (693, 676) Fire code decoding is shown in Figure 1. Test for zero circuit is composed of OR gate. $r(x)$ is the received polynomial and the syndromes are the remainders that result from dividing $r(x)$ by the factors of $g(x)$, i.e., $1 + x + x^6$ and $1 + x^{11}$ respectively. The error pattern is identified when the contents of both registers are exactly the same. If an consecutive error with length b less than 6 has appeared, the pattern of errors can be expressed as $e(x) = x^i B(x)$. If an error burst of length $b \leq 6$ has occurred, then the error pattern can be expressed as $e(x) = x^i B(x)$. In order for the error pattern to shift out

from the buffer register, it must be cyclically shifted $(n - 1) - (i + 5) = n - i - 6$ times. The syndromes calculated in the shift registers for the factors $1 + x + x^6$ and $1 + x^{11}$ are, respectively,

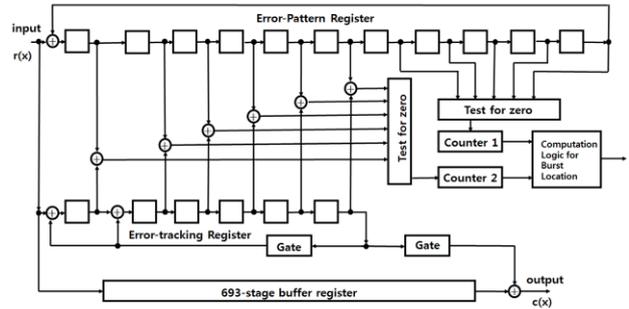


Figure 1. High-speed error-trapping decoder for the (693, 676) Fire code

$$\begin{aligned} x^{i+6}B(x) &= q_1(x)(1 + x^{11}) + s_c(x) \\ x^{i+6}B(x) &= q_2(x)(1 + x + x^6) + s_p(x) \end{aligned} \quad (3)$$

After $n - i - 6$ cyclic shifts, $e(x)$ becomes

$$e^{(n-i-6)}(x) = x^{i+6}B(x)x^{n-i-6} = B(x) \text{ modulo } (x^n + 1) \quad (4)$$

Thus, each register contains the below

$$\begin{aligned} B(x) &= q_1(x)(1 + x^{11}) + s_c^{(n-i-6)}(x) \\ B(x) &= s_c^{(n-i-6)}(x) \text{ modulo } (x^{11} + 1) \end{aligned} \quad (5)$$

or

$$\begin{aligned} B(x) &= q_2(x)(1 + x + x^6) + s_p^{(n-i-6)}(x) \\ B(x) &= s_p^{(n-i-6)}(x) \text{ modulo } (x^6 + x + 1) \end{aligned} \quad (6)$$

from which we obtain

$$s_c^{(n-i-6)}(x) = s_p^{(n-i-6)}(x) = B(x) \quad (7)$$

If the relationship between the error and the syndrome is described in this format, it means that the burst-pattern $B(x)$ is trapped in the b low-order stages of the error-pattern register and that the $b-1$ high-order stages of the error-pattern register contain all 0s by the time the register has been shifted $n - i - 6$ times. Thus we see that the contents in the error-tracking register lock the burst pattern $B(x)$ in the b low-order positions of the error-pattern register.

III. IMPLEMENTATION OF FIRE DECODER

The fast error-trapping decoder for a (693, 676) Fire code with $g(x) = (1 + x + x^6)(1 + x^{11})$ can be implemented as shown in Figure 1. The improvement in decoding speed is possible only when the decoder has some computation capability or facility that is available to the decoder. But this decoding circuit is clearly more complex than a conventional decoding circuit because a fast error-trapping decoder requires more logic. However, since speed and simplicity cannot be achieved at the same time, some trade-off must be made.

The error-trapping decoder for the Fire code described above requires at most $2b + e - 3 = 72$ shifts of the two syndrome registers to carry out the error-correction process, while the conventional error-trapping decoder requires $n = LCM(e, 2b - 1) = 693$ shifts. Since n is much greater than $2b + e - 3$, it can be easily seen that decoding speed is improved. The status for the Error-Pattern Register and Error-Tracking Register of the (693, 676) Fire Decoder according to cyclic shifts are shown in Table 1. and Table 2.

Table 1. Cyclic Shifts for the Error-Pattern Register of the (693, 676) Fire Decoder

Shift No. j	Syndrome polynomial	Register contents
0	$x + x^6$	0 1 0 0 0 0 1 0 0 0 0
1	$x^2 + x^7$	0 0 1 0 0 0 0 1 0 0 0
2	$x^3 + x^8$	0 0 0 1 0 0 0 0 1 0 0
3	$x^4 + x^9$	0 0 0 0 1 0 0 0 0 1 0
4	$x^5 + x^{10}$	0 0 0 0 0 1 0 0 0 0 1
5	$1 + x^6$	1 0 0 0 0 0 1 0 0 0 0
6	$x + x^7$	0 1 0 0 0 0 0 1 0 0 0
7	$x^2 + x^8$	0 0 1 0 0 0 0 0 1 0 0
8	$x^3 + x^9$	0 0 0 1 0 0 0 0 0 1 0
9	$x^4 + x^{10}$	0 0 0 0 1 0 0 0 0 0 1
10	$1 + x^5$	1 0 0 0 0 1 0 0 0 0 0

Table 2. Cyclic Shifts for the Error-Tracking Register of the (693, 676) Fire Decoder

Shift No. j	Syndrome polynomial	Register contents
0	1	1 0 0 0 0 0
1	x	0 1 0 0 0 0
⋮	⋮	⋮
6	$1 + x$	1 1 0 0 0 0
⋮	⋮	⋮
38	$1 + x + x^3 + x^4$	1 1 0 1 1 0
⋮	⋮	⋮
61	$1 + x^4 + x^5$	1 0 0 0 1 1
62	$1 + x^5$	1 0 0 0 0 1

The Reiger bound can be expressed by $b \leq (n - k)/2$. The ratio $R = 2b/(n - k)$, which is called the burst-correcting efficiency, is unity and has an upper bound $b = (n - k)/2$. Codes which meet $z = 1$ are said to be optimal. Since z is expressed by the ratio $2b/(m + 2b - 1)$ for a Fire code, we obtain $z=0.62$ for $b=5$ and $m=7$. If b is chosen to be equal to m , then we have $z=0.7$ for $b=m=7$. As a result, Fire codes are not very efficient with respect to the Reiger bound.

IV. CONCLUSION

The decoder for burst-error correction which often occurs in wireless communication and storage system has been proposed in this paper. Some prerequisites comment for the code design is described and quoted. In the decoding system, high speed error trapping method is proposed. The (693, 676) Fire code decoder using the error pattern register and the error tracking register is implemented and two registers are described how they work. The decoding time can be shortened than that of existing techniques. The decoder is very suitable for the implementation with VLSI, and will be used for the wide applications in information transmission and digital storage systems. This circuit for decoding is well suited for the implementing nano-integrated circuits and is adopted for a wide range of applications in storing digital data and transmitting information.



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