A Low Power 6T-Auto Awake Mode-SRAM Design for high speed storage application

B. Satheesh, Prabhu Benakop

Abstract: ***In the digital world, Static Random Access Memory (SRAM) is one of the efficient core component for electronics design, it consumes huge amount of power and die area. In this research, the SRAM design analysis in terms of read margin, write margin and Static Noise Margin (SNM) for low power application is considered. In SRAM memory, both read and write operation affect by noise margin. So, read and write noise margins are considered as the significant challenges in designing SRAM cell. In this research, robust 6T-SRAM cell is designed to decrease the power utilization. The Auto Awake Mode is developed to control the entire 6T-SRAM cell design. The proposed 6T-SRAM- Auto Awake Mode (6T-SRAM-AAM) was implemented to reduce power utilization of understand and write down operation inside the 20 nm FinFET library. The experimental results showed the proposed 6T-SRAM-AAM design reduced power consumption of read & write operation up to 25% to 33.33% compared to existing Static RAM cells design.***
Keyword: SRAM, low-power consumption,6T &7T- SRAM design, Auto Awake Mode.

I. INTRODUCTION

Nowadays, the handheld electronic Instruments such as movable telephone, handy cam, Loptap etc.are becoming more important part of personal computing and is mainly calculated to offer a matching set of compute, message and informational apparatus in a gadget about the size of standard palm. The low down power SRAM circuits contain develop into a important component of many VLSI circuit chips [1-3].In past decades, the traditional CMOS technology has been affected by two major problems, those are less reliability and more power utilization [4]. Through a write down operation,60% of the total dynamic power require to operate bit lines in traditional SRAM cell designs [5],[6]. The Cache built on adiabatic principles is introduced based on slowly varying supply voltages [8].

This method reduces the total power dissipation, which uses several power switches and the position produce circuit in extra area overhead. To overcome the above-mentioned problem, the 6T-SRAM-AAM cell is designed in this paper. The AAM is controlled by the SRAM cell design when the AAM condition was one, at the time SRAM cell perform otherwise it does not perform. The proposed 6T-SRAM-AAM cell design efficiently reduced power consumption and impediment of the system balance to the 7T-SRAM cell design.

Organization of this paper as follow, part-2 presents a literature survey of recent papers based on SRAM cell designs. In part-3 a brief explanation of the 6T-SRAM-AAM cell design is presented, part-4 show the proportional experimental results of existing and proposed 6T-SRAM-AAM cell design strategies.And finally part-5 explained about proposed work summary

II. CORRELATED WORK

Many researchers have suggested a numbers of the techniques for SRAM cell design. A brief evaluation of a few significant Static RAM cell designs is existing in this part. Byung-Do Yang [5] proposed a small power Static RAM using BL accuse recycle for understand writing and put in writing operations. This proposed charge recycling SRAM design was based on the hierarchical BL architecture and BL charge recycling method. The proposed method was achieved less degradation of SNM, 17% & 84% of read and write power consumption respectively achieved. other than the operation speed is inadequate to 145MHz.W. Kang *et al.* [9] introduced a non-volatile SRAM propose with Magnetic Tunnel Junction. They designed MAP of the MTJ device. The switching techniques provided better accumulate power, delay, and dependability disquiet. The main limitation of the system is, it consumes more switching power. A. Makosie*jet al.* [10] introduced TFET-based 8T SRAM cell. The 8T SRAM cell maintains full functionality in all operation modes at 1V supply voltage with no architectural limitation linked to the half-selection problem. The cell design allowed the use of long word lines with bit interleaving. The major drawback of the Static-RAM design is, whenever the supply voltage increases, at the time substantial leakage power also increases. E. Karl *et al.* [11] proposed a huge presentation, voltage scaling of 162 Mb Static RAM range was urbanized in 22nanometer tri-gate bulkiness equipment. The 22 nm tri-gate technology delivered a 0.092m High-Density Cell (H-DC) bit cell and 0.108 m Low Voltage Cell (LVC)bit cell. The main limitation of the 6TStatic-RAM design is, internal sensing delay is very high. These all related works have several issues like more delay and power consumption, high critical cell design. Here, the 6T-SRAM-AAM cell design is implemented to overcome these problems and to minimize dissipation of power and delay comparasion of existing SRAM cells design.

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III. 6T-SRAM-AAM SYSTEM

In this paper, the SRAM architecture design consists of 6Ts with a symmetrical configuration that maintains the threshold voltage of the system. The SRAM plays an important role in VLSI technology due to its low-latency and large storage. A numbers of transistors employed in the SRAM circuit, which limits the reliability of the circuit . In this work, the designing based on the AAM circuit design. A brief explanation about the conventional 7T-SARM cell and 6T-SRAM-AAM cell design is explained below.

3.1. 7T- SRAM

The block diagram of the 7T- SRAM is shown in Fig. 1, which provides high read stability. The read and write path of 7T- SRAM cell is independent and never interference mutually . The design of 7T SRAM cell reduces the activity factor of the discharging BL pair to perform a write operation. This cell design uses 2-PMOS transistor (MFET1 and MFET3) for write operation and NMOS transistor (MFET 5, MFET 6, and MFET 7) for read operation. The 7T SRAM cell is made by single BL, for the write operation and BL and RL used for reading operation in 7T SRAM cell design.

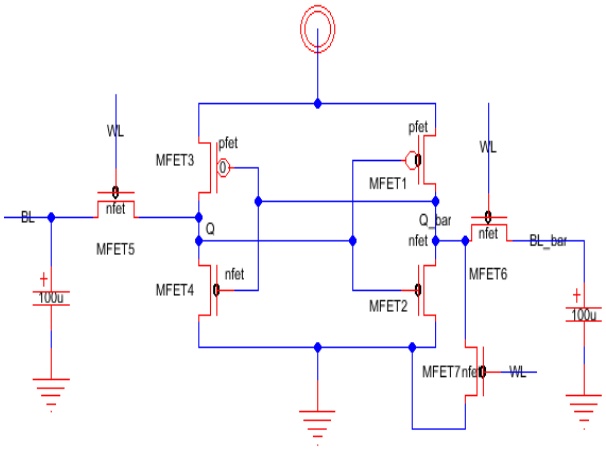

Figure 1.Block diagram of the 7T-SRAM circuit design.

The conventional 6T SRAM circuit requires three BL (like 2-BLs (BL &BL_b) and one WL used for any read and write operations. Hence, the 6T SRAM cell designachieved the less power consumption compared to 7T- SRAM design. To reduce the power requirement for charging/discharging in the 7T- SRAM circuit a single BL is used [12].The brief explanation of proposed 6T- AAM- SRAM Cell Design is described in below section.

3.2. 6T- AAM- SRAM Cell Design

Fig. 2 shows a circuit diagram of the 6T-SRAM-AAM design, which balancing several factors including area, power/leakage consumption, and speed performance.

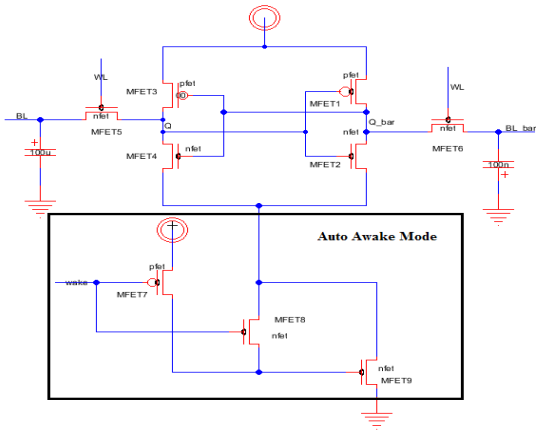

Figure 2. 6T-SRAM-AAM circuit diagram.

The 6T-SRAM-AAM method consists of nine- MFETs. It has 2- cross-coupled inverters that show the Bi-stable latching circuitry. Two storage nodes (node1 and node2) in the 6T-AAW- SRAM, which is accessed by two-additional transistors connected to 2-BL (BL and BL_b). These transistors are called as pass transistor and access transistor to control the storage cell in the read &write operation [18]. Access to the cell is enabled by the WL, it controls the 2-access transistors such as MFET5 and MFET6, which are connected by BLs: BL and BL_b. To transfer the data for both read& write operations during reading access, the BLs are actively driven low and high by the inverters in the 6T-SRAM-AAM design.

3.2.1. 6T- AAM- SRAM operation

The 6T SRAM is traditional choice for most on-chip memory designs. The cell design is required for balancing the several factors in terms of speed, silicon area and power consumption. The challenging issues in designing the optimum 6T SRAM cell are less cell region to obtain huge density memory, less power and low down leak current for group of cells function system. The 6T-SRAM-AAM design is based on two-different states such as read state and write state. The three different state works as follows,

3.2.1.1. SRAM Read Operation

For a proper read operation, both the BLs such as BL and BL_b are pre-charged to Vdd. When the WL goes high (value 1) it enables the access transistors. Some read pulses are stored in the memory after the read operation is done. If the internal node Q value is bit 1 then the internal node Q_bar is bit 0. At the time value of the BL_bar is bit 1 and internal node Q_bar is bit 0. Here, the BL and BL_bar values are used to sense the amplifier, which act as a comparator.

3.2.1.2. SRAM Write Operation

If the content of the memory is 0 then the internal node (Q_bar) value becomes 1 and these values are stored in Q. The WL= 1 value is required to write operation in the 6T-SRAM- AAM-. If

the WL=0, it is not possible for a write operation. Here, an input operation is done by using BL and BL_bar. The BL_bar is connected to ground because of the internal node Q value is 0 at the time Vdd value is 1, here voltage is different so that entire system voltage is discharged.

3.2.1.3. 6T- SRAM Design based on AAM Operation

The AAM design has 2-PMOS and 4-NMOS. AAW design having 3T such as 1 PMOS (MFET7) and 2NMOS (MFET8, MFET9).The 6T- SRAM output is given into the MFET 8 and MFET 9, these base stations are connected to MFET7, which act as AAM. The AAM control the overall 6T-SRAM cell based on power consumption. By using AAM circuit, the static power of the SRAM design will reduce. In the AAM- SRAM cell, data will be maintained and a voltage around SRAM memory must be greater than the minimum data retention voltage. Earlier do research perform to decrease the power consumption of Static Rams design. In that design, which is employed to increase the fundamental technology of transistor size and leakage. The existing high-performance SRAM cells usean asymmetric configuration of the 6Ts It can minimize the leak by employing upper V_t, but the usage of high V_t transistor causesthe performance of SRAM cell by unacceptable line margin. In this research, the asymmetric SRAM cells minimize the leakage by selecting the preferred state and this also reduces the performances of transistors when cell is in the same status. The experimental results of proposed 6T-SRAM-AAM cell design is briefly explained as follows.

IV. RESULT AND DISCUSSION

A power and delay of an SRAM cell designs are the two key design circuits in the nanometer scheme. For comparison, this paper Employed the 6 Transistors-Static RAM-AAM cell design. This paper implemented 20nm technology in FinFET library for 6T-SRAM-AAM cell design. The Schematic track diagram of the 6Transistor-SRAM –AAM is given below Figuer.3.

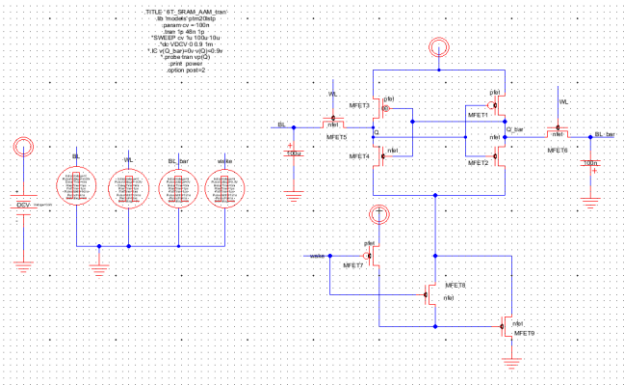

Figure 3. Schematic circuit diagram of the 6Transitor-SRAM-AAM

4.1. Area computation

The area can be optimized by having a lesser number of cells and by replacing multiple cells with a single cell that includes both functionalities. In this paper, the transistor area is computed by transistor width and length (1Transistor = 15 (width)*24 (length) = 360n).

4.1. Power computation

The power consumption by the particular source is computed by multiplying the average
current drawn from the source and voltage provided by the source.

4.2. Delay computation

The Static RAM delays are termed as the time required to change Static RAM cell design one sense gate to another sense gate. The wait is computed difference of time between the 0 to 0.9 voltages

Table.1. Implemented based on 20nm technology for existing methods like 7T-SRAM, 6T-SRAM, and 6T-SRAM-AAM.

Design	Operation	Area (nm)	Dynamic Power (µm)	Delay (ns)
7T-SRAM	Read	2520	900	0.5
6T-SRAM	Read	2160	540	0.1
6T-SRAM-AAM	Read	3240	360	0.01
7T-SRAM	Write	2520	1080	0.4
6T-SRAM	Write	2160	720	0.2
6T-SRAM-AAM	Write	3240	540	0.01

Table 1 shows the area, power consumption and delay performance of conventional 7T &6T SRAM cell design and 6T-SRAM-AAM cell design. In both methods occupied more area and consume more power. In this paper, the 6T-SRAM cell is designed by using AAM, which used SRAM operation control by the AAM, that improved low-powerconsumption and delay performance compared to 7T-SRAM and 6T-SRAM cell design. The comparison graph of the power and delay performances are shown in Figure 4 and 5. These results are drawn by using 20nm technology for different methodologies. According to the graph, the blue and orange color represent existing technology and the gray color represent6T-SRAM-AAM cell design. From this graph, it is clear that 6T-SRAM-AAM design consumes less power and occupied less area than the 6T-SRAM and 7T-SRAM cell design.

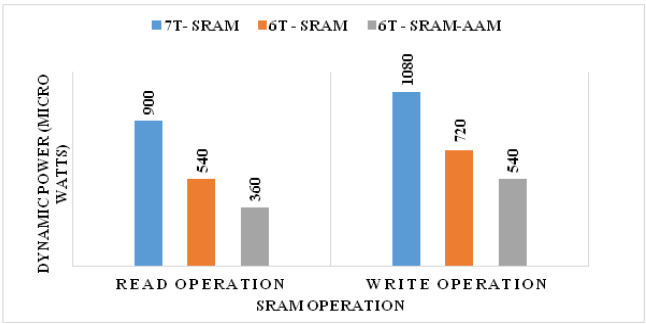

Figure.4.Performance of dynamic power for SRAM Cell designs in 20nm technology.

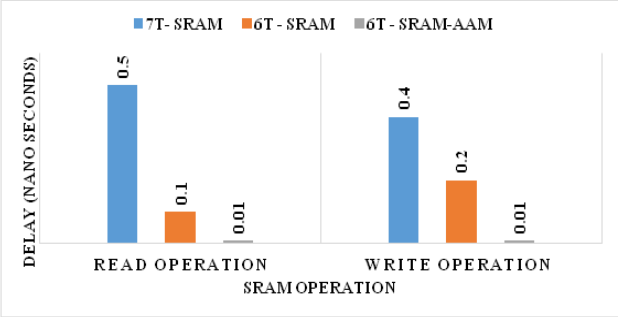

Figure 5. Performance of delay for SRAM cell designs in 20nm technology

Tab.2. Reduced performance of total dynamic, static power and total delay for existing and 6T-SRAM-AAM design.

Design	Total Dynamic power (µW)	Total static power (µW)	Total Delay (nS)
7T-SRAM	1980	27.9	0.9
6T-SRAM	1260	21.15	0.3
6T-SRAM-AAM	900	18.45	0.02

The total dynamic power, total static power and total delay performance of the existing and 6T-SRAM-AAM design shown in Table2. From the table, total dynamic power is computed based on read and write operation, if the condition WL=BL=RL=1. In Table2, it clearly shows 900 µW of total dynamic power is reduced by using 6T-SRAM-AAM design compared to existing methods like 7T-SRAM and 6T-SRAM.Furthermore, if the condition WL=BL=RL=0, then the read &write operation is not possible in the SRAM circuit design. At the time the total static power is computed in SRAM cell design. The 18.45 µw of total static power minimized by the 6T-SRAM-AAM design compared to existing SRAM cell designs. As well as the total delay also reduced 0.02 ns by using 6T-SRAM-AAM design compared to existing methods. Fig. 6 shows the compression graph of total dynamic/ static power performance for SRAM cell designs in 20nm technology. Fig. 7 shows comparison performance of total delay for SRAM cell design in 20nnm technology.

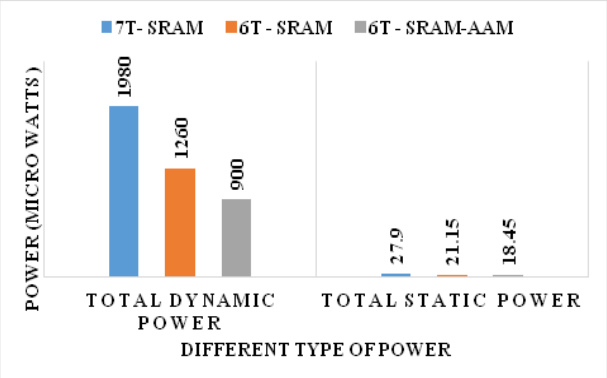

Figure 6. Comparison performance of total dynamic and static power for SRAM design in 20nnm technology

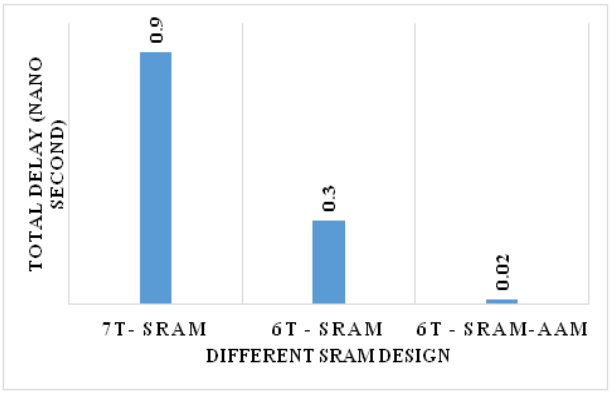

Figure 7. Comparison of total delay performance for 20nnm technology.

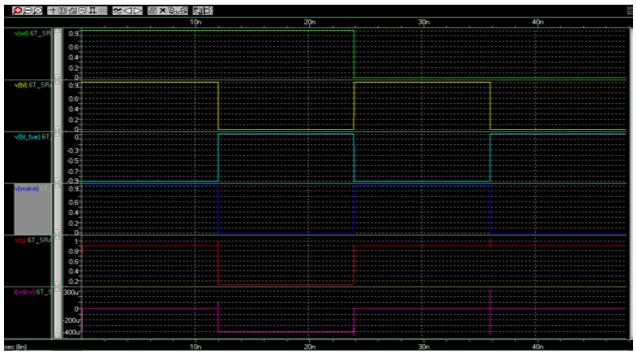

Figure 8.Performance of Read operation of the 6T-SRAM-AAM design

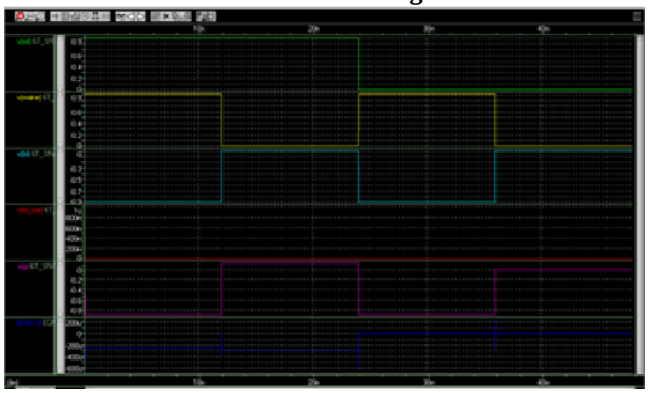

Figure 9.Performance of Write operation of the 6T-SRAM-AAM design

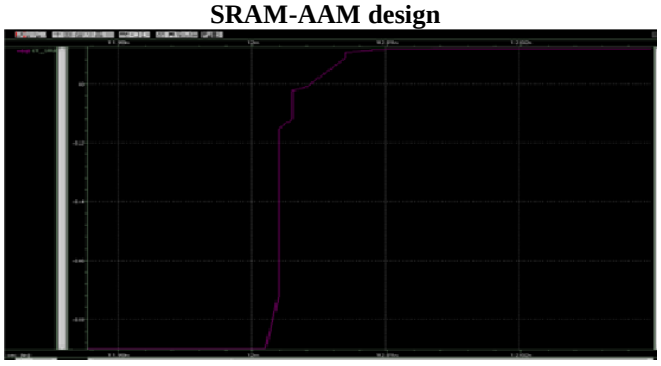

Figure 10.Performance of delay performance of the 6T-SRAM-AAM design

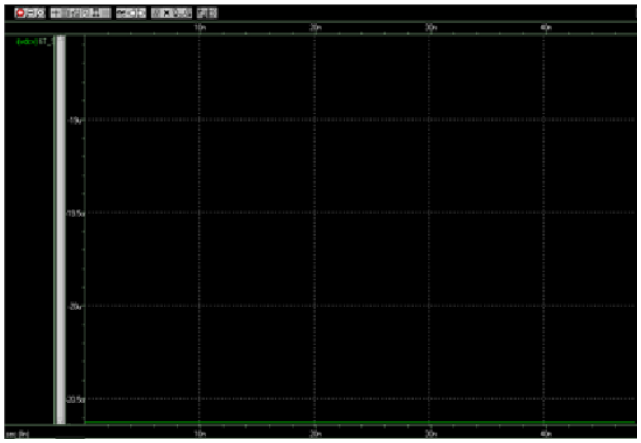

Figure 11.Performance of Static power of 6T-SRAM-AAM design

Fig. 8 illustrates the Rd function of the 6Transistor-StaticRAM-AAM design. Fig. 9 shows the write operation of the 6T-SRAM-AAM design. The delay performance of the 6T-SRAM-AAM design is illustrated in Figure10. Fig. 11 shows the static power performance of the 6Transitpr-Static RAM-AAM design. Fig. 8 shows the conditions of BL is 0.9v, WL is 0.9v and BL_bar is -0.9v in read operation of the 6T-SRAM-AAM design. Fig. 9shows the condition BL is -0.9v, WL is 0.9v and BL_bar is 0 in write function of the 6T-SRAM-AAM design. In Fig. 10, delay performance computed between the 12 v to 12.1v. In the Fig.11, static power is computed by the threshold voltage (v) and current (I). Finally, the6T-SRAM-AAM design is used to calculate the static power performance of BL, WL and BL-bar.

V. CONCLUSION

The SRAM design is used for high-speed operation with less power scheme by employing small voltage swings on the bit-line margin. In this research, the 6Transitor Static RAM cell was designed in 20nm FinFET technology based on AAM controller to minimize the power consumption of the both Rd& WR operation for real time applications.. Hence, the proposed method achieved 33.33% of dynamic power (µm) in read operation, 25% of dynamic power (µm) in existing 6T Static RAM cell.In this research, both 7Transistor SRAM and 6T SRAM cells has been designed and compare to this cell designs the proposed 6T-SRAM-AAM design obtained better power consumption. In Future work, the leakage current will play significant role to minimized power consumption. By creating a layout of the transistors SRAM cell design in Xilinx or Cadence tool, it can minimize area, respectively.

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