Design of 21t Sram Cell for Low Power Applications

B.K.L Aruna , D.Sravani

Abstract: ***Data is stored in memories and the memories can be classified into static and dynamic memories. The static memories are widely used in today's world due to their design simplicity and speed. The emission of alpha particles usually gives rise to soft error through package radio active delay. The distribution of electrons is disturbed by the positive charged alpha particles which travels through the semiconductor. A signal which is digitalized can be altered from 0 to 1 or vice-verse if the disturbance is large. Many electronic components which are made up of semi conductors are susceptible to damage by radiation; But the susceptibility to radiation damage is decreased by the changes in the design and manufacturing which are based on the non hardened equivalents for radiation hardened components.The merits of 21T SRAM cell are robust and achieves high soft error tolerance and that the upsets can be tolerated when compared to 13T SRAM cell. Another advantage of 21T SRAM cell is that there is a reduce in power and delay when compared to 13T SRAM cell and can be practised in space applications for designing power supplies and batteries. This paper evaluates the 21T SRAM cell which can be operated at low voltage sub threshold region and is evaluated at 180nm using cadence tool.***

Index Terms: ***6T SRAM cell, 13T SRAM cell, 21T SRAM cell, Cadence virtuoso,Dynamic random access memory,Static random access memory, soft errors, sub threshold region.***

I. INTRODUCTION

The rise of modern communication systems and the signal processing systems have paved the way for the SRAM memories to be used in many applications such as space. The memory components and processing units are main elements for designing system on chips(SoC's). On the whole the memory components occupy 60 to 70% of the area on the dies and consume power [1] sometimes. A group of semiconductor memory is the static random access memory and this memory circuit is called a bi stable latch circuit since it is used to store each bit. The term static is differentiated from dynamic in the way it is refreshed periodically. SRAM shows data remanence, but sometimes it is still volatile in the sense that the input or output data is disappeared when the memory is switch off. The conventional SRAM which consists of six transistors is simple but has limits to access low power devices and to reduce the power consumption various methods have been introduced. This static random access memory is saved to be the best useful and the most general memory advancements in now a days. Single event upsets in micro electronics are due to the high energy particles [2] which are moving in the natural space environment and which strikes sensitive parts of the micro electronic circuits. Static Random Access Memory with the use of technology scaling occupies a large amount of space and power consumption on the system on chip devices.The memories which are used for storing the data that is digital within the huge extent of the digital system are called semiconductor memories. A soft error is seen whenever a radiation event causes a disturbance in charge which reverses or flips the state of the data in the cell of the memory, register, latch and flip flop. This glitch is defined to be a soft error [3] because the data is temporarily impaired by the emission of radiation and if at all a new data is written to the device the device stores the data correctly. The single event upset [4] is nothing but a soft error.

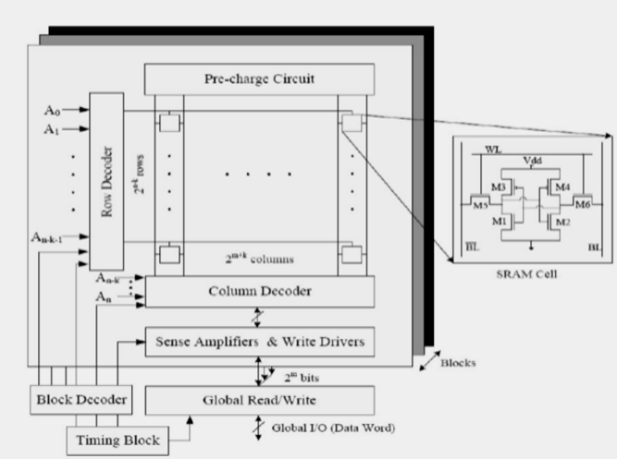

Fig 1.Architecture of SRAM cell

The architecture of SRAM cell consists of precharge circuit, SRAM cell, decoder and timing block.The precharge circuit is responsible for pulling up the bit lines to high voltage in both the operations which include reading and writing . In general the decoders are of many types, but the important two types of decoders are given here. One is row decoder and other one is column decoder. The row decoder gives the output as 2n when it takes an n- bit address. These row decoders are used to name the selected row in the memory array. The selected word line is operated according to the address that is given to the decoder. After all the bit lines are precharged to a high voltage, the next operation is to select the column of the memory cell array that is to be selected in the read and write operation. A multiplexer or the decoder is used to evaluate the column selection.

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The selection of 2m columns is computed by using m-bit column address. To read the data from the memory the sense amplifier is used. The low power signals are detected by the sense amplifier from the bit lines which is stored in the memory cell. The sense amplifier amplifies small swing voltages[7] to the logic levels that are recognizable so that the data can be interpreted correctly. The SRAM cell size can be determined as 2^mwords or 2^m x n bits where 'm' indicates address lines and 'n' data lines. The most commercial size of word is in eight bits, that means for every of the 2^m various words within the SRAM chip, a single byte can be read or written . The timing block is used to give specific timing to the SRAM cell. The conventional 6T SRAM cell design and operation is represented in section II. Section III consists of the existing 13T SRAM cell design and operation. Section IV gives the design and operation of the 21T SRAM cell. The simulation results are shown in section V and section VI shows the conclusion related to the proposed work.

II. CONVENTIONAL SRAM DESIGN AND OPERATION

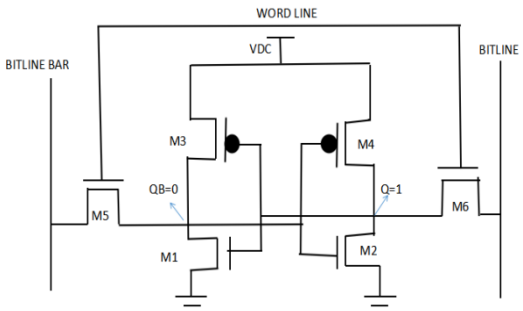

Fig 2. 6T SRAM cell block diagram

A SRAM cell is performed by three separate states: standby mode which measures that the circuit is in empty state , reading mode which means the data has been appealed and lastly writing mode which means renewing the details. The operating mode of SRAM has read mode and write mode and the noise can be measured using read .and write stability respectively. The states which are discussed above work in the following manner as shown below.

STANDBY MODE

When the word line is not affirmed, the cell is disconnected from the bit lines through the access transistors M5 and M6.

The transistors M1-M4 form two cross coupled inverters which will continue to boost each other until they are connected feedback [8] to the power supply.

READ MODE

Ideally, the reading function in the sram cell takes place by inserting the word line WL and reading the SRAM cell state by one access transistor M6 and bit line BL. Thus these lines are similarly large and have extended parasitic capacitance. Thus to increase the speed of reading ability, a complicated procedure is used that is: First in read cycle the lines are precharged to high voltage. Then the word line is insisted which implements both transistors M5 and M6, which causes the bit line voltage to marginally come down. Then the bit lines BL and BL' have a short voltage difference between them. A sense amplifier is used for detecting the potential of the lines and detects which detects which bit line has the higher voltage and thus tells us whether 0 or 1 is stored. The read operation will be faster if the sensation of the amplifier is higher. As the NMOS is more strong , the pull-down is easier in NMOS than in PMOS. Thus, the bit lines are normally pre charged to high voltage. If the pre charging is done at low voltage then the power consumption decreases.

WRITE MODE

First the write cycle is started by implementing the value which is to be written to the bit lines. First the bit lines BL is set to 1 and BL' to 0. When the reset pulse is applied to the SR-latch there is the change in state of the flip flop from 0 to 1 which is written by complementing the bit lines.The word line is then applied and the value is stored. The preceding state of the cross inverters is nullified by the bit line input drivers as these drivers are strongly designed than the relatively uncertain transistors. In practical, the access transistors M5 and M6 are stronger than the bottom NMOS and the top PMOS transistors. This is because the NMOS have strong pull up than the PMOS transistors. Therefore by this means the cross coupled inverters magnify the process of writing [12].

III. 13T SRAM CELL DESIGN AND OPERATION

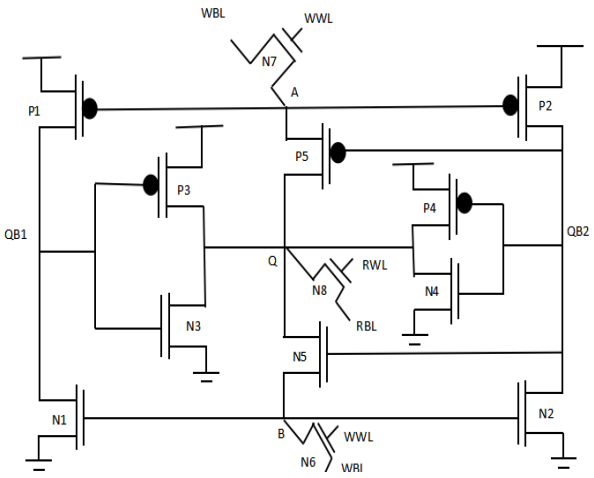

Fig 3. 13T SRAM cell block diagram

The main purpose for designing the 13T SRAM cell is for implementing robust, low potential, ultra low power operation [16-17] in field application such as space and other radiation prone environments. These requirements can be full filled when the circuit is designed using a dual and separated feedback mechanism to decrease the susceptibility which arises due to supply potential scaling [9].The designed 13T SRAM cell is addressed in fig 3. The 13T SRAM cell is designed on the basis of five separate nodes namely Q,QB1,QB2,A and B with correct input value stored at node Q. The node Q is forced by a pair of CMOS inverters which are names as N3,N4,P3 and P4 which are again directed by the complementary data levels

of the transistors P1, P2, N1 and N2 which are guarded by the general nodes A and B which are given back through feedback. These nodes A and B are linked to the node Q by a couple of inverted transistors P5 & N5 which are forced by node QB2. As there is separated feedback mechanism there rises node separation which decreases the soft error capability.This design completely protects the node Q from the soft error upsets , but also produces critical charge at node Q.

STORAGE MECHANISM

Opening with logic 1 state, the low level at node QB2 implements Q to charge A to VDD by using P5 transistor so that the PMOS transistors will be turned off and the currents through the QB1 and QB2 will be eliminated. The currents are of different types out of which the flow of leakage currents from the heavily forced node Q charge node B using N5 transistor which then switches on N1 and N2 transistors and implements a route of discharge to assist in locking the nodes QB1 and QB2 to a value 0. A similar process takes place during 0 state also. In the 0 state the node QB2 is at level 1 which allows the node B to discharge Q by the use of N5 transistor and eliminating the paths from the nodes QB1 and QB2 by the use of the transistors which are represented by N1 and N2 respectively. The value stored at node A will come to node Q through P5 which allows the P1 and P2 transistors to nodes QB1 and QB2 in order to restore the value of charge vanished at the nodes.

V . 21T SRAM CELL PROPOSED DESIGN AND OPERATION

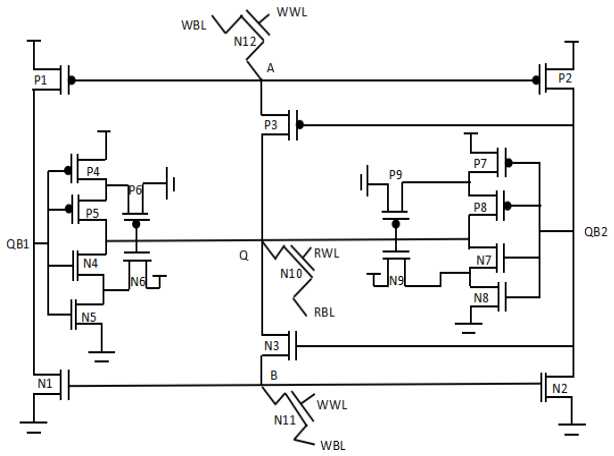

Fig 4. 21T SRAM cell block diagram

The design of the 21T SRAM cell is shown above . Opening with logic 1 state, the low level at node QB2 implements Q to charge A to VDD by using P5 transistor so that the PMOS transistors will be turned off and the currents through the QB1 and QB2 will be eliminated. The currents are of different types out of which the leakage currents from the strongly forced Q node charge node B through N5 which then turns on N1 and N2 and implementing a path of discharge to assist in locking QB1 and QB2 at a value 0. A similar process takes place during 0 state also. In the 0 state the node QB2 is at level 1 which allows the node B to discharge Q by the use of N5 transistor and eliminating the paths from the nodes QB1 and QB2 by the use of the transistors N1 and N2 respectively. Any value stored at node A will come to node Q through P5 which allows the P1 and P2 transistors to nodes QB1 and QB2 in order to restore any value of charge lost at the nodes.The operation of the above designed SRAM cell is similar to the 13T SRAM cell. The designed SRAM cell has more number of transistors which increases area but reduces the power consumption and delay. To decrease the power consumption multiple supply voltages are given to the designed SRAM cell. The designed SRAM cell is used for many space applications which are used for designing power supplies and solar batteries. The designed SRAM cell not only reduces delay and the power consumption[15] but also implements the circuit to be robust practically from soft error upsets.

VI. SIMULATION RESULTS

A . 13T SRAM CELL

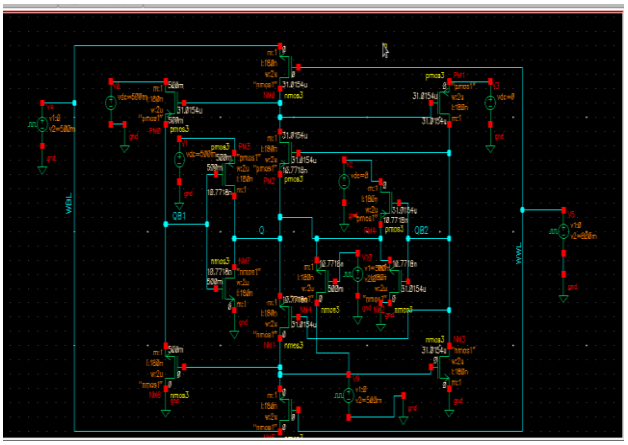

Fig 5. 13T SRAM cell design using cadence

The existing dual feedback separated 13T SRAM bit cell is designed as shown in figure above. Due to this separated feedback mechanism the flipping of data at the nodes can be reduced.

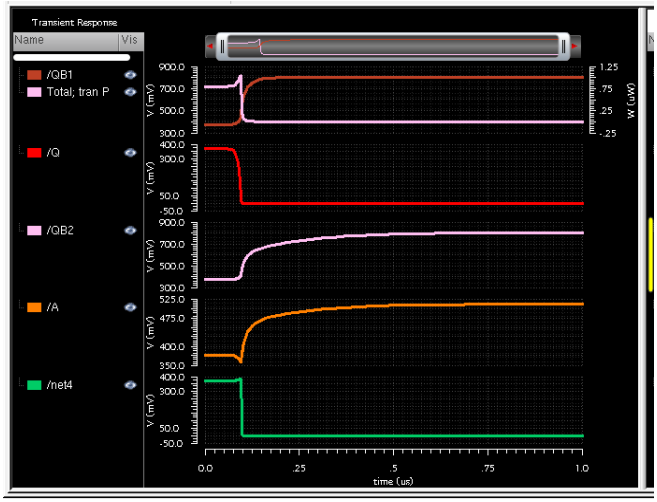

Fig 6 . Transient waveforms of 13T SRAM bit cell

The output of the 13T SRAM cell is shown above. Thethrough put whatever is there at Q will be inverted and willappear at QB1and QB2.
The output which will appear

at QB2 will be equal but some lower in amplitude than QB1.

B. 21T SRAM CELL

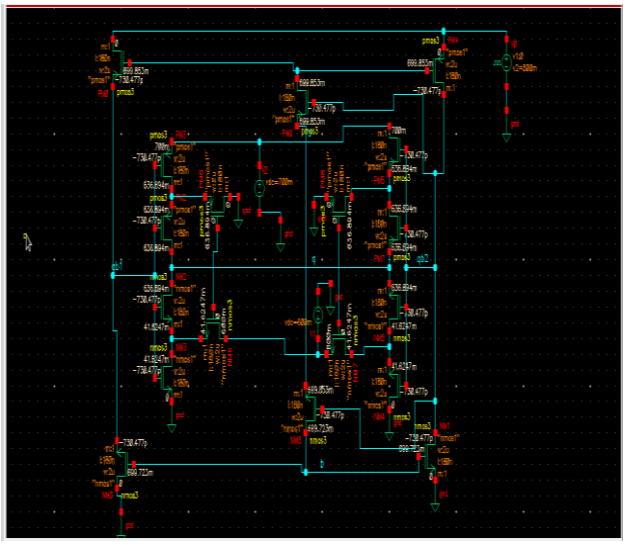

Fig 8 . 21T SRAM cell design using cadence

The proposed 21T SRAM cell is designed above is indicated in the figure. For reducing power consumption and delay the designed circuit which is indicated above is implemented .

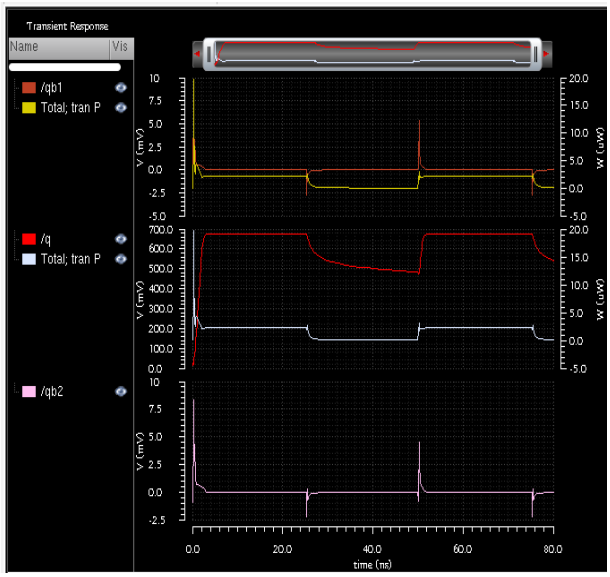

Fig 7 . Transient waveforms of 21T SRAM bit cell

The output of 21T SRAM cell is indicated above. Whenever there occurs an upset at one node the occurred upset is reduced by the dual driven feedback mechanism.

A. COMPARISIONS BETWEEN 13T AND 21T SRAM CELLS

PARAMETERS	1. 13T BIT 2. CELL	21T BIT CELL
Power consumption	0.876uW	0.250uW
Propagation delay	20.10nsec	40.2nsec
Read Stability	400.5m in dB	1700m in dB

Table 1. Comparison table regarding some parameters of 13T & 21T SRAM cell

B. ADVANTAGES , DISADVANTAGES AND APPLICATIONS

The initial and the foremost advantage of the designed 21T SRAM cell is that as the nodes in the circuit increases not only the power consumption, delay decreases, but also there is an increase in stability which results in reduction of static noise margin. The other advantage is that as the number of nodes increases the data cannot be flipped.

The other advantage is that when the data is taken out from node q the temporary upsets appearing on other junctions is allowed. The vertex which are serving are formed with duplication to see that the SEU will be weaken by the other branches.

For example : when the affect of radiation allows a charge shift on any nodes of the designed bit cell, the other nodes of four are implemented such that the state change at this branch cant change the value which is stored in the cell and change can be removed within a recovery time.

The disadvantage is that as the number of transistors are increases the area increases which increases the die area in the silicon chip.

The designed 21T SRAM cell can be used in the space applications in the use of power supplies and heavy batteries.

IV. CONCLUSION

This paper is designed mainly for robust, low voltage and low power applications which are operated at high radiation environments. In low power space applications the designed circuit is a best solution in low power applications. Compared to previous solutions , this design implements arrays which diminishes the range of area and consumption of power by 30-40%. By varying potential and process parameter changes, the proposed solution shows high stability. In the region of sub threshold , high radiation tolerance was achieved. For improving the bit cell robustness, dual and separated feedback mechanism is found. The SEU tolerance was inherently provided by two basic methods. One is the data which was to be

read out from the node Q , is reducing the upsets so that they can be tolerated. Other is that the remaining boosting nodes are well made with repentant values so that the upset will be engaged through the another branches.

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