Impact of band to band Tunneling on Transient performance of Dual Gate Tunnel Field Effect Transistor (TFET)

Deepak Kumar, Raj Gaurav Mishra, Ranjan Mishra, Amit Kumar Shrivastava

Abstract: ***Tunnel Field Effect Transistor (TFET) is gated reverse biased P-I-N diode structured semiconductor device and can be considered as a reliable low power device. TCAD (Sentaurus 2D) simulations for various Gate metal work function (4.1-4.3 eV) shows that its ON-current (I_{ON}) arises from quantum mechanical band-to-band tunneling (B2BT) and observed that threshold Voltage (V_T) for TFET decreases with increase in Gate metal work function. The thermionic emission of electrons in MOSFET limits the sub-threshold swing (SS) by 60 mV/dec whereas TFET has potential for low SS ie. SS<60 mV/dec. TCAD Simulations confirmed that that the Gate – Drain capacitance (Cgd) strongly follows the Gate capacitance (Cgg) all over the voltage range (0-0.9V) which increases the miller capacitance for TFET. It is investigated that for TFET, the injection of carriers into the channel is through B2BT which effectively couples the Gate charge to the Drain. A look up table based Verilog-A model is generated for TFET and used to simulate the static and dynamic behavior of TFET based digital circuit in Cadence spectre. Miller effect causes the peak voltage overshoots are noticed at the drain side during transient responses and can be responsible for dynamic power loss and high turn ON/OFF delay***

Index Terms: B2BT, VerilogA, tunneling, miller effect, Gate capacitances.

I. INTRODUCTION

As the MOSFET technology is shrinking today, the number of transistors per unit chip area tends to increase the leakage and thus increases the standby power consumption in the electronic devices [1]. MOSFET scaling below 32 nm limits its performance by facing several [2]. Tunnel FET is gated reverse biased P-I-N diode structured semiconductor device and the ON current (I_{ON}) arises from B2BT mechanism. Charge transport mechanism in MOSFET limits SS by 60 mV/dec., whereas for TFET B2BT mechanism shows the potential for lower value of SS (< 60 mV/dec) for low voltages. The leakage energy dissipation (E_L) in transistor given by eqn.(1)[3-4].

$$E_L \propto V_{DD}^2 . 10^{\frac{-V_{DD}}{SS}} \quad (1)$$

Revised Manuscript Received on July 05, 2019

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From the eqn. (1) it is clearly shows V_{DD} and SS have dominant impact on device performance. Scaling down V_{DD} definitely decreases the leakage energy consumption in the digital circuits but at the same time it affects the speed of operation. Therefore, one way is to find a semiconductor device with lower SS (<60 mV/dec) than conventional MOSFET and TFET exhibits this property due to injection of electrons from source to channel due to B2BT mechanism which make it suitable low power digital applications.

The motivation for describing the eqn. 2 is to show that SS ($dV_{gs}/d(\log I_{ds})$) of the TFET has different kind of parameter dependencies compared to a MOSFET and is shown below

$$SS = \ln(10)\left[\frac{1}{V_{eff}}\frac{dV_{eff}}{dV_{gs}} + \frac{E+b}{E^2}\frac{dE}{dV_{gs}}\right]^{-1} \quad (2)$$

The terms in eqn.2 are not limited kT/q and the first term can be maximized to achieve a lower sub-threshold swing. Accordingly, the SS for TFET increases with gate-source voltage and much steeper at lower gate voltages. The second term describes about derivative of the electric field (*E*) across the junction and should be maximize to achieve lower SS. This reduced (*E*) the sub-threshold leakage for electronic devices in standby mode (see eqn. 1).

This paper reports the device simulation of a 30 nm dual gate P^+ I N^+ Si TFET structure using TCAD Sentaurus-2D to obtain its I/C-V characteristics. The small signal AC analysis (1 MHz) was carried out in Sentaurus 2D to investigate the capacitances formed in the device and its variation with the Gate voltages (C-V plots) for both TFET and MOSFET The small signal AC analysis (1 MHz) was carried out in Santaurus 2D to investigate the capacitances formed in the device and its variation with the Gate voltages (C-V plots) for both TFET and MOSFET. For the Device simulation, B2BT model is used with various metal contact work functions (4.1 – 4.3 eV) and hafnium oxide (HfO_2) as a gate dielectric of thickness 1 nm. Simulation results shows that as the Gate voltage increases, the channel's CB shifts towards the valence band of source and beyond a certain gate voltage, the tunneling of electrons from the VB of source to the CB of the channel [5] takes place and this transport process called as B2BT mechanism which responsible for low SS in TFET

Electron tunneling transmission from source to channel region is given by eqn. (2) [6].

$$T_t = \exp\left(-\frac{4\lambda}{3}\frac{\sqrt{2m^*}}{(h/2\pi)(\Delta\phi + E_g)}(E_g)^{\frac{3}{2}}\right) \quad (2)$$

Where $\Delta\phi$ is the energy range over which B2BT takes place, E_g is energy band gap of the TFET material, m^* is the electron's effective mass, h is Planck's constant and screening length $\boldsymbol{\lambda}$ refers to the spatial extent of the electric field and can be expressed in the terms of the gate oxide dielectric material (ϵ_{ox}), thicknesses of the gatedielectric (t_{ox}), dielectric constant of Si (ϵ_{si}) and thickness of the device (t_{si}), and gate geometry. The screening length ($\boldsymbol{\lambda}$) expressed by the following eqn. (3) [7].

$$\boldsymbol{\lambda} = \sqrt{\frac{\epsilon_{si} \cdot t_{ox} \cdot t_{si}}{2 \cdot \epsilon_{ox}}} \quad (3)$$

It also includes the MOSFET simulation (30 nm) for the comparative study of charge transport and I/C-V characteristics with TFET. Since analytical models for TFET is not available so the optimum method for integrated circuit simulations is to develop a Look up table based model using Verilog-A for both P and N type TFET devices. This model is used to simulate and investigate the static and dynamic behavior of TFET based digital circuits [16-18]. All the Verilog A based simulations are done in Cadence spectre. Cadence simulation results investigated the voltage overshoots for TFET transient responses. Miller capacitance formed at the drain side is the major component responsible for voltage overshoot and can be the result of effective Gate charge coupling to the Drain due to B2BT mechanism in TFET.

II. DEVICE STRUCTURE AND SIMULATION SETUP AND PARAMETERS

Fig.1 shows devices structure of silicon based dual gate TFET $P^+ I N^+$ type. The Hafnium Oxide (HfO_2, ϵ_r= 21) used as a gate dielectric for oxide thickness of 1 nm and the channel length of the device is 30 nm. N type TFET consist of a Source region (P^+) has Boron doping with concentration of $1x10^{20}cm^{-3}$. The drain region (N^+) has Phosphorus doping with= concentration of $1x10^{20}cm^{-3}$. Similarly, for P type TFET consists of Source region (N^+) doped with Phosphorus doping concentration of $1x10^{20}cm^{-3}$ and Drain region (P^+) has Boron doping concentration of $1x10^{20}cm^{-3}$. For both the cases, the channel region is intrinsic with Boron doping concentration of $1x10^{16}cm^{-3}$. The body thickness, $t_{si} = 7nm$ for TFET is used here for device simulation. For MOSFET device simulations, here we have considered the same device structures and dimensions as for TFET with Source and Drain doping of Phosphorus concentration of $1x10^{20}cm^{-3}$and body remains lightly P doped.

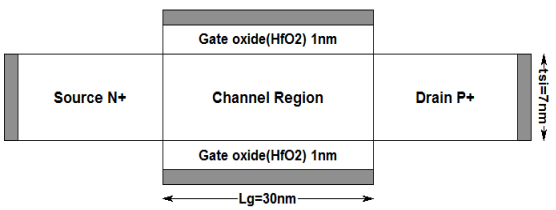

Fig. 1 TFET structure , Lg = 30 nm

All the structures describe in this section are constructed in Sentaurus device editor (SDE) and simulated in 2D. The device structure and physical models coded into the device simulator. The Poisson and carrier continuity equation solved iteratively to yield the transfer and output characteristics of the device shown above. Fermi statistics, non-local tunneling model for TFET and Shockley-Read-Hall (SRH) models used for device simulation to obtain I/C-V and Energy band diagrams etc.

III. CARRIER INJECTION MECHANISM FOR TFET AND MOSFET

In order to understand the operating principle of the TFET, it is necessary to compare with MOSFET. TFETs and MOSFET of dual gate (DG) structures with a Gate length (L_g) of 30 nm, 1 nm thick HfO_2 and body thickness (t_{si}) of 7 nm are simulated to investigate the energy band diagrams, I/C-V and SS. The achieved data is used to generate look up table based model for the circuit simulation using Verilog-A module in cadence spectre [8]. Fig. 2 and Fig. 3 show the simulated energy band diagrams (across the body) for a N-MOSFET and N-TFET. For MOSFET, in OFF state (V_g = 0 V, V_d = 0.75 V), the conduction process in a MOSFET is limited by p-n junction energy barrier across source and the channel which prevents the thermionic emission of charge carriers. In the ON state (V_g = V_d = 0.75 V), the source to channel barrier get lowered and enables the thermionic emission of electrons leads to flow of conduction current.

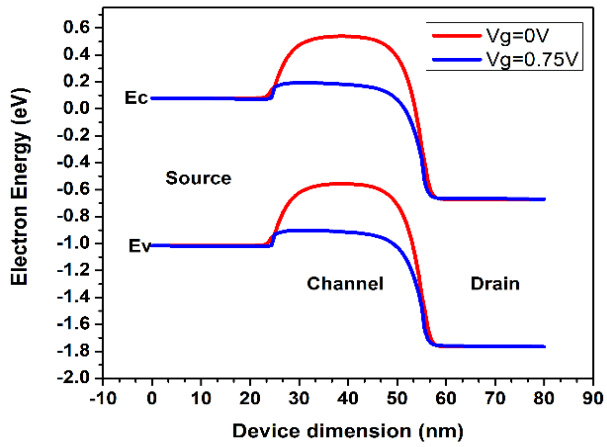

Fig. 2 Energy band diagram for MOSFET (Lg = 30 nm) shows OFF (vg = 0.75 V) and ON state (Vg= 0.75 V)

For TFETs, in OFF state (V_g = 0 V, V_d = 0.75 V), the carrier transmission (see Eqn. 2) is low due to the wide tunnel junction barrier across the source and channel (low electric field) results very low OFF current (I_{OFF} ~ fA). However, in the ON state (Vg = Vd = 0.75 V) the conduction band (CB) in the intrinsic region are pushed down as shown in Fig. 3 and tunneling of electrons takes place between the valence band (VB) of the N+ region and the CB of the intrinsic channel region which leads to flow of current [9]. The energy barrier width for B2BT is the critical factor for determining the amount of Drain current through a Tunnel FET [6][10]. The energy barrier width can be considered as driving factor for I_{ON} in N type TFET. Simulation results show that the drain current increases exponentially with reduction in the barrier width across intrinsic and P+ regions [10].

Retrieval Number: H7236068819/19©BEIESP
DOI:10.35940/ijitee.H7236.078919

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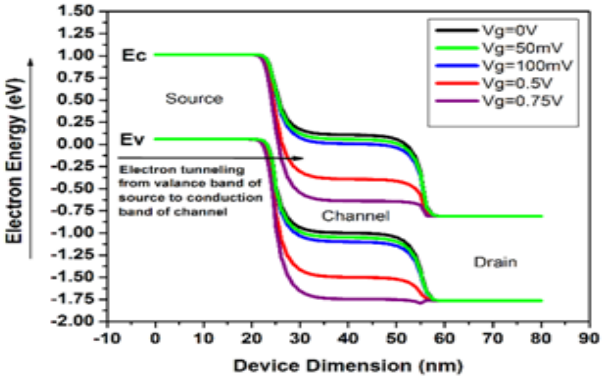

Fig. 3 Energy band diagram of TFET investigating B2BT mechanism

IV. I-C/V SIMULATIONS FOR TFET AND MOSFET

Fig. 4 shows the comparison of Drain current (I_d) vs gate voltage (V_g) characteristics of both TFET and MOSFET. The I-V characteristics for TFET are simulated for different work functions. Let us consider TFET I_d-V_g characteristic for work function = 4.2 eV shown in Fig. 3 to explain its behavior (tunneling current). Here the paper also focuses on drain current arises through tunneling of charge carriers. From the Fig. 2, as the gate voltage increases, the channel's CB energy level shifts downwards. Further increment in Gate voltage, it is observed that the CB of the channel is align with the valence band (VB) energy level for Vg = 100 mV and results to start the B2BT mechanism. Further increase in Vg (100 mV – 750 mV) tend to shift CB of channel below the VB of source and results in lowering of tunneling barrier between the source and channel which increases the more electron's tunneling. The transportation of carriers is responsible for the flow of drain current due to B2BT. Here V_T is defined for the gate voltage (V_g) where the drain current is 100 nA. It is also clearly observed from the Fig. 4 that V_T shifts towards for lower Gate voltages as we increase the Gate metal work function. This is because for the higher gate metal work function, the energy band gap between the
CB of the channel and VB of the source is large. In order to push the CB of the channel towards the VB of source, more gate voltage is needed to enable the tunneling, which results in increases of V_T of the device.

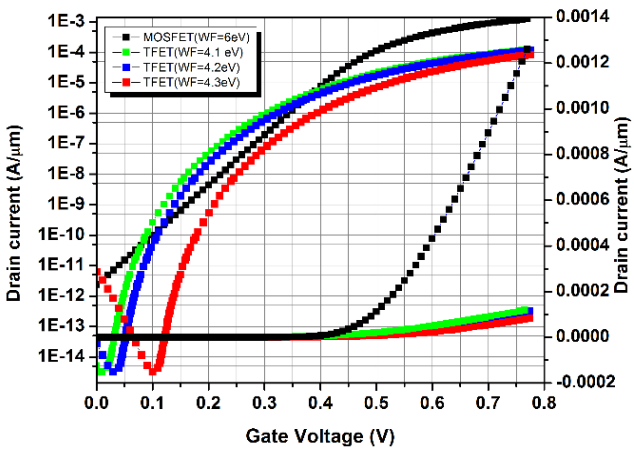

Fig. 4 I-V characteristics of MOSFET and TFET for various gate metal work functions

The small signal AC analysis (1MHz) performed in TCAD is performed to carried out the C-V characteristics for TFET and MOSFET [11]. Fig. 5 shows the C-V characteristics for N MOSFET and it is investigated that Gate to Drain (Cgd) does not follows the Gate capacitances (Cgg) and almost remains constant with very low value (2 fF). It is also observed that gate to source (Cgs) Capacitance is reaching close towards the Cgg for higher gate voltages and these characteristics predict the charge in MOSFET is equally coupled to the source and drain. Cgd and Cgs contributes equal capacitance for Cgg (Cgg = Cgd + Cgs) in linear region ie. Cgd = Cgs. For the saturation region Cgd= 0 and Cgs becomes 2/3 times Cgg.

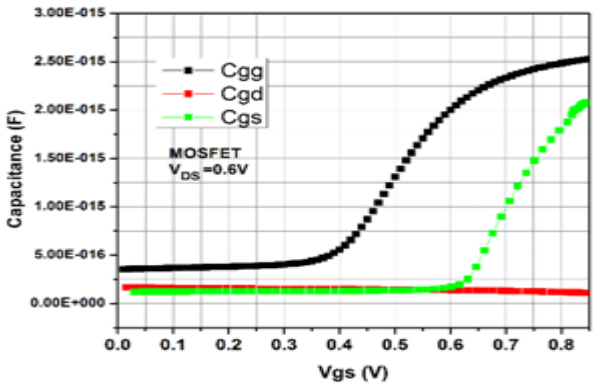

Fig. 5 C-V characteristics for MOSFET

Fig. 6 shows the simulated C-V characteristics of N-TFET. The only motive of these C-V simulations to analyze the effect of Cgd on transient response. The Cgg partitioning in a Tunnel FET is significantly different from MOSFET because of the difference in transport mechanism of the two devices. The source-side barrier limits carrier transport in MOSFET, whereas TFET operates under B2BT mechanism. In MOSFET, the thermionic emission equally couples the charge to source and drain but not in the case of TFET devices. The injection of carriers are carried out by B2BT which effectively decouples the gate charge from the source region due to which the gate charge predominantly coupled to the drain region [12], therefore the Gate – Drain capacitance (Cgd) closely follows the Gate capacitance (Cgg) all over the voltage range (0-0.9 V) as shown in Fig. 6.

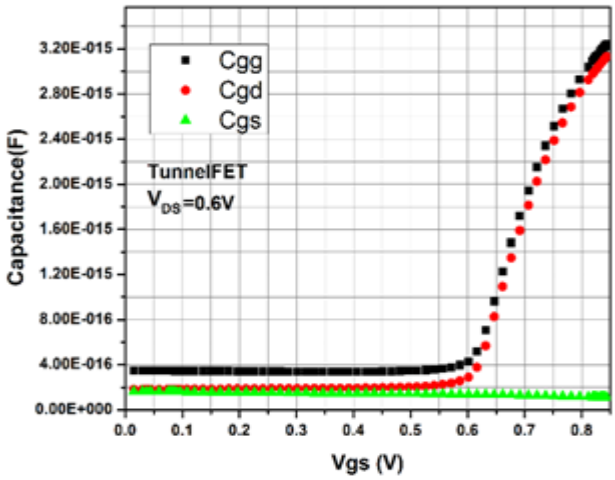

Fig. 6 C-V characteristics for TFET which clearly shows that Cgd strongly follows Cgg.

V. VERILOG-A LOOK UP TABLE BASED MODEL FOR CIRCUIT SIMULATIONS: STATIC AND DYNAMIC RESPONSE.

A lookup table-based Verilog-A model is generated for both N and P type TFET devices. This model is used to simulate static and dynamic behavior of TFET based digital circuits [14].The extracted I-V and C-V characteristics are stored in 2-D look up tables. Verilog-A module is used to build instances, which relates to the look up table for circuit simulations in Cadence Spectre. The only motive to simulate the VTC of the TFET inverter (see Fig. 7) is to validate the look up table based model by comparing the results with benchmark circuits in Purdue Emerging Technology Evaluator (PETE) simulator.

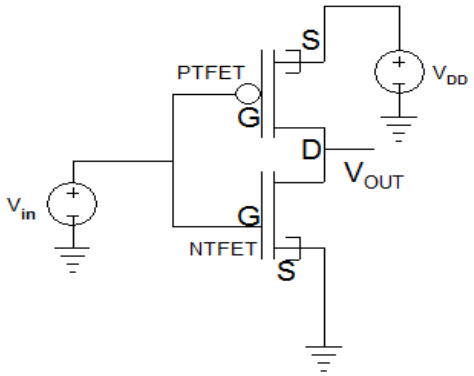

Fig. 7 TFET based Inverter circuit using verilog A in cadence

The most commonly parameters to specify the performance of any inverter is noise margin: low noise margin NML (VOH - VIH) and the high noise margin NMH (VOH - VIH) [15]. Fig. 8 shows the Voltage Transfer Characteristics (VTC) and performance parameters are listed in Table 1. It is clearly observed that Look up table based model is suitable to static simulations of digital circuits.

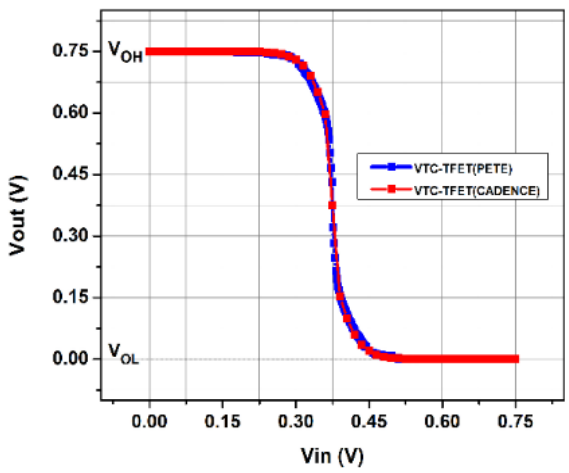

Fig. 8 VTC characteristics of TFET based simulation in Cadence and PETE

Table 1 Simulated VTC parameters for TFET inverter and validation

Parameters	TFET (PETE)	TFET (CADENCE)
VOH	0.75 V	0.75 V
VOL	0 V	0 V
Gain (at VM = 0375V)	16	14.84
VIL	0.31 V	0.30 V
VIH	0.44 V	0.435 V
NMH (VDD - VIH)	0.31 V	0.315 V
NML (VIL)	0.31 V	0.30 V

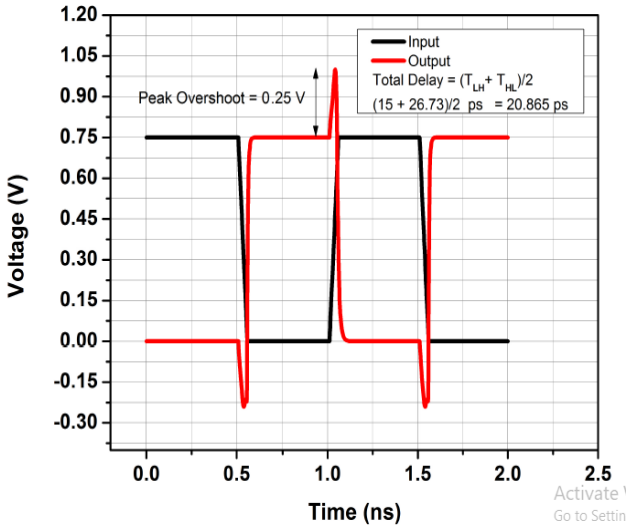

Fig. 9 Transient response of TFET inverter and shows voltage overshoots due to miller effect at drain side

The simulated transient characteristics of a TFET Inverter are shown in Fig. 9, the positive and negative voltage overshoots of 0.25 V are observed in this case. These voltage overshoots can be attributed to higher Cgd as compared to Cgs ie. Cgd follows the Cgg for the higher Gate voltage (0.6 – 0.9 V). Cgd in a TFET inverter is the driven parameter which causes feedback of the transient signal from the output (Drain node) towards the input (Gate node) called as Miller Effect. This can be understand as the input rises and output falls and at the same instant Cgd couples back a magnitude of output transient response to the input node , thus slows the input rising waveform. These voltage overshoots clearly have a negative impact on the performance of the inverter as it may lead to high dynamic power loss and large turn-on/off delay for digital circuits.

VI. CONCLUSION

The carrier transport phenonomenan in MOSFET and TFET is different and one is limited by hot electrons and latter is limited by Band to band tunneling of electrons. B2BT offers the low value of I_{OFF} and steep SS at lower gate voltages.It is investigated that charge in channel and drain regions in the Si TFET is directly coupled to each other due to B2BT tunneling between source and channel. Coupling of the charge leads to follow the Cgd with Cgg, therefore responsibe for miller effect at the Drain node in TFET inverter and results in volatge overshoots during the transient response which increses the turn on/off delay in the digital circuits. Look table based model with Verilog-A shows the promising results for static and dynamic simulations of the TFET based digital circuits.

Retrieval Number: H7236068819/19©BEIESP
DOI:10.35940/ijitee.H7236.078919

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