A Layout Technique To Reduce The Impact Of Parasitic Capacitors Within A Capacitor Array On The Nonlinearity Of Data Converters.

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Abstract*: —** ***SAR ADC has a moderate speed, Low area and low cost compared to other ADC implementations. The accuracy expected from a commercial SAR ADC is very high and research has been going on for many years to improve the accuracy. The Linearity of the data converters is the key for accuracy. The Integral nonlinearity and differential nonlinearity errors of data converters are governed by the matching of the unit capacitors/resistors with in capacitor/resistor array. Layout of these arrays can add significant parasitics affecting the nonlinearity of data converters. This paper presents a layout technique to reduce the impact of the parastics on data converter's nonlinearity.

***Index Terms*:**

I. INTRODUCTION

Signal processing these days typically happen in digital domain. The data converters convert the real word analog signal in to digital output. To preserve the quality of the signal there is a demand for converters of high resolution.

Successive approximation register ADC is one of the most popular architecture of data converter. The architecture of conventional N-bit SAR ADC is as shown in Fig. 1. The blocks include sample-and-hold circuit, a comparator, a N-bit capacitive digital-to-analog converter (DAC) array and a SAR control logic, where N is the resolution of the ADC [4]. In this paper we will discuss about layout of a cap array in a 8bit/10bit SAR ADC. The architecture of the DAC used for study is a hybrid one, where in first four MSB are determined by resistor array and latter six/four LSB are determined by capacitor array.

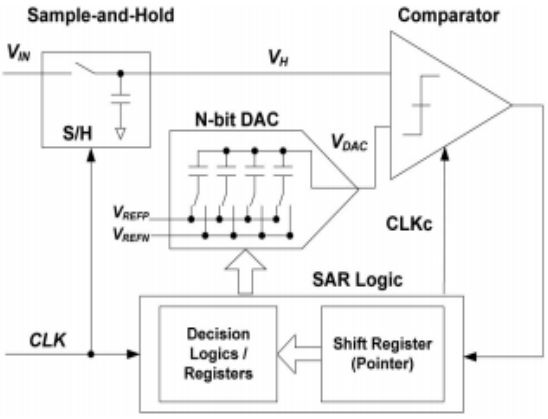

Fig 1. Block diagram of N bit SAR ADC

The schematic of the capacitor array is shown in the Fig2. The capacitor array is binary weighted with each branch having capacitor values of C, 2C, 4C, 8C, 16C, 32C. For better matching the unit capacitor of value C is chosen and the array of 64 is built as shown Fig3 satisfying the common centroid criteria [2] [3]. The minimum size of unit cap C is chosen based on random matching criteria. For our design the value of unit cap comes to 100f (2.5u by 2.5u). So the Cap array is small (40u by 40u). The top and bottom plates of the unit capacitors have to connected and brought out to the periphery of the capacitor array. These routes will have to travel a long distance and can contribute to significant parastics affecting nonlinearity of the data converter. This paper addresses this problem.

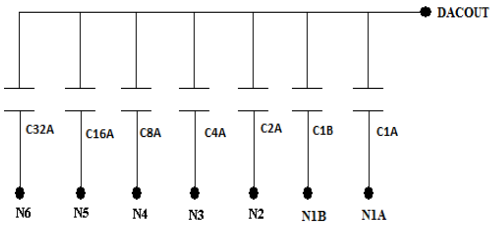

Fig 2. Schematic of the 8bit capacitor array

Revised Manuscript Received on July 05, 2019

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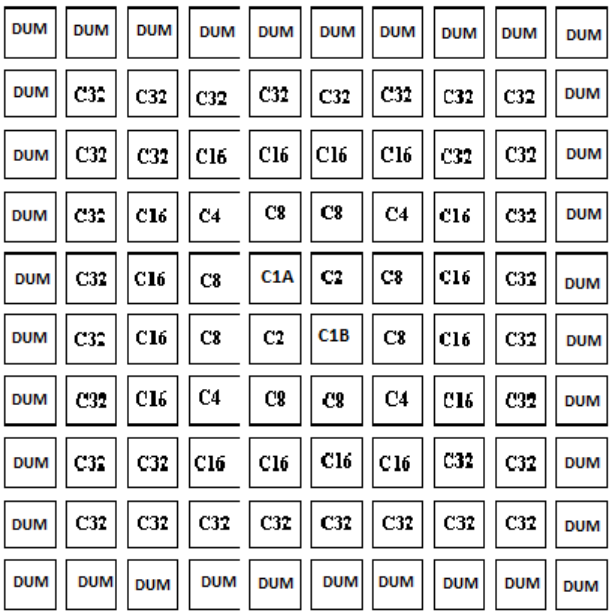

Fig 3. Placement of unit caps within capacitor array

II. PROBLEM AND SCOPE OF THE WORK

The Linearity and the accuracy of the ADC is mainly dependent on the capacitor DAC array matching characteristics, with increase in the resolution of the data converters the maintenance of the accurate capacitor value poses big challenge [6]. The mismatch in the layout can be classified as systematic mismatch and random mismatch. Systematic mismatch is caused by identical devices with asymmetric environment and random mismatch is caused by variation in the processing conditions [3]. In this paper the mismatch and its effect on the linearity of the data converters. The unit capacitor elements are Fence metal caps. The structure is shown in the Fig 4. The top and bottom plates form a comb structure. Metals are stacked to increase the capacitance between top and bottom plate [2] [8]. In this case we have used MoM (Metal-Oxide-Metal) capacitors. The oxide acts as the dielectric material. Fig 5 shows the layout of the capacitor array with bottom plates highlighted. Fig 6 highlights the top plate route (in yellow). The routes, the top and the bottom plates form individual parasitic caps. Apart from the parasitic capacitance formed by the unit capacitor the routing capacitance also plays critical role and hence there is a scope for improvement. Understanding the importance of parasitic capacitance formed helps in analyzing the effects on the performance of the DAC [7]. Let the capacitance formed between top plate and bottom plate be C1, this is the main intended capacitance; the capacitance formed between bottom plate and substrate be C2; and top plate to substrate as C3as shown in Fig 7. Since the top plate of the capacitor is connected to DAC OUT, any additional parasitic capacitance between top plate and substrate would induce mismatch. The basic criteria is to have zero parasitic mismatches from top plate to bottom plate across the array; minimal parasitic from top plate to substrate and some tolerance for bottom plate to substrate.

The effect of these parasitic capacitors on the INL/DNL (in LSBs) of the 6bit Capacitor array is shown in the Fig8. The parasitic routes cause an INL error of 0.4LSBs and DNL error of 0.7 LSB's. In Addition the bottom plate and top plate routes which are brought to periphery will add addition parasitic on individual nodes. The challenge is to have equal and minimal parasitic on all the nodes and nullify the routing effects.

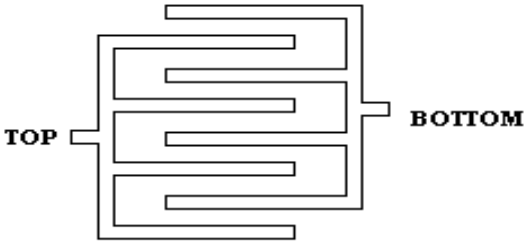

Fig 4. Unit capacitor structure

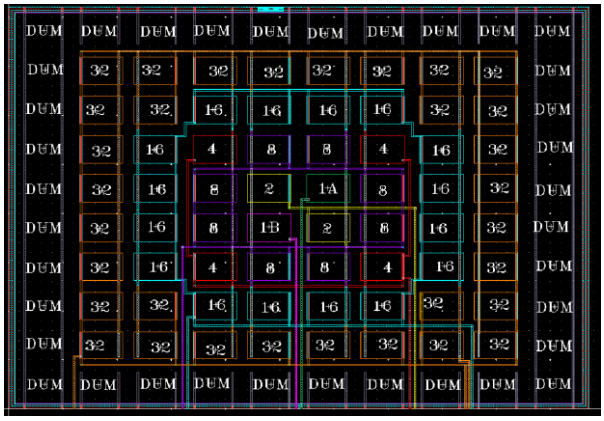

Fig 5. Layout of capacitor array

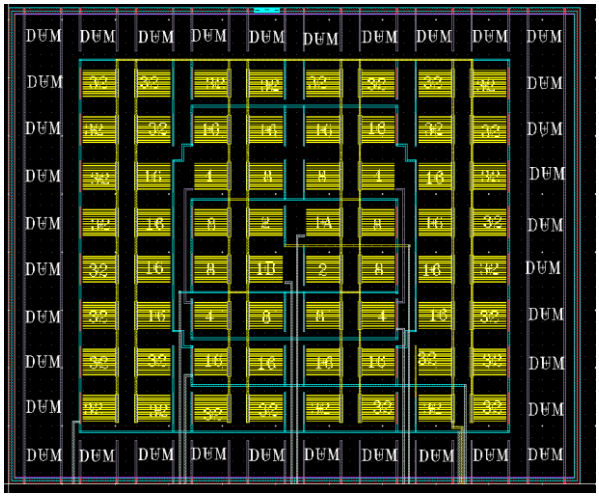

Fig 6. Yellow line highlights top plate routes.

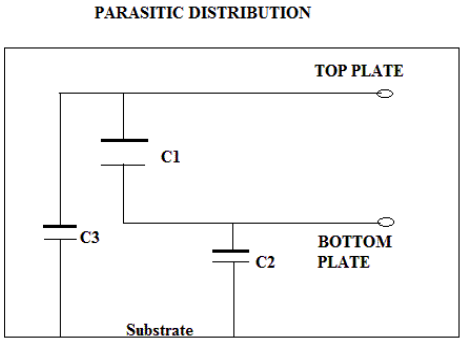

Fig 7. The Parasitic distibution.

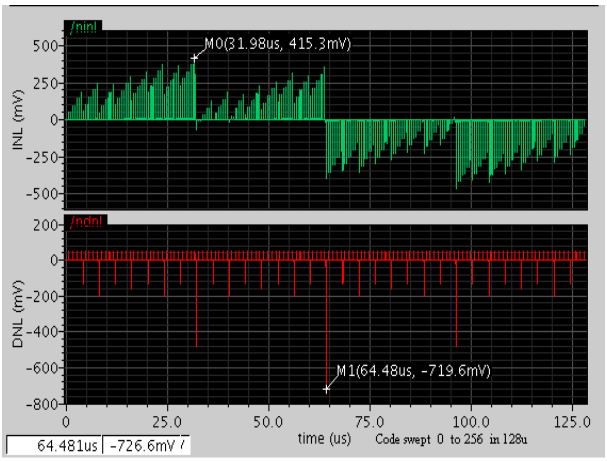

Fig 8. INL/DNL error (in LSBs) due to parasitic capacitors

III. METHODS

The binary weighted capacitor array brings in the design comfort on unit capacitor parasitic effect. The parasitic capacitors along with the actual capacitors will also be binary weighted. In simple terms the parasitic capacitor effects the unit capacitor value and the value of capacitor deviates from its actual intended value.If the unit capacitor is C0 then the attenuated capacitor C0' is defined as **C0'=C0+ C.** Where C is change in the parasitic capacitance parallel to array capacitor. Apart from the direct parasitic effect various other effects such as the second-order lithographic errors, the proximity effects, the symmetry and the complexity of the wiring, and the far range fringing field effects also play important role. In today's sub nanometer technologies the parasitics induced due to interconnect routings have reached the order of couple of fF on the other hand the scaling of devices have reduced the unit capacitance in the DAC array to few fF. Various placement techniques are used to nullify the systematic mismatches; the matrix-adjustment method is used to achieve a more symmetrical structure for any binary-weighted capacitive array; thus minimizing the first-order process gradient effects. The capacitive array is surrounded by the dummy unit capacitors; which act as adjacent structures in order to suppress the second-order lithographic errors and the proximity effects. The placement of the remaining dummy capacitors is done according to the space availability. All of these technique doesn't deal with secondary effects of parasitic capacitance on the performance of the DAC. This paper clearly classifies the different parasitic capacitances formed with respect to both the plates of the capacitor and shows the shield method to nullify the effects of the same.

IV. SOLUTION

Ideally the parasitic cap C1 should be equal for all binary weighted caps, but the parasitic formed from the bottom plate routings which are brought to the periphery will add addition caps. Since the cap array is binary weighted; the overall mismatch grows from C1A to C32A. Similarly the parasitic cap C3 from top plate to substrate is formed because of the unit cap's comb structure.

The proposed solution brings in the idea of shielding the unit capacitor using the bottom plate. The unit capacitor uses the lowest metal to act as the shield for the top plate. The proposed capacitor structure is as shown in fig. 9. By this arrangement the top signal is restricted to the environment where it forms cap only with bottom plate. This structure brings in additional cap between top plate and bottom plate (C1) and thereby increasing the unit capacitance value. Since the DAC cap array is a binary weighted arrangement, any increase in the unit capacitance value increase the capacitance of all the units in the same fashion. Thus the primary effect of the new structure is nullified across the CAP DAC. The shield structure also avoids the parasitic capacitance from top plate to substrate (C3), but this will increase the capacitance between bottom plate and substrate (C2).

The parasitic capacitors C1 and C3 have direct impact on the linearity of the capacitor array as they directly affect the capacitor value of the array, whereas C2 capacitors affect only the speed of operations. In this case mismatch of (+/-) 0.01% is achieved. As seen in Fig 5 and Fig 6; the unit capacitors of two adjacent rows are flipped such that top plates align. There by avoiding the parasitic cap between internode bottom plate capacitance and top plate. The top plate routing is done in those channels where it sees only top plate on either side. Similarly bottom plate routing is done in the other channel where bottom plates align. The same is done horizontally also. The routes highlighted in yellow (Fig 6) are the top plate route. We see alternate channels dedicated for top and bottom plate routes. Hence nowhere top plate and bottom plate routes are running in parallel. This way interaction between top and bottom plate routes has been significantly reduced. The integral nonlinearity error with the new layout is shown in Fig 9.

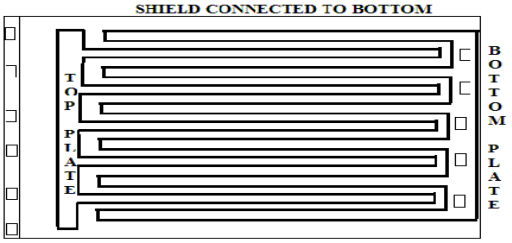

Fig 9. Unit Cap Arrangement.

V. RESULTS

Fig 8, shows the INL/DNL error of .41/.72 LSB with regular cap arrangements and Fig 10 shows the INL/DNL error of 0.03/0.06 LSB with the proposed cap modifications and arrangement. We see the new layout has significant improvement in the INL/DNL error. The INL/DNL errors have come down from 0.41/0.72 LSB to 0.03/0.06 LSB with the modified layout.

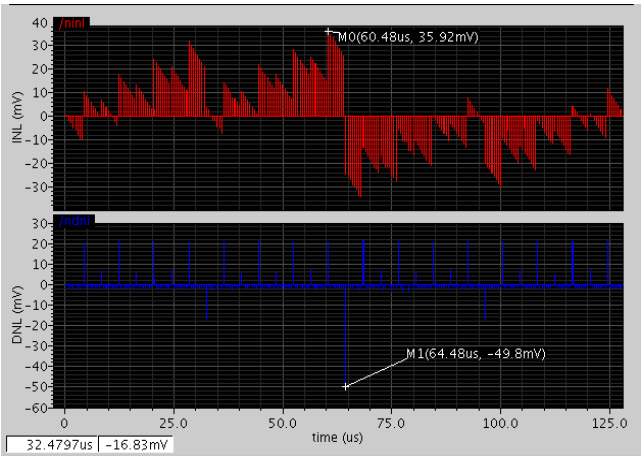

Fig 10. The INL/DNL error with the new cap array routings

VI. CONCLUSION

The result shows that, it is important to achieve a zero mean offset or zero systematic mismatch which are placement driven in the binary-weighted capacitive array as random mismatch which is process dependent cannot be totally eliminated. The result shows apart from the placement the unit capacitor structure played important role in nullifying systematic mismatches. The symmetrical and common-centroid placement for the capacitive array helps in nullifying the first-order oxide gradient. Additional dummy unit capacitors are placed adjacent to the capacitive array to reduce the proximity effects and second-order lithographic errors. The capacitor array placement resembles a star-like arrangement so that it simplifies the wiring scheme and minimizes the number of asymmetrical wiring compared to existing works.

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