Design of Low Power Amplifier for Brain Signal Measurement Applications

Navdeep Kaur, Neelam Rup Prakash

Abstract: This paper presents the idea of analog amplifier which amplifies the amplitude of the real time EEG signals. This amplifier is for the front end application in brain signal measurement applications. In this paper instrumentation amplifier has been used for the designing purpose. The parameters of the proposed amplifier have been analyzed in order to achieve better gain and less power dissipation. The parameters like voltage, slew rate, gain bandwidth product, and sizing of Mosfet have been analyzed to achieve high gain using Cadence Virtuoso Software.

Index Terms: EEG, opamp, instrumentation amplifier.

I.   INTRODUCTION

The EEG is a measurement of the electrical activity of the brain from scalp. The measured waves show the cortical activity of the brain. The amplitude of EEG signal is very small, measured in microvolts. The desired EEG signal falls into four frequency bands: Delta($0.5 \leq f < 4$ Hz), Theta($4 \leq f < 8$ Hz), Alpha($8 \leq f \leq 13$ Hz) and Beta($f > 13$Hz). But the power line interference 50/60 Hz artifact, patient related artifacts (e.g. movement, sweating, eye movements etc.) and technical artifacts (e.g. cable movements, electrode paste related) affect the accuracy of the EEG signals. Therefore, amplifier is designed in order to amplify the amplitude of the real time EEG signals. The designing of amplifier has been done on cadence virtuoso tool in order to amplify the EEG signals. The idea of research is to design an instrumentation amplifier with less power dissipation and high gain for amplification of EEG signal in front end. To reach this goal it is required to optimize parameters of instrumentation amplifier. Parameters like voltage, slew rate, gain bandwidth product, and sizing of MOSFET have been used to optimize the result and to determine the better output.

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A. Signal Acquisition and amplification: The most important block of signal conditioner is the pre-amplification stage. Since EEG is the potential difference between two different leads; the solution would be to use differential amplifier. To increase input impedance, two voltage followers are placed at the input as shown in figure 1.
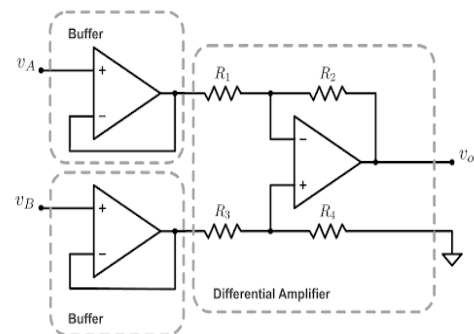

Figure 1: Instrumentation amplifier [2].

II.   METHODOLOGY

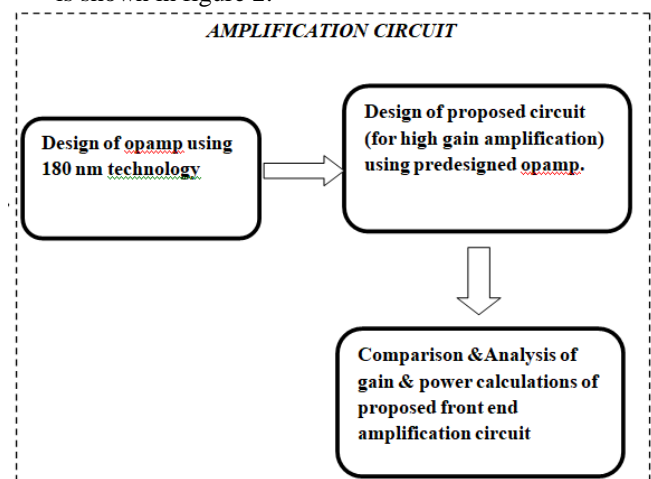The work flow of the proposed instrumentation amplifier is shown in figure 2.

Figure 2: **Work Flow of Amplifier Design.**

Step I: The first step is to design a two stage operational amplifier (opamp) using 180nm technology. This technology needs a power supply of 1.8 V for its operation which leads to less power dissipation in the circuit. The two stages of opamp is used to increase the overall gain of the opamp so that it would amplify low voltage EEG signals [3].

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Step II: The second step is to design a proposed circuit of instrumentation amplifier using predesigned two stage opamp. In this proposed design voltage buffers are used to increase the input impedance and to isolate the circuit so that there will be a less interference in between the signals. The combination of resistors is used in this amplifier to increase the overall gain.

Step III: The third step is to compare and analyze the gain and power values of opamp and the proposed instrumentation amplifier for EEG signals.

A. Advantages of instrumentation amplifier:

The design of the amplifier for EEG signal consists of an instrumentation amplifier as shown in figure 3. The EEG signal measured from the electrode is very small in magnitude and contains lots of noise. It is necessary to amplify the weak signal and filter out the noise present in the signal. The following reason describes the usage of instrumentation amplifier [4].

a) High gain.
b) High common-mode rejection ratio (CMRR)
c) High input impedance.
d) High common-mode extraction.

The gain requirement can be increased by using two stage operational amplifiers and it provides the necessary gain for amplification of EEG signals. The instrumentation amplifier boosts CMRR. The instrumentation amplifier offers excellent accuracy and more flexibility. The flexible 3-opamp design and small size allows us to use in wide range of application.
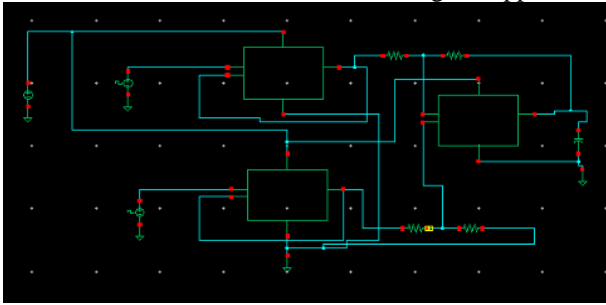

Figure 3: Circuit diagram of instrumentation amplifier

B. Design of operational amplifier:

The operational amplifier is the basic block of an instrumentation amplifier used in the EEG amplifier. The operational amplifier design was implemented as long tailed pairs with current mirror circuit as shown in figure 4.To reduce the flicker noise, we should increase the $W\!/\!L$ ratio of input transistors in the first stage of the amplifier. The device matching in the second stage of the amplifier does not provide any change in the noise performance.
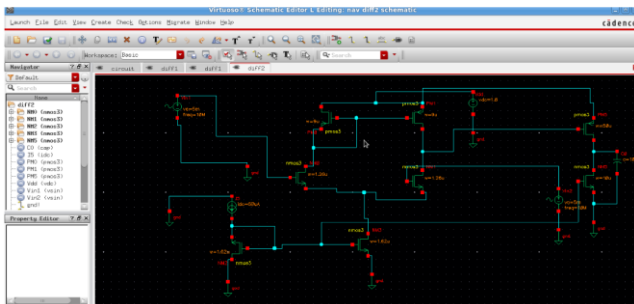

Figure 4: Schematic view of two stage operational amplifier

C. Performance Analysis of operational amplifier:

The overall differential gain of the amplifier is given by

$$A_{total} = A_{Ist\ stage} + A_{2nd\ stage} \qquad (1)$$

Normally, the gain the amplifier is given by output voltage divided by the input voltage.

Gain of the first stage of opmp= $g_{m1}/g_{ds1}+g_{ds4}$ (2)

Gain of the second stage of opmp= $g_{m6}/g_{ds6}+g_{ds7}$ (3)

After running DC analysis of two stage operational amplifier on cadence virtuoso the results of parameters of MOSFET are as:

Parameters of MOSFET	Values
g_{m1}	169.156u
g_{ds1}	8.50749u
g_{ds4}	4.03979u
g_{m6}	1.684m
g_{ds6}	37.3384u
g_{ds7}	32.1812u

where g_m is transconductance of MOSFET and g_{ds} is drain to source transconductance of MOSFET.

Gain of first stage of opamp=45.18 dB
Gain of second stage stage of opamp=27.68 dB
Total gain of operational amplifier = 72.86 dB

III. SIMULATION AND ANALYSIS

The schematic diagram of the proposed instrumentation amplifier consists of voltage buffers to increase the input impedance and to isolate the circuit so that there will be a less interference in between the signals. The combination of resistors is used in this amplifier to increase the overall gain. The instrumentation amplifier consist of opamp built with 180nm technology so that there will be less power consumption in the circuit. Each of the input of the instrumentation amplifier in ideal circuitry is connected to the electrode which measures the value of the voltage from the scalp.

The AC analysis of the two stage opamp using cadence spectre simulator is shown in the following figure 5.
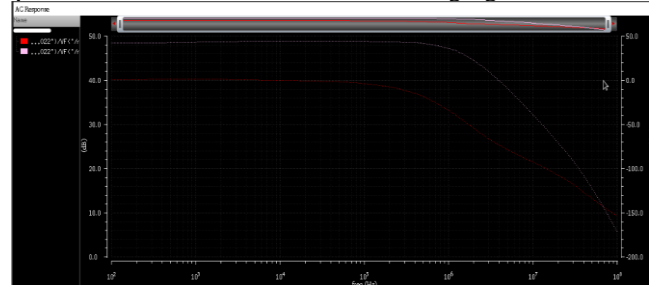

Figure 5: AC analysis of two stage operational amplifier at 180nm technologyThe transient response of the instrumentation amplifier is shown in the figure 6. In this figure the difference between the two inputs is amplified which is almost negligible. Hence the proposed circuit can be used for the front end EEG amplification as this amplifier can amplify the smallest possible difference

between the two electrodes which are connected to the scalp of the patient. The signals then further send to filtration circuit for the proper analysis of EEG bands.

Figure 6: Transient analysis of proposed instrumentation amplifier

Table 1: Comparison of results

Sn o	Parameters	Results of proposed circuit	Results of [1]
1.	Technology	180nm	180nm
2.	Supply voltage	1.8V	1.8V
3.	Maximum voltage at non inverting terminal (+)	1.6V	-
4.	Minimum voltage at inverting terminal (-)	0.8V	-
5.	Gain	72db	60db
6.	Power dissipation of opamp	246µW	-
7.	Overall power dissipation	384µW	980µW

IV. CONCLUSION

In this paper the proposed instrumentation amplifier which consists of two stage operational amplifier designed at 180nm technology provides a gain of 72dB for amplification of EEG signals. The proposed design is of low power technology as it needs only 1.8V power supply. The proposed design amplifies the smallest possible voltage difference between the two electrodes of the amplifier as seen from the transient analysis of the amplifier which is desired for brain signal amplification.

REFERENCES

1. Cortes, F.P., Fabris, E. and Bampi, S., "Analysis and design of amplifiers and comparators in CMOS 0.35 µm technology", *Microelectronics Reliability*, 2004, 44(4), pp.657-664.
2. Geiger, R.L. and Sanchez-Sinencio, E., "Active filter design using operational transconductance amplifiers", *IEEE Circuits and Devices Magazine*, 1985, 1(2), pp.20-32.
3. Kumar, S.P., Chandrasekar, A., Nagaraj, A., Gupta, P. and Sekhar, S., "Design of an Electroencephalogram (EEG) amplification circuit for neonates", *International Conference on Communication and Signal Processing (ICCSP)* , 2016,(pp. 2069-2072). IEEE.
4. Moni, D.J. and Gopalakrishnan, N.," A Low Power CMOS Electrocardiogram Amplifier Design Using 0.18 µm CMOS TECHNOLOGY" , *International Journal of Advancements in Research & Technology,* 2013, 2(2).
5. Pu, X.J., Liu, T.J. and Yao, D.Z., "Design of an EEG preamplifier for brain-computer interface , *Journal of Electronic Science and Technology*,2009, 7(1), pp.56-60.
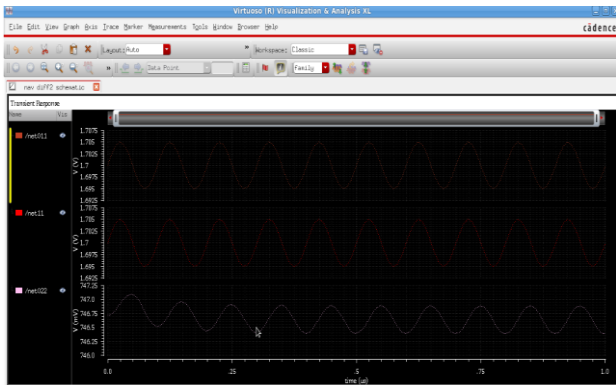
AUTHORS PROFILE

Navdeep Kaur received her B.E. degree in Electronics &Communication Engineering from University Institute of Engineering & Technology, Chandigarh in 2017.She is currently pursuing her MTech in Electronics (VLSI-DESIGN) from Punjab Engineering College (Deemed To Be University) Chandigarh. Her current research work includes CMOS amplifiers for biomedical application and design of digital filters for real time biomedical signals.

Neelam Rup Prakash has a vast experience in both Industry and Academia for nearly 32 years. She has headed the Electronics & Communication Engineering Department at Punjab Engineering College (Deemed to Be University), Chandigarh. She started a new Postgraduate Program in VLSI Design in the Department during her tenure as HOD. Her area of research includes Digital Design, Low Power VLSI Circuit Design, Computer Aided Diagnostics and has a number of publications in journals of repute. She is the Co-ordinator of the Centre of Excellence in Industrial and Product Design. She has guided over 50 MTech and PhD students. She is a member of various forums like IEEE, IETE, etc. She has a number of patents to her credit.