Design and Implementation of Embedded Audio System based on Zynq-SOC

Ananth Kumar Vissampalli, Rani Rudrama Kodali

Abstract*: Nowadays smart world requires, Embedded audio system with optimum design metrics for smart applications in various fields like smart car, intelligent systems and Robotics etc. This paper describes the Design and implementation of embedded Audio system for real-time applications on SOC-FPGA with optimized design metrics (low power, low-cost, low development time, low area, high speed). An electret microphone / line in are used to feed the audio input. An audio codec from Analog devices named ADAU1761 which is integrated on the zynq-7020 board. In the proposed embedded audio system, the block design in Vivado2017.2 has been modeled with VHDL; application software developed using C language in SDK2017.2. This Audio system is the optimized solution for a wide range of smart applications.

Index Terms: ADAU1761 codec, Electret microphone, embedded audio system, Zynq 7020-SOC.

I. INTRODUCTION

The system which has optimized design metrics will gives the better results than the ordinary system. Optimization of the design includes the parameters like speed, area and time required for the design. The design area reduction increases the speed of the system. The reduction of the design area is achieved by decreasing the size of the components used in the design. There are some reconfigurable devices like FPGAs which are not having any processing system but having only programmable logic space. By using these types of devices, a separate processing system is required to process the logic stored in the programmable logic and it requires a large area. Then the term miniaturization comes in to picture. A device which has a processing system along with the programmable logic gives a solution for the minimization of the design area. As the processing system and programmable logic are integrated on the same chip it is called as system on chip (SOC). As the name embedded audio system, it is the combination of hardware and software. Miniaturized PC, Microphone and speakers will make it possible to design compact embedded audio system for a particular application. This audio system can able to hear and record the audio frequencies which are not heard by human beings. The computing platform is the key design metric to design audio system. Many solutions are provided based on general purpose processors (GPP), Digital signal processors (DSP), Reconfigurable devices (Field Programmable Gate Array) FPGA [1]. This proposed system is designed by using ZYNQ-7000SOC-FPGA. It is an all programmable SOC to combine both hardware and software in to single device, and provides high performance, flexibility, scalability, low power. Zedboard has Processing System (PS) [2] and Programmable Logic (PL) [3]. Dual-core ARM CORTEX A9 is the Processing system which operates at 1 GHZ. Artix-7 FPGA is the Programmable Logic having reconfigurable resources like 140 BRAMs, 13,300-logic slices, DSP48E1s-220, XADC hard IP block used for hardware functionality. The advanced extensible interface (AXI) is used to interface processing system and programmable logic. AXI belongs to third generation of advanced microcontroller bus architecture and is used for high-speed interconnect.

Vivado was developed for high-speed FPGAs. It is an IDE(Integrated Development Environment) used to create block design of hardware and for interacting with integrating and packaging IP which results re-usage of design.SDK(Software Development Kit) is for driver support of GCC library in c/c++ languages, Xilinx IP's.

The aim of this work is to design an embedded audio system which has low power, low area, less development time and has high performance. The Zedboard is a low cost development board from AVNET-ZYNQ 7000 family [4]. An electret microphone [5] is connected to microphone jack of the audio codec on Zedboard. A headset is connected to headphone out/line out jack.

II. PROCEDURE

The design tools and hardware requirements for proposed design are Zedboard (XC7Z020clg484-1), Vivado2017.2, Xilinx SDK 2017.2 on windows operating system, an electret microphone, 3.5mm audio cable. The hardware block design was created using Vivado 2017.2 and generated a bitstream (.bit) file. By generating bitstream a hardware description file also generated and is used to define the hardware. Exporting hardware and launching Xilinx SDK will make space within the project to create an application. A new application will be created to define hardware functionality. Xilinx SDK will automatically generate a board support package which has the required drivers and libraries for the application. Configuration of the project facilitates the altering of the system behavior by defining the audio script in the application project. After configuration of the project the project will be able to work on the targeted hardware (Zedboard).

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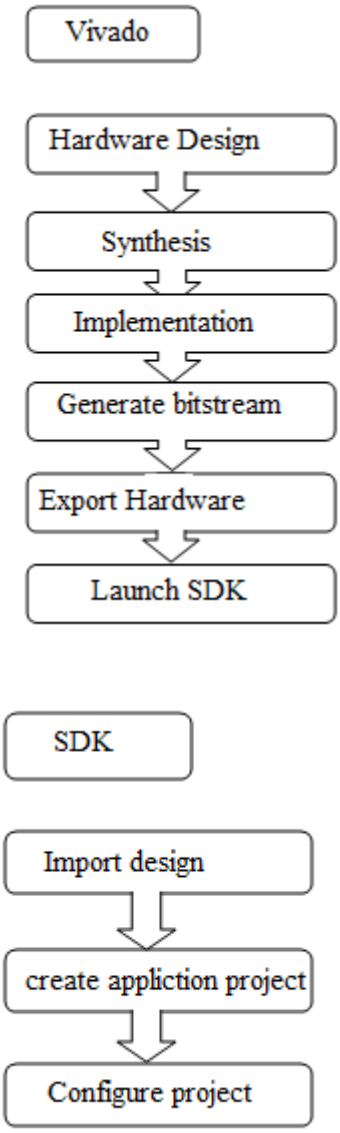

Fig.1.Design Methodolody for Proposed System

III. ZYNQ ARCHITECTURE

Zynq-7000 Is An All Programmable System-On-Chip Architecture. All The Resources In It Are Programmable. Software, Hardware, I/O Pins Are Included In Single Chip And Is Termed As System-On-Chip [6]. Zynq-7000 Is Termed As Processor-Centric Platform, Because It Has Processing System (A Dual Core ARM Cortex-A9) And Programmable Logic (FPGA Based) On Single Board. Different Types Of Designs Are Available For SOC-Fpgas To Develop Different Smart Applications. Zynq-7000 Is Based On 28nm Technology.

The Fig2 Depicts The Architecture Of Zynq-7000 SOC. It Enables The Implementation Of Design Logic In PL And Runs Application Software In PS. The Processing System ARM CORTEX-A9 Will Support The Linux Operating System And It Can Support Some Other Operating Systems. It Has A Hard Core Processor (ARM Cortex-A9) In Processing System (PS) And A Soft Core Processor (Microblaze) In Programmable Logic (PL). These Types Of FPGA Soft Core Processors are most useful for reducing the design time.

The Programmable Logic (PL) and Processing System (PS) in Zynq-7000 SOC have dedicated power domains. The power domain for PL will be disabled if required. The Processing System (PS) ARM cortex-A9 will always boot first and then PL will boot and functions as the application software defined. An Application Processing Unit (APU), memory interfaces, I/O peripherals (IOP), interconnects are in built within the PS [7]. APU consists of two ARM processing units each one having dedicated computational unit, a NEON media processing engine (MPE), floating point unit (FPU), memory management unit (MMU). Memory management unit has two levels of cache memory which are level 1 and level 2. Level 1 has (32kb+32kb) in two sections for instruction and data storing. Level 2 has (512kb) cache and on-chip memory (256kb). A snoop control unit (SCU) forms connections between on-chip memories and ARM cores.

The processing system has different operating modes. (1) Only one core will process the operation while the second core is in standby mode. (2) Both cores will be turned on and work as symmetric or asymmetric. If both cores are operated using single operating system it comes under symmetric mode. If each core is operated by individual operating system it comes under asymmetric mode. Zynq PS has secure mode operation which is called as trust zone technology. Memory interface unit consists of dynamic and static memory controllers. The communication between IO peripherals and external devices is done through 54 multiuse's I/O (MIO) pins in Zedboard. These pins are used to establish services like GPIO, SPI, UART, TIMER, ETHERNET, and USB. Zynq has two high performance interfaces between ARM cortex-A9 and Artix-7 for data transmission. The data transmission between processing system and programmable logic is through AXI ports.

Programmable Logic (PL) has Control Logic Block (CLB) which is divided in to two logic slices. Each slice consists of 4 Look-Up-Tables, Flip-flops and other logic. A single LUT may capable to implement logic for up to 6 inputs, small ROM, RAM, a shift register and PL has resources DSP48E1S used for high speed arithmetic and Block RAM (BRAM) used for dense memory requirements.

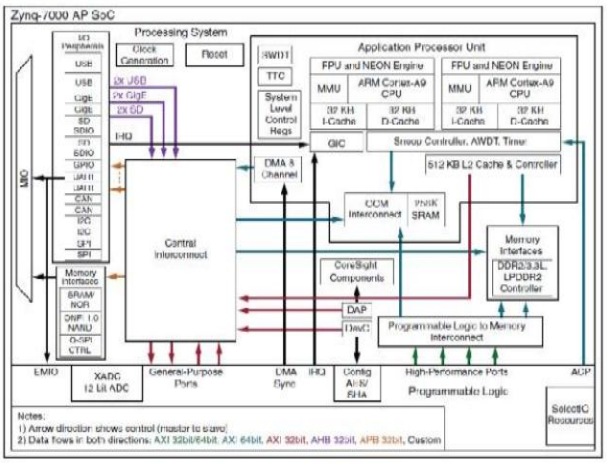

Fig.2.ZYNQ Architecture

IV. ADAU1761 CODEC

The embedded audio system comprises of hardware and software. The main hardware role is played by the audio codec which encode and decode the audio signals. The audio codec used for this work is ADAU1761 [8] from Sigma DSP is a low power, stereo with integrated digital audio processing which supports 48khz record and playback at 14 mW from 1.8v analog supply.

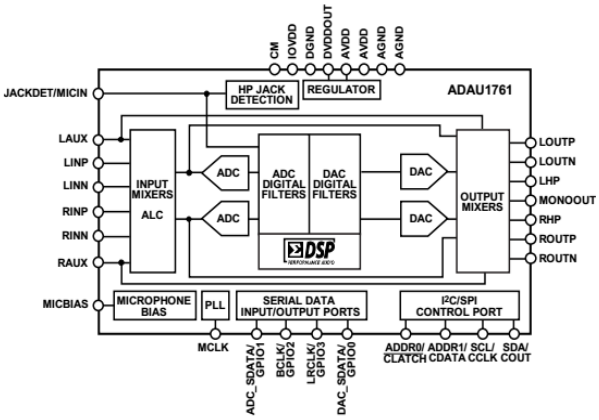

Fig.3.Functional diagram of adau1761 codec

The sample rate supported by the stereo ADCs and DACs is from 8 kHz to 96 kHz and also used it as digital volume control. It has features include 6 analog input pins, flexible analog input/output mixers, PLL supporting input clocks from 8 MHZ to 27 MHZ, Analog automatic level control (ALC), IIC and SPI control interfaces. A functional diagram for ADAU1761 is shown in the figure 3.

The functional description of the ADAU1761 gives the working of the audio codec. Input is applied at input mixers through the input channels LAUX, LINP, LINN, RINP, RINN, and RAUX. An Automatic Level Control (ALC) in integrated within the input mixers. It is used to continuously adjust the gain to keep the recording volume constant as the input recording volume level varies. SERIAL DATA INPUT/OUTPUT PORTS are used to receive/transmit the data in a serial order. It has different clocks like BCLK, LRCLK for providing different clock frequencies for the transmission of the data between hardware. ADAU1761 has two types of control modes and it is operated in one of the two modes. The two control modes are IIC control and SPI control. This codec has an inbuilt regulator with different modes (CM, IOVDD, DGND, DVDDOUT, AVDD and AGND) to provide different voltages as per the requirement of the power supply for ADC, output driver. The applied input signal fed to digital filters through analog to digital converters (ADC). Then the digital signal is again converted to analog by using digital to analog converters (DAC) and fed to output mixer through DACs.

At the output mixers output channels LOUTP, LOUTN, LHP, MONOOUT, RHP, ROUTP and ROUTN are used to connect the output load. MICROPHONE BIAS is a voltage for Electret Microphone. PLL uses the MCLK as a reference to generate the core clock frequency.PLL has different operating modes such as Integer mode and Fractional mode. Pin configuration of the ADAU1761 is shown in the figure 4.

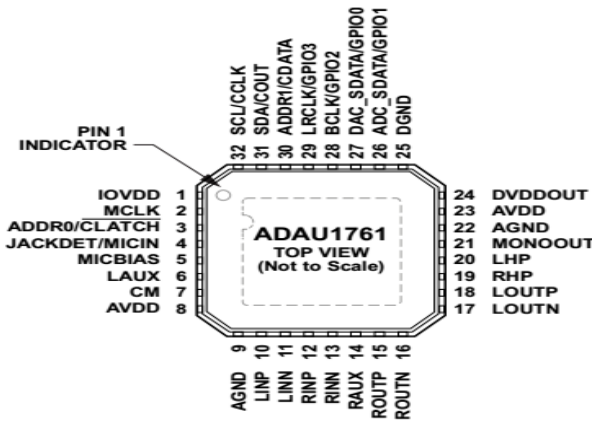

Fig.4.Pin configuration of adau1761 codec

V. MICROPHONE/LINE IN INTERFACING

Microphone is a transducer which converts audio signals into electrical signals. It is directly plug in to MIC in jack of the Zedboard. A line in cable is used in this work to feed input from an audio device. A 3.5mm audio cable is connected to LINE IN jack of the Zedboard and other side is connected to the audio output jack of an audio device.

Fig.5. Electret microphone

VI. IMPLEMENTATION OF DESIGN

To implement this work, Vivado 2017.2, Xilinx SDK 2017.2 tools are used. The hardware used is Zedboard, an electret microphone. Block design was created in the Vivado 2017.2 and IP modules Zed_audio_ctrl, NCO (Numerically Controlled Oscillator), AXI GPIO are created and packaged using Vivado IP packager. These IP's are combined in AXI-4lite to interface with processing system of the Zedboard. The implemented design is illustrated in the following figure 6.

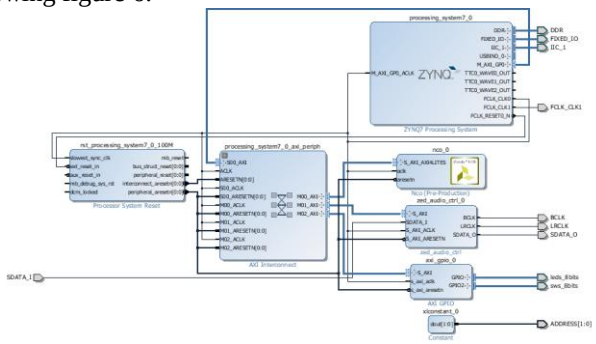

Fig.6.Hardware Design for the proposed audio system

The block design of the audio system is created in the Vivado and the IP blocks required for the design are added to the IP repository. In the block design, a zynq processing system is the central processing system of the hardware block design. Running block automation of the zynq processing system automatically generates the processor system reset. Zynq processing system consists of some memory, wave generators, FCLK_RESET. DDR, FIXED_IO, IIC and FCLK are made as external pins. An IP called NCO [9] from Intel is used in the design. Numerically Controlled Oscillator (NCO) synthesizes a discrete-time, discrete-valued representation of a sinusoidal waveform. It outputs a sinusoidal waveform in two's complement representation. Another IP zed_audio_ctrl is used in the design which has different clocks BCLK, LRCLK, and SDATA_O, output of the block. Clock is used to control the encoding and decoding speed. Every IP block has slave AXI (S_AXI) inside it, and is used to connect to master AXI in the Zynq processing system. AXI_ARESET is used to reset the IP block which brings the IP core to the initialization. AXI_ General Purpose Input Output (AXI_GPIO) IP [10] block has two external ports called leds_8bits and sws_8bits which are used to indicate the switch condition either it is in ON/OFF. Each switch generates a sin wave and is mixed with the input signal. A constant IP block [11] is used to store the present address of the ADAU1761 memory and receive data from the processor and update the address with received data.

The behavior of the hardware is defined by the C script which is written in the application project. Board support packages, drivers required for the audio codec are generated by the SDK. After configuring the application project, it will be programmed to the Zedboard. Hardware setup for the implemented audio system is shown in the following figure.

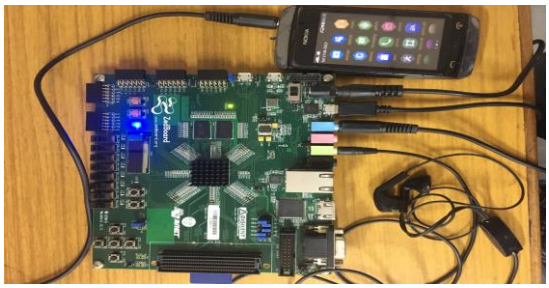

Fig.7. Hardware setup for designed audio system

VII. RESULTS

The aim of this work is to design a real time audio application using FPGA to meet optimized design metrics such as low power, low area, less development time and high speed. The design is implemented by using the resources of the FPGA. Table 1&2 depicts the Resource utilization (Look-up tables, LUTRAM, flip-flops (FF), Block RAM (BRAM), IO and buffer like BFUG) for the synthesis and implementation of the design. As the FPGA has a large number of resources this audio system utilized less number of resources [12]. As a result it consumes very low power. It takes less time to implement the design. The resource utilization details are shown in the following tables.

I. Utilization – Post Synthesis

Resource	Estimation	Available	Utilization %
LUT	961	53200	1.81
LUTRAM	70	17400	0.40
FF	1283	106400	1.21
BRAM	2	140	1.43
IO	25	200	12.50
BUFG	2	32	6.25

II. Utilization Post Implementation

Resource	Utilization	Available	Utilization %
LUT	836	53200	1.57
LUTRAM	68	17400	0.39
FF	1186	106400	1.11
BRAM	2	140	1.43
IO	25	200	12.50
BUFG	2	32	6.25

VIII. CONCLUSION

Many smart applications require embedded audio system and many solutions are available, but this paper gives a unique solution by using SOC-FPGA device. SOC-FPGA is a powerful platform in all aspects to design embedded audio system. This audio system was implemented by combining the processing system (ARM cortex-A9) and programmable logic (FPGA) in Zynq. An electret microphone is connected to the MIC IN jack of the Zedboard to give the hearing sense to the device. A 3.5mm audio cable was used to feed LINE IN to the audio device. As the device Zedboard is an All Programmable SOC everything is programmable. The behavior of the audio system is defined by the application software which is programmable.The behavior can be altered as per the user requirement. Audio codec plays a vital role in this audio system. The entire design controls the audio codec. The audio codec is a less power consuming device which gives better performance.

IX. FUTURE SCOPE

The audio without noise is recommended by the user. The audio produced in this paper may contain some noise and need to be filtered. As an extension, digital filters will be used within the design to filter the noise present in the audio.

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