Development of Analog Behavioural Model of BiMOSFET

Harini. V, Mahesh Acharya, A. Vijayakumari

Abstract: ***Behavioural modelling of a power semiconductor device offers many advantages to an application engineer as it is possible to model the device from the available datasheet without a detailed knowledge of the fabrication process. The development of an analog behavioural model for a BiMOSFET is undertaken here by using the Hammerstein model. The Hammerstein model is developed with static and dynamic block sub-blocks and is designed to respond for varying temperatures.The datasheet values of I_c and $V_{ce}$are utilized to derive the static linear block,while the dynamic block is modelled as Hammerstein current source.The developed model of the BiMOSFET has been verified for its terminal characteristics through OrCAD simulations and hardware testing. The developed model of BiMOSFETexhibits fast simulation times with reasonable accuracy. The hardware testing is carriedout with BiMOSFET IXBF55N300 by observing its currents and voltages under the variation of gate voltage at constant collector emitter voltage and variation of collector emitter voltage at constant gate voltage.***

Keywords: Analog Behavioural Model, BiMOSFET

I. INTRODUCTION

Power electronic systems are the key enablers and the most ubiquitous systems in today's era of 'Green Engineering' due to the evolution of power semiconductor devices catering towards increasing conversion and volumetric efficiencies [1, 2]. Simultaneously, high penetration of electrical circuit simulation software such as SPICE in industries has also become possible owing to increased computing power enabling complex system developments. A successful power electronic design is the result of a proper combination of power devices, circuit topology, and control circuitry. At the application level, the external steady state and transient characteristic of the device is more important than the fundamental physics-based equations [3]. For high power devices, vendor-based or intrinsic SPICE models are often not available necessitating development of device modelling techniques [3]. Semiconductor device modelling can be classified into four types: behavioural modelling, structural modelling, code modelling and analog modelling in HDL (Hardware Definition Language) [4]. Behavioural model has low simulation accuracy and neglects static and dynamic non linear effects. However, the usage of piece wise linear and linear elements in modelling ensures convergence and a reduced simulation time. Structural models have higher accuracies. But, the generated discontinuous non-linear curves cause convergence problems. Code modelling implements the device equations in a subroutine. However, it is not portable and requires simulator recompilation on each model addition. Analog HDL models have high accuracies and mid-level simulation times. However, they require many parameters which are not available in datasheets and are not SPICE portable [5]. Analog Behavioural Models (ABM) are SPICE compatible user-friendly extensions of behavioural models. It allows for the direct implementation of the device non-linear equations. Also, the non-linear characteristic is linearized by piece wise linear approximation [5]. Various ABM for SPICE are proposed in literature for IGBT[6-10, 12]. One among the earliest model was the Hefner Model which exhibited good computation times with reasonable accuracy. The model was first designed for SABER and then subsequently adapted to SPICE [6, 7]. The Hefner model is suitable only for constant temperature simulations [8].Conversely, the Hammerstein model consisting of a static block (linear characterization) and dynamic block (non-linear characterization) [9, 10],with its behaviour closely resembling the physics-based model in [11] overcomes the limitations of Hefner model. However, these models have been simulated using Saber Software which are not Spice compatible. Semiconductor devices undergo five basic phenomena viz. charge storage, resistivity modulation, electrothermal behaviour, MOS-capacitance and breakdown limits, which are very important even for a BiMOSFET. Most accurate models will have to incorporate all these effects precisely [12].The BiMOSFET introduced by IXYS is a reverse conducting switch which is an intermediate between the MOSFET and IGBT. It exhibits the advantages of both these devices viz. fast switching times of MOSFET and power levels of IGBT [13, 14]. This work attempts to simulate an ABM of BiMOSFET by modifying the Hammerstein model in [9] and subsequent verification through simulation studies. The device characteristics are obtained through OrCAD simulations and also verified with an experimental setup.

II. DEVELOPMENT OF ABM OF BIMOSFET

Any analog behavioural macro-modellingstarts with the development of a set of integral and differential equations describing the device behaviour followed by the formulation of the electrical equivalent circuit using controlled current and voltage sources.

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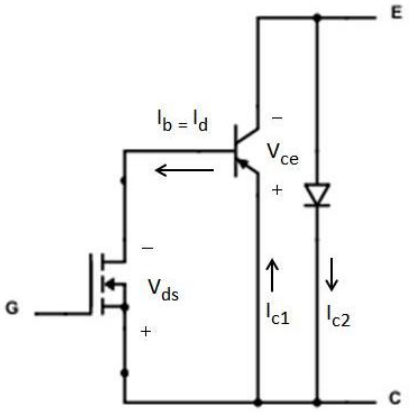

Fig. 1 Equivalent Circuit of BiMOSFET

The BiMOSFET is constructed on a DMOS(Diffusion Mosfet) structure and is hence comprisedof a MOSFET and BJT. However, its base is homogeneous and the shorted N+ region in the BiMOSFETdecreases the PNP transistor gain.This is also responsible for the appearance of an intrinsic diode across the collector and emitter during turn off of the device [13, 14].Thus, the equivalent circuit of a BiMOSFET is represented as a Darlington pair of BJT and MOSFET with a turn off diode as shown in Fig. 1. The model is developed by using the MOSFET equations in linear and saturation regions, BJT in the active region and diode in cut off and saturation regions. The collector current of BJT can be expressed as

$$I_{c1} = (1 + \beta) I_d \#(1)$$

Where, β is the dc current gain of BJT and $I_b = I_d$ are the BJT base current and MOSFET drain current. The saturation voltage ($V_{ds(sat)}$) of MOSFET definesthe boundary for transition from its linear region.

$$V_{ds(sat)} = V_{ge} - V_{th} \#(2)$$

where, V_{th} denotes the threshold voltage of the MOSFET withV_{ds}>$V_{ds(sat)}$, the MOSFET operates in the linear region while V_{ds}<$V_{ds(sat)}$make it operate in the saturation region.

Hence, from equations (1) and (2), the MOSFET drain current (I_d)is expressed as [9]:

$$I_d = \begin{cases} k_p \left[(V_{ge} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right] & \forall\, V_{ds} < V_{ds(sat)} \\ k_p (V_{ge} - V_{th})^2 & \forall\, V_{ds} > V_{ds(sat)} \end{cases} \#(3)$$

Thus,

$$I_{c1} = k_1 \left[(V_{ge} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right] \#(4)$$

Where k_p represents the transconductance and

$$k_1 = k_p (1 + \beta)$$

If V_d denotes the voltage drop of BJT across its base and emitter then, the voltage across collector and emitter can be expressed as,

$$V_{ce} = V_d + V_{ds} \#(5)$$

Thus, the BJT collector current can be expressed as

$$I_{c1} = \begin{cases} k_1 \left[(V_{ge} - V_{th})(V_{ce} - V_d) - \frac{(V_{ce} - V_d)^2}{2} \right], \\ \forall\, V_{ce} < V_{ge} + V_d - V_{th} \\ k_1 (V_{ge} - V_{th})^2 \;\; \forall\, V_{ce} > V_{ge} + V_d - V_{th} \end{cases} \#(6)$$

The diode current is expressed as,

$$I_{c2} = I_{ces} e^{\left(\frac{qV_j}{kT} - 1\right)}$$

From Fig. 1, $I_c = I_{c1} - I_{c2}$, where, I_{ces} denotes the leakage current, q denotes the charge on electron, V_j is the diode junction drop, T is the temperature (25 ^{0}C) and k is the Boltzman constant. The saturation voltage of device can be given by

$$V_{ce(sat)} = V_{ge} + V_d - V_{th} \#(7)$$

However, the relationship between $V_{ce(sat)}$ and $V_{ge}$is non-linear necessitating the use of two correction functions g_1 and g_2.

$$g_1 V_{ce(sat)} = V_{ge} + V_d - V_{th} \#(8)$$

$$\frac{I_{c1(sat)}}{g_2} = k (V_{ge} - V_{th})^2 \#(9)$$

$$g_1 = x_0 + x_1 V_{ge} + x_2 V_{ge}^2 \#(10)$$

$$g_2 = y_0 + y_1 V_{ge} + y_2 V_{ge}^2 \#(11)$$

The values of x_0, y_0, x_1, y_1, x_2 and y_2 are determined from the output characteristics of the datasheet through the solution of three simultaneous equations with three unknown variables. Hence, the corrected collector current is expressed as,

$$I_{c1} = g_2 k \left[(V_{ge} - V_{th})(V_{ce} - V_d) - \frac{(g_1 V_{ce} - V_d)^2}{2} \right] \#(11)$$

Table I: Correction function values for corrected collector current

x_0	1.507
y_0	-0.762
x_1	-0.131
y_1	0.289
x_2	0.03
y_2	-0.006

III. VERIFICATION OF ABM OF IXBF55N300

IXBF55N300 is a 3 kV, 34 A BiMOSFET. The behavioural model of IXBF55N300 is developed using Fig. 1 and replaced in Fig. 2. The terminal characteristics of IXBF55N300 aresimulated in OrCAD using the test circuitin Fig. 2. At First the value of V_g is kept constant and the voltage across the switch, V_{ce} and current through resistor $R_L$represented as $I_c$is observed by varying V_s. Subsequently, the value of V_s is kept constant and by varying V_g, the variation of V_{ce} and $V_{ge}$are observed.

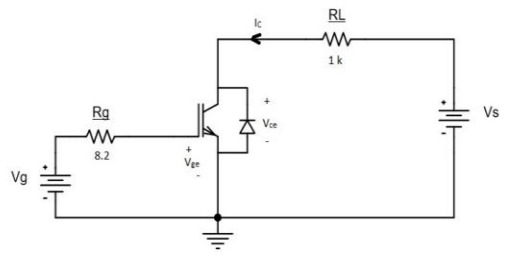

Fig. 2 Test circuit of BiMOSFET

The output characteristics of the BiMOSFET for different V_g values of 3 V, 6 V, 10 V and 15 Varedepicted in Fig. 3, while Fig. 4 represents the variation of V_{ce} with V_g at constant values of$V_s$at 5 V, 10 V, 15 V and 20V. Fig. 5 depicts the transfer characteristics of the BiMOSFET under test.

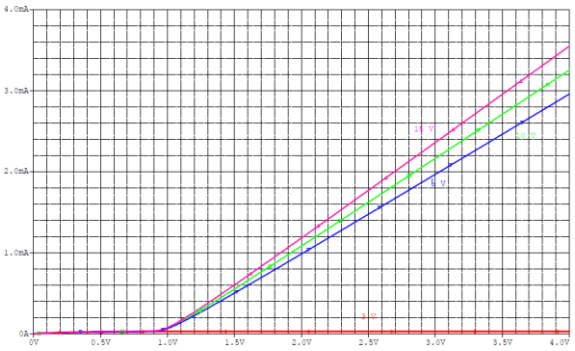

Fig. 3 I_c vs V_s characteristic at constant V_g

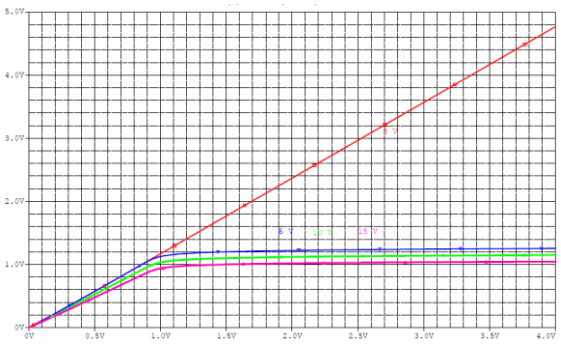

Fig. 4 V_{ce} vs V_s characteristic at constant V_g

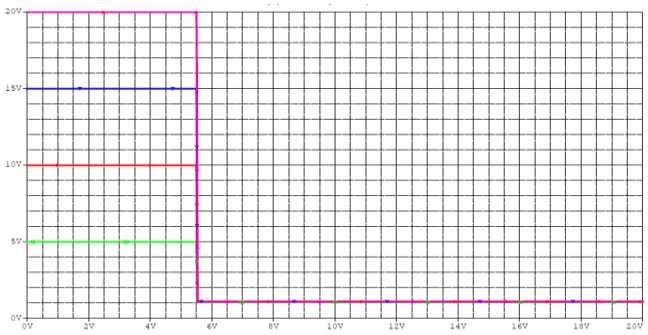

Fig. 5 V_{ce} vs V_g characteristic at constant V_s

The test circuit in Fig. 2 has been verified practically with the experimental set up of Fig. 6. The circuit parameters of test circuit is used in Fig. 6.

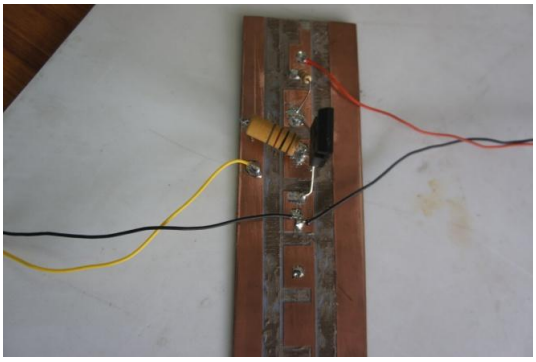

Fig. 6 Hardware test circuit

The observed results are tabulated in Table II and Table III.

Table II: Observed values in practical circuit for constant V_g testing

V_{ge}(V)	V_s(V)	V_{ce}(V)	I_c(mA)
4	0	0	0
	5	4.75	0.22
	10	9.74	0.23
	20	19.67	0.26
6	0	0	0
	5	0.08	4.91
	10	0.97	9.80
	20	1.4	19.59
10	0	0	0
	5	0.08	4.88
	20	0.96	9.82
	20	1.3	19.64
15	0	0	0
	5	0.07	4.95
	10	1.14	9.82
	20	1.32	19.65

Table III: Observed values in practical circuit for constant V_s testing

V_s(V)	V_{ge}(V)	V_{ce}(V)	I_c(mA)
0	0	0	0.03
	5	0	0.03
	10	0	0.02
	15	0	0.03
5	0	0	0
	5	0.08	4.97
	10	1.48	10.02
	15	1.38	14.97
10	0	0	0
	5	0.06	4.96
	10	1.29	9.97
	15	1.14	14.98
20	0	0.32	0
	5	0.36	4.97
	10	1.32	9.96
	15	1.23	14.97
25	0	0.41	0
	5	0.42	4.98
	10	1.21	9.97
	15	1.13	14.99

Table IV: Simulated and Observed Parameters of IXBF55N300

Parameter	Simulation	Hardware	Datasheet
$V_{ge(th)}$	5.4 V	4.23 V	3 V – 5 V
$V_{ce(sat)}$	1 V – 1.2 V	1.14 V – 1.18 V	1.5 V – 1.7 V
I_{ces}	40 µA	20 µA – 30 µA	50 µA

From figures 3 and 4, it can be inferred that the device has a on state drop in the range of 1 V – 1.2 V when conducting currents in the range of 0 mA to 20 mA. From figures 3, 4 and 5, it is observed that the simulated device conducts for values of V_{ge}> 5.4 V and V_{ce}> 1 V. A similar trend in the practical devicebehaviour is observed from Tables II and III. The actual device conducts for values of $V_{ge}\geq$5 V and $V_s\geq$4.23 V. The on state drop in the circuit is found to be between 1.14 V to 1.18 V practically.The on state drop of the device decreases with increase in gate voltage as observed in fig. 4 which is consistent with all power devices. However, at any particular value of V_s, it is expected that I_c should vary with variation in device drops to satisfy KVL of the circuit. This deviation is due to the inadequacy of the modelling technique which needs higher tolerances for assured convergence causing error in computed value. From Table III, it can be concluded that the behaviour of the BiMOSFET model is accurate in the saturation and cutoff regions across the simulated, hardware experimental and the manufacturers' values. However, the model exhibits inaccuracies in the transition from cut-off to saturation i.e. near saturation region.

IV. CONCLUSION

The analog behavioural model for a commercial BiMOSFETIXBF55N300has been developedusing Hammerstein model and implemented in OrCAD simulations and in hardware experiments. The terminal characteristics of the BiMOSFET is verified from the simulation results and correlated with the hardware results and the compliance confirmed. The terminal characteristics are simulated in OrCAD and implemented using a basic dc test circuit. The model has been found to exhibit fast convergence and shown reasonable accuracies in the saturation and cut-off regions. However, the model performance at the near saturation region has been observed to be poor due to approximations and reduced model considered.The model is verified by comparing the simulated and tested values with the datasheet.

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