A Gated Diode DRAM Cell for Improved Power and Speed

Y. N. Thakare, S. N. Kale

Abstract*: In this paper performance analysis of Gated diode based Dynamic Random Access Memory (GD-DRAM) cell is compare with capacitor based DRAM cell in terms of average power dissipation, propagation delay, read access time and write access time at 250nm technology. The GD-DRAM is also referred as capacitorless DRAM. This gated diode stored data in DRAM which is an alternative solution to capacitor. This gated diode DRAM shows cutback in leakage and access time as compared to capacitor based DRAM. A gated diode is formed by shorting two terminal of MOS transistor i.e. source and drain. When the voltage V_{gs} is higher than knee voltage V_{th}; then data get stored on it. Nowadays dynamic random access memory is highly attracting market as compared static RAM because of its high package density, low cost and small area. In this paper this gated diode also resolves the issue of fabrication of capacitor in conventional DRAM cell. The major problem associated with DRAM is power dissipation. The above cells were designed and simulated in Tanner EDA tool and their results were analyzed at 250µm technology. Here we investigated that gated diode based DRAM has superior performance in terms of read time, write time and average power dissipation.

***Index Terms*: DRAM, GD-DRAM, power dissipation, gated diode, speed, etc.**

I. INTRODUCTION

Dynamic Random Access Memory (DRAM) is found in number of electronics devices. They are available in different sizes depends on the device application but in finally their role in all remains same. The basic purpose memory in electronics devices is to store the data and retrieved it whenever it is required. In last few years academician performed lot much research on DRAM to improve power dissipation, efficiency and speed. Numbers of methods and design technique are proposed authors for reading and writing the memory, for minimizing the power dissipation and so on. Various electronic devices such as mobile phones, hand-held gadgets, GPS positioning system, defense and military system, communication system, computers, medical appliances and many more devices which store their data on a memory as shown in figure-1.1.

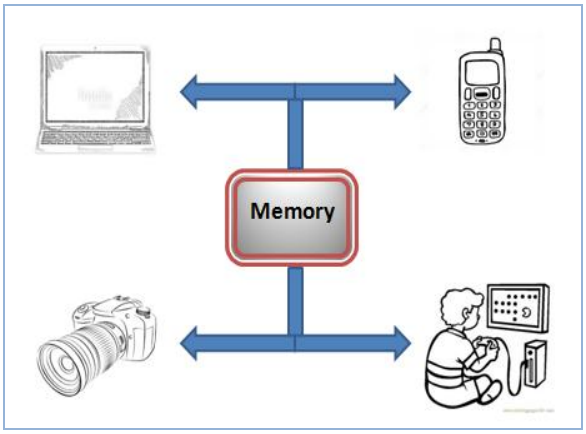

Figure 1.1- Memory Based Electronics Devices

In future it will be predicted that memory will acquire maximum area on embedded chip. This memory must be dynamic random access memory because of its low power, high package density and low cost. By tradition static random access memory was the first choice for embedded devices by the developer just because of its high speed of operation, large noise margin and logic compatibility. There are number of SRAM cell are developed but out of which 6T SRAM cell was widely used for embedded application. However, this 6T SRAM cell has some limitation like number of transistor required per cell, power consumption and area. Hence, there should be an alternative to 6T SRAM cell which overcomes the problem associated with it. Hence, researcher moves towards dynamic RAM. Dynamic random access memory required minimum number of transistor for read write operation as compared to static RAM. As a result area requirement for DRAM cell is very less which increase the integration density of cell.

II. ANALYSIS OF CAPACITOR-DRAM

In dynamic random-access memory (DRAM) data is stored on a capacitor in the form of charge. Depends on the charging level of capacitor the binary logic is considered. If this capacitor is charged then it is considered as logic ‘1’ or discharged then as logic ‘0’. In DRAM capacitor shows leakage and hence its data get lost after some time. To retain its value as it is a refresh cycle should be send before data lost. This is called as destructive read operation of DRAM. There are different DRAM with capacitors circuits are available. Here capacitor based three-transistor DRAM (3T-DRAM) was designed and analyzed in Tanner EDA tool. The 3T-1C DRAM cell circuit is shown in figure 2.1.

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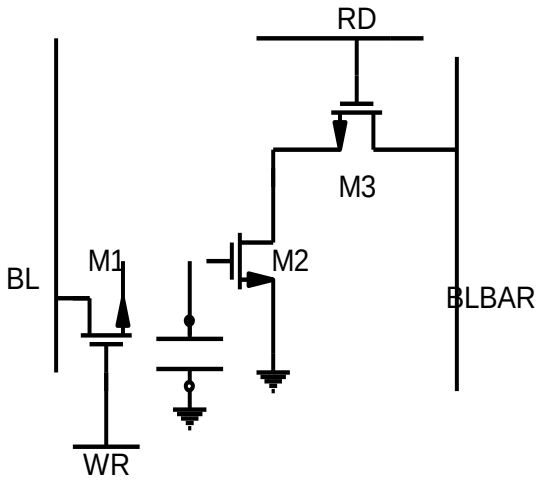

Figure 2.1 Three-Transistor DRAM Cell [7]

The 3T-1C DRAM cell formed the core of the first popular MOS semiconductor memories such as 1KB memory from Intel. This memory used capacitor as a storage node. It was also used for some of the 4 Kb and 16 Kb DRAMs. The 3T cell, as the name implies, consists of 3 transistors and two pairs of column and row lines. There is a write column line and read column line, and there is also a write row line and a read row line. The data to be stored is charged to the gate capacitance of transistor M2. Transistors M1 and M3 are used to control access to the data stored in M2. To write to the cell, the WR is set to "high", which switches M1 on. The data to be written flows from the BL and either charges or discharges the input capacitance C of M2. After the input capacitance has been sufficiently charged or discharged, the WL is then turned off. To read data from the cell, the RD is precharged to a predetermined voltage. M3 is switched on by setting the read row line to high. When M3 is switched on, the BLBAR is either driven low or unchanged based on the data value stored on the input capacitance of M2. If the charge stored at the input capacitance is low (storing logic "0"), then M2 is turned off and the BLBAR is unchanged. Otherwise transistor M2 is on and this will drive the BLBAR down indicating a stored logic 1. The value of a 3T DRAM cell is stored in the input capacitance of M2. Over time, the stored charge will dissipate as the capacitor discharges. Substrate leakage also causes the value to decay. The value has to be refreshed periodically to retain correct values. The schematic view of 3T DRAM cell is shown in figure 2.2.

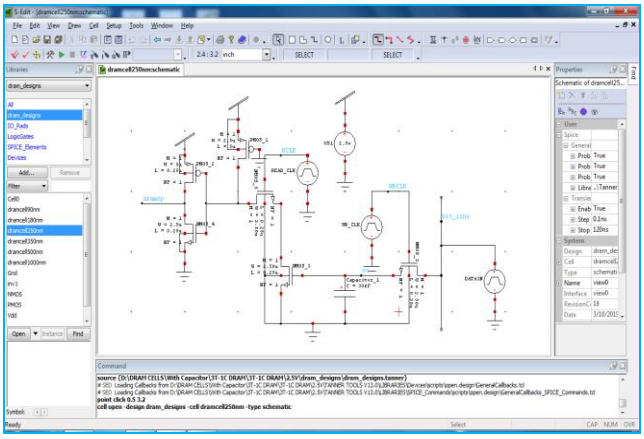

Figure 2.2 Schematic of 3T DRAM Cell

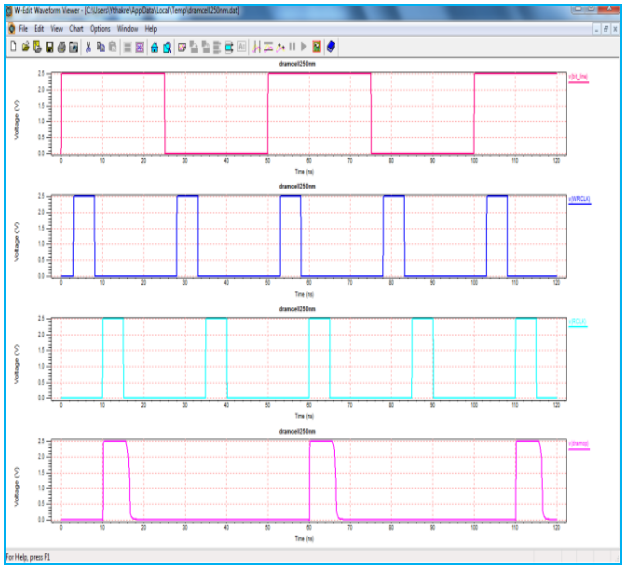

Figure 2.3 Input/Output Waveform of 3T DRAM

III. ANALYSIS OF GD-DRAM

According to current market high density memories are in more demands. Hence to increase the density of cell dynamic RAM is mostly used. Dynamic random access memory cell required minimum number of cell as compared to SRAM. The capacitor based DRAM becomes the popular memory up to last few decades. Nowadays a gated diode is an alternative to the capacitor in DRAM which try to overcome the problems associated with capacitor in dynamic RAM. As in DRAM capacitor acts as primary storage node, hence DRAM density is much as compared to SRAM. DRAM with capacitor was not suitable for VLSI design because fabrication of capacitor was a critical job. Also capacitor shows leakage current and hence periodic refresh was required. It is necessary to replace the capacitor. Hence in recent trends DRAM is design with transistors and gated diode as storage node.

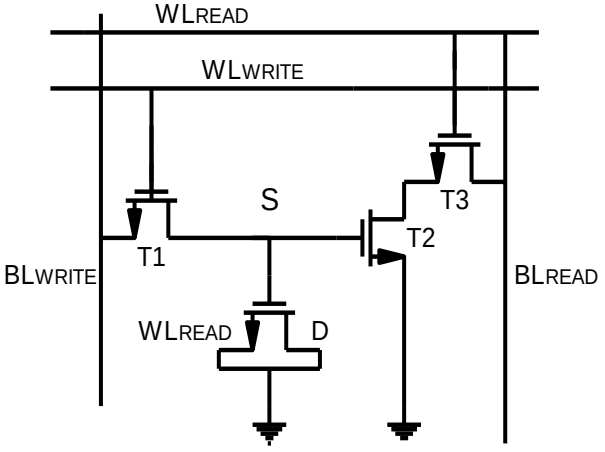

Figure 3.1 Three-Transistor Gated diode DRAM Cell

The gated diode based 3T-1D DRAM cell is most popular DRAM cell because of its non destructive read operation, high package density and to overcome the problem associated with capacitor based DRAM. In conventional DRAM cell data is stored in a capacitor in the form of charge whereas in novel DRAM its store because of voltage controlled capacitance formed by gated diode.
The lack of capacitor is very helpful in terms of scalable design, capacitor fabrication problem.

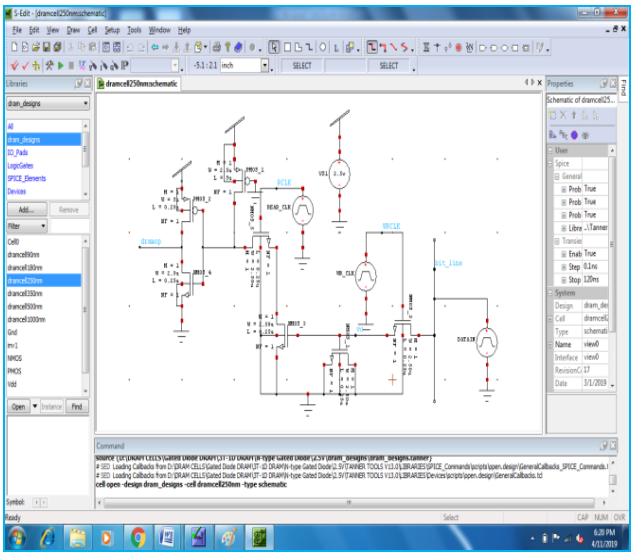

Figure 3.2 Schematic of 3T-1D DRAM Cell

Schematic of the 3T-1D (3-transistor, 1-diode) DRAM cell shows in figure 3.2. During storing '1' on a storage node because of threshold voltage of T1, there is a small drop of voltage on the storage node D1. Hence it's totally depends on gated diode for improving the speed of operation. This diode here performed a role as voltage controlled capacitor, whose capacitance high when data '1' is stored and its low when storing a '0'. Every time when the cell is read, the base of this capacitor reaches at VDD. If the cell stores a '1' and it is read, the charge stored on the capacitor of D1 which boosts up the turn-on voltage of T2, quickly discharging the bitline. As a result, the access speed can match the speed of 6T SRAM cells. Similarly, when a "0" is stored, the capacitance of D1 is smaller and there is almost no voltage boosting, which keeps T2 off during the read. [5]

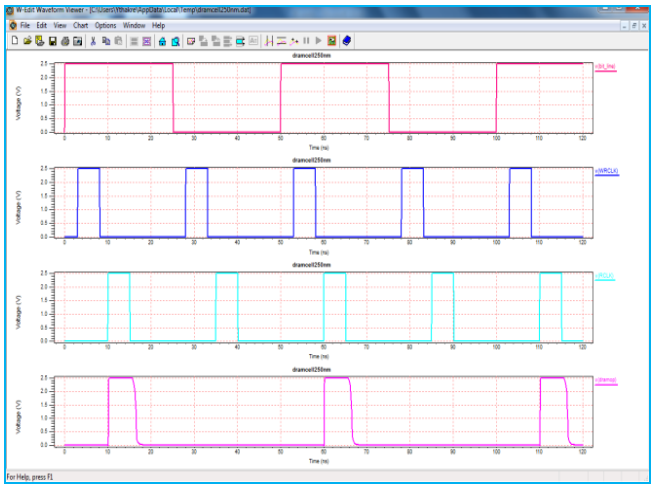

Figure 3.3 Input/Output Waveform of 3T-1D DRAM

IV. SIMULATION RESULT AND PERFORMANCE CAMPARISON

The simulation based performance comparison of 3T DRAM and 3T-1D DRAM in 250nm technology is shown in table 1.

Table1: Performance Comparison of 3T & 3T-1D DRAM

Parameters\ DRAM Cell	3T DRAM	3T-1D DRAM
Technology	250nm	250nm
VDD	2.5V	2.5V
Leakage Current	18 µA	16 µA
Average power	47 µW	40
Propagation Delay	8.55 ns	8.40 ns
PDP	0.4 pJ	0.3pJ
Write Access Time	150 ps	126 ps
Read Access Time	220 ps	189 ps

The graph shown in figure 4.1 shows that 3T-1D DRAM cell has less leakage current as compared to 3T DRAM.

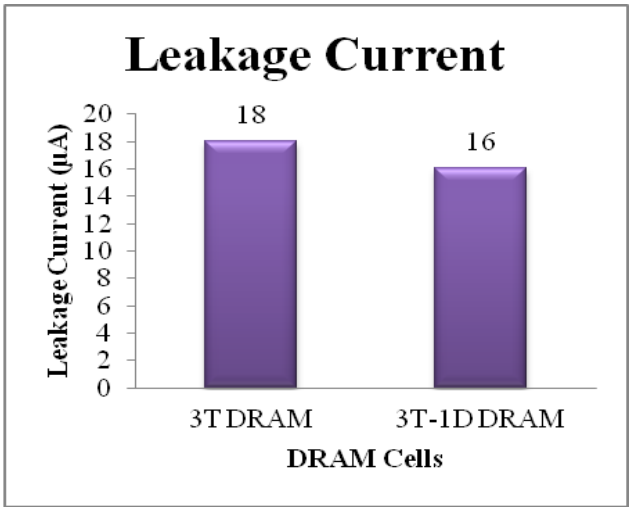

Figure 4.1 Leakage current of DRAM Cell

The graph shown in figure 4.2 shows that 3T-1D DRAM cell has less average power as compared to 3T DRAM. Hence by the use of gated diode in place of capacitor, power dissipation goes down.

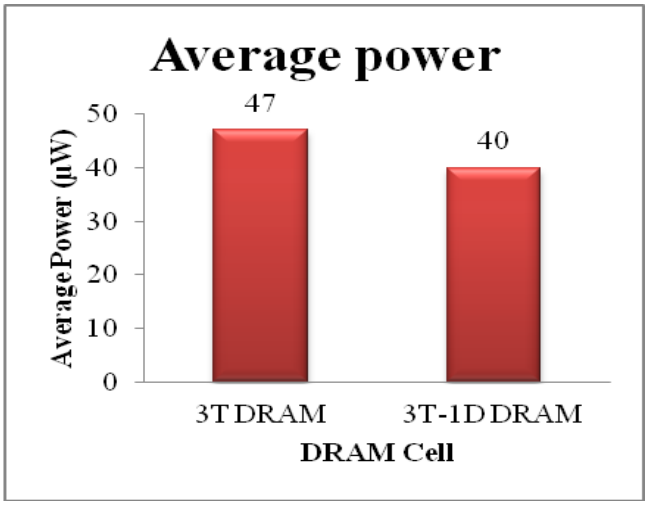

Figure 4.2 Average power of DRAM Cell

The graph shown in figure 4.3 shows that 3T-1D DRAM cell has less propagation delay as compared to 3T DRAM.

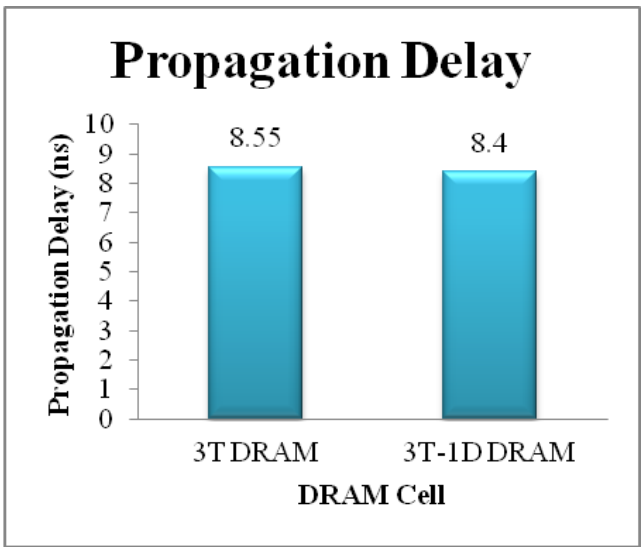

Figure 4.3 Propagation Delay of DRAM Cell

The graph shown in figure 4.4 shows that 3T-1D DRAM cell has less power delay product as compared to 3T DRAM.

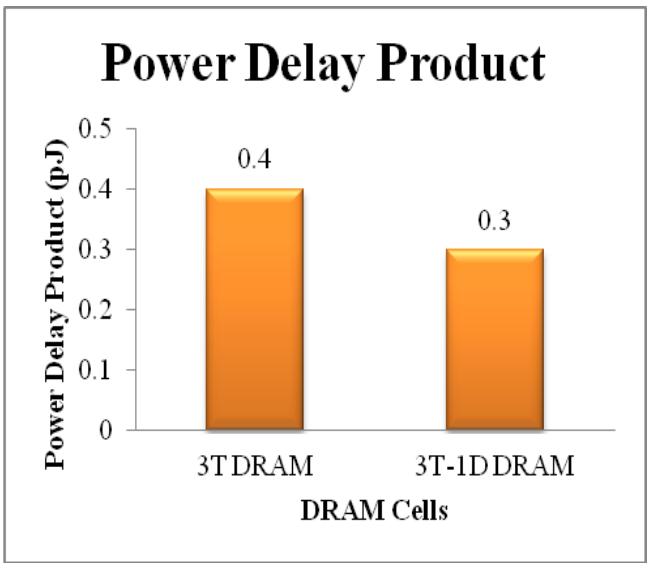

Figure 4.4 Propagation Delay of DRAM Cell

The graph shown in figure 4.5 shows that 3T-1D DRAM cell has less write access time as compared to 3T DRAM. Hence by the use of gated diode in place of capacitor, speed operation of memory is become faster.

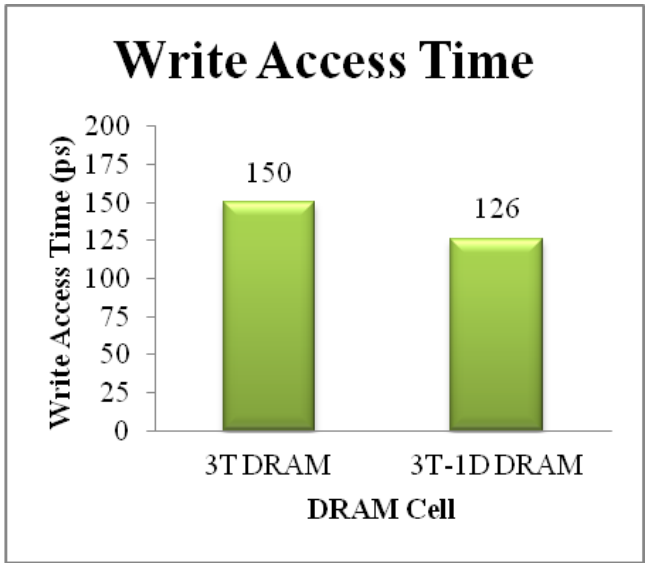

Figure 4.5 Write Access Time of DRAM Cell

The graph shown in figure 4.6 shows that 3T-1D DRAM cell has less read access time as compared to 3T DRAM. Hence by the use of gated diode in place of capacitor, speed of operations quite improvement.

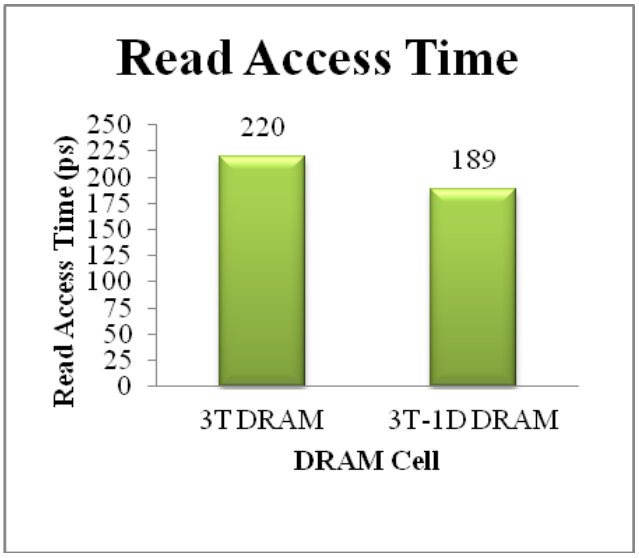

Figure 4.6 Read Access Time of DRAM Cell

V. CONCLUSIONS

From the above performance parameters analysis it is observed that the 3T-1D DRAM cell in 250nm technology shown that better performance as compared to 3T DRAM in terms of leakage current, average power dissipation, propagation delay, power delay product, write access time and read access time. From the performance analysis it is observed that the 3T-1D DRAM gives better result as compared to 3T DRAM. It has been designed and analyzed that gated diode DRAM cell gives 40µW power which is less than capacitor based DRAM.

REFERENCES

1. A.Mudgal, S. Akashe, S.B.singh, "Power analysis of 3T DRAM cell using FinFET at 45nm Process Technology," In proceeding of World Congress on Information and Communication Technologies (WICT), pp.555- 560,October 2012,Trivandrum, India.
2. E. Amat, A. Calomarde, C.G. Almudever, N. Aymerich, R. Canal, A. Rubio, "Impact of FinFET and III-V/Ge technology on logic and memory cell behavior," IEEE Transactions on Device and Materials Reliability vol.l4, No.l,pp.344-350, March 2014.
3. E. Amat, C.G. Almudever, N. Aymerich, R. Canal, A. Rubio, "Strategies to enhance the 3TiD-DRAM cell variability robustness beyond 22nm," Microelectronics Journal vol. 45, No.IO, pp.1342-1347, October 2014.
4. P.Asthana, S.Mangesh, "Capacitor Less DRAM cell Design for high performance embedded system," In proceeding of International Conference on Advances in Computing, Communication and Informatics(ICACCI),pp.554-559, September 2014, New Delhi, India.
5. Y.Thakare, S.Kale "An Effect of Process Variation on 3T-1D DRAM" International Journal of Scientific & Engineering Research, Volume 4, Issue 7, July-2013 170 ISSN 2229-5518.
6. Y.Thakare, S.Kale, "Performance Analysis of N-Type Gated Diode Three-Transistor DRAM in 180nm Technology" Helix Vol. 8(6), Copyright © 2018 Helix E-ISSN: 2319-5592; P-ISSN: 2277-3495, pg.4388- 4393.
7. Y.Thakare, S.Kale, "Analysis of Different Parameters of 3T-1D Dram Cell Using N-Type and P-Type Gated Diode in VLSI Technology" Cikitusi Journal For Multidisciplinary Research, ISSN NO: 0975-6876, Volume 6, Issue 2, pg.93-102.
8. M.T.Chang et.al, "A 65nm Low Power 2T1D Embedded DRAM with Leakage Current Reduction" IEEE International SOC Conference, Hsin-Chu, Taiwan, 26-29 September 2007.
9. B. Raj et.al., "Analysis of Power Dissipation In DRAM Cells Design For Nanoscale Memories" International Journal of Information Technology and Knowledge Management July-December 2009, Volume 2, No. 2, pp. 371-374.
10. T. Gupta et. al., "Comparative analysis of 2T, 3T and 4T DRAM CMOS cells" International Conference on Information, Communication, Instrumentation and Control, Indore, India ISBN:978-1-5090-6314-7, 05 February 2018.

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