

# Design and Analysis of Cascode LNA for 60 GHz Wireless Applications

Rajendra Chikkanagouda, Cyril Prasanna Raj P.

**Abstract-** Design methodology and analysis of a 60GHz-band Low Noise Amplifier (LNA) is presented in this paper. The LNA has been designed and simulated using source degenerated cascode topology in 90 nm CMOS for operation at 60 GHz. The structured LNA is minimized for its area with 50%. The designed LNA is computed with ADS and is verified its functionality in terms of Noise Figure (NF), Gain, Linearity, Power dissipation and Stability. The designed LNA uses 12 mW of dc power from a 1.5 V supply with 16.3 dB gain and a NF of 3.5 dB at 60 GHz. The designed LNA is unconditionally stable and has IIP3 of -9 dBm with FoM of 15.

**Index Terms:** 60 GHz, 90 nm, CMOS, LNA, Cascode, ADS.

## I. INTRODUCTION

A significant research topic in the domain of microwave engineering today is low-cost transceiver front-end designs for the unlicensed frequency band around 60 GHz. Historically, Monolithic Microwave Integrated Circuits (MMICs) have been composed using III-V semiconductor technologies, such as Gallium Arsenide (GaAs) or Indium Phosphide [InP] have been reported in [1, 2], an expanding number of 60 GHz building blocks and systems have been recently reported in advanced SiGe BiCMOS [3, 4, 5] and CMOS technologies [6, 7, 8, 10]. Still, a CMOS technology promises higher levels of integration, reduced cost, size and power consumption. CMOS implementation also benefits directly from Moore's Law [10], and CMOS performance is improving at regular intervals, expanding its usefulness into mm-wave frequencies. SiGe Heterojunction Bipolar Transistor (HBT) technology offers maximum cut-off frequency ( $f_T$ ) competitive with GaAs, although GaAs still offers better integration of passives and better power-handling capability. The 60 GHz band experiences attenuation due to oxygen retention. The oxygen absorption at 60 GHz severely limits range of long distance and used for short range wireless links. [12, 13]. Low Noise Amplifier (LNA) design is required to be carried out by considering design requirements such as stability, low Noise Figure (NF), gain, FoM and matching performance [5]. Of all the design requirements NF and gain have been given due consideration in LNA design. There are several LNA topologies such as the Common Gate (CG), cascode, Common Source (CS), Current Reuse (CR) and distributed amplifier topology are the important topologies.

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In this paper, 60 GHz of 90 nm RF-CMOS is explored in the implementation of critical building block of LNA. Cascode LNA design is selected for its circuit simplicity and is designed to operate at 60 GHz band. Designing a LNA for mm-wave applications and its simulation setup is presented in Section 2 and Section 3 respectively. Discussion on Results is reported in section 4. Conclusion is reported in Section 5.

## II. LNA DESIGN METHODOLOGY

The LNA utilizes single ended two stage cascode [3], as this topology allows for better reverse isolation and good stability. The reverse isolation and stability are essential parameters for direct conversion architectures. Series inductors are placed between the CS transistor and CG transistor for improvements in gain, NF and bandwidth. The cascode LNA is shown in Fig. 1 has two transistors  $M_1$  and  $M_2$  which is a cascaded version of CG and CS structure respectively. These two stages are connected through series inductor  $L_M$ . CS gate structure is connected with gate inductance  $L_g$  and source inductor  $L_s$ . The Voltage  $V_{in}$  is the gate input through  $C_1$  (Coupling Capacitor). Ali M. Niknejad [14] has reported on cascode LNA design which is found to have virtually low noise at low and medium frequencies. Based on discussions presented in [14] cascode LNA configuration is carried out. The MOSFET input impedance [14] is given by equation (1),

$$Z_{in} = j\omega L_s + \frac{1}{j\omega C_{gs}} + R_s \quad (1)$$

The series RLC circuit resonant frequency is tuned to the desired operating frequency. The gate inductor  $L_g$  is introduced to carry out for tuning. The equivalent circuit of cascode LNA is presented in Fig. 2, considering small signal analysis. The small signal model comprises of the voltage controlled current source, a constant current source which are in parallel between drain and source. A parasitic capacitance  $C_{gs}$  is present between source and gate. The current  $i_o$  from drain flows to ground through  $r_o$ . A small impedance  $r_o$  generates DC bias at the gate causing source degeneration. Based on discussions presented in Ali M. Niknejad [14], the fundamental principles of LNA design the LNA's noise current can be computed by using equation (2),

$$\left(1 - \frac{-g_m r_o}{1+g_m r_o}\right) i_d = \left(\frac{1}{1+g_m r_o}\right) i_d \quad (2)$$

## Design and Analysis of Cascode LNA for 60 GHz Wireless Applications

The MOSFET trans-conductance is  $g_m$ ,  $i_d$  is the noise current and  $r_o$  is transistor degeneration resistance.

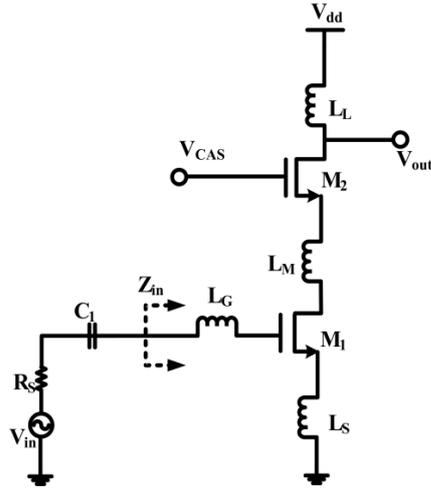


Fig. 1 Cascode CMOS LNA

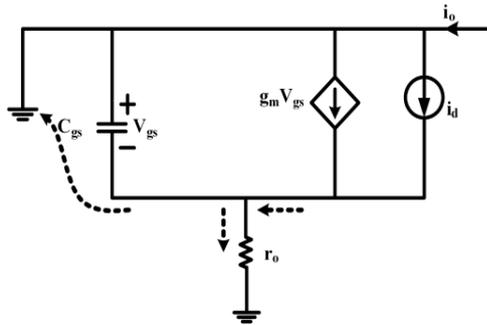


Fig. 2 Small signal model of cascode LNA

The design of cascode topology is discussed in [3] and shown in Fig. 3 which exhibits good isolation, improved bandwidth and better gain even at mm-wave frequencies. For enhancing the LNA performance, an inductor ( $L_M$ ) is placed in cascode configuration. This inductor forms an artificial transmission line between the CS and CG to satisfy for its lower maximum  $f_T$  (cut-off frequency).

The value of gate oxide capacitance is identified to be  $13.806 e^{-3}$  by considering equation (3),

$$C_{ox} = \frac{\epsilon_r \epsilon_0}{T_{ox}} \quad (3)$$

The centre frequency  $\omega_0 = 2\pi f$  is calculated which is found to be  $377.143 e^{-3}$  radians/sec.

90 nm technology being used for LNA design, the length of the transistor is set to 90 nm and the source resistance is assumed to be 50 Ohm as per recommended standards. The width ( $W$ ) of the transistor is found to be  $32 \mu\text{m}$  by computing equation (4),

$$W = \frac{3\omega_0 R_S C_{ox} L}{4} \quad (4)$$

The value of gate to source capacitance  $C_{gs}$  is calculated from equation (5) which is found to be 265 pF,

$$C_{gs} = \frac{2\omega_0 C_{ox} L}{3} \quad (5)$$

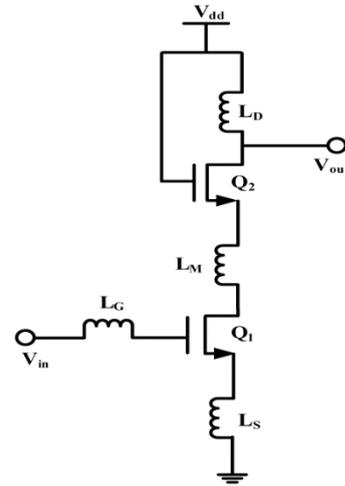


Fig. 3 Cascode with middle inductor

The value of degeneration inductor  $L_S$  is set as 60 pH and the cut off frequency  $\omega_T$  is found to be  $8.33 e^{11}$  radians/sec by considering equation (6),

$$\omega_T = \frac{g_m}{C_{gs}} = \frac{R_S}{L_S} \quad (6)$$

The effective trans-conductance  $g_m$  of LNA is found to be 220 A/V by considering equation (7),

$$g_m = \omega_T C_{gs} \quad (7)$$

The value of gate inductor  $L_G$  is found to be 205 pH by considering equation (8),

$$L_G = \frac{1}{\omega_0^2 C_{gs}} - 1 \quad (8)$$

The load inductor values are 70.3 pH and 46.87 pH by computing equation (9),

$$L_{LOAD} = \frac{1/2\pi f}{C_{OUT}} \quad (9)$$

The next section presents detailed discussion on proposed two stage LNA.

### III. 60 GHz LNA DESIGN

The two stage cascode LNA schematic is shown in Fig. 4. The cascode topology minimizes the capacitance effect between the gate and drain  $C_{gd}$ . This advances reverse isolation and stability. The design consists of two stages, of which each stage of two transistors. The first stage is designed for simultaneous noise and input matching. The second stage is designed for gain improvement. The second stage transistors  $M_3$  and  $M_4$  have higher widths ( $30 \mu\text{m}$ ) than  $M_1$  and  $M_2$  ( $20 \mu\text{m}$ ) for better linearity. The DC-blocking capacitor  $C_C$  is placed between two stages. The series inductors ( $L_{M1}$  and  $L_{M2}$ ) are placed in each stage between the CS and the CG circuit. The first stage is to minimise the noise and second stage is for gain improvement with good linearity.

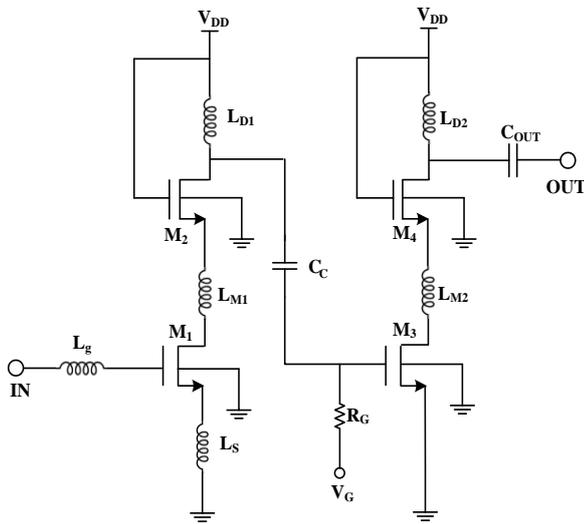


Fig. 4 Schematic of the proposed LNA

The corresponding specifications of the LNA are operating frequency between 58 GHz to 65 GHz, NF less than 4 dB, gain greater than 14 dB, good linearity and stability. Considering the designed parameters of the transistor geometry the LNA is modelled and LNA parameters are required to evaluate LNA performance is computed by using 90 nm BSIM3 model. The Figure of Merit (FoM) is described in ITRS [15]. The FoM is characterized in equation (10).

$$FoM_{LNA} = \frac{G.IIP3.f}{(F-1)P} = \frac{OIP3.f}{(F-1)P} \quad (10)$$

Where G is gain, F is Noise Factor, P is power consumption, IIP3 is Third Order Intercept Point and F is Frequency. Accomplishing a decent FoM for LNA at mm-waves is nontrivial, since the performance degrades when CMOS devices operating at frequencies close to the transistor values. In Fig. 4, the characteristic impedance ( $Z_{o1}$ ) is equal to the load impedance of  $M_1$  (equation 11) and source input impedance of  $Q_2$  (equation 12).

$$Z_{o1} = \sqrt{\frac{L_{M1}}{C_{gs2} + C_{sb2}}} = Z_{Q1,load} \quad (11)$$

$$Z_{o1} = Z_{Q2,in} = \frac{1}{g_{m2}} + \frac{\omega L_{D1} Q}{1 + g_{m2} r_{o2}} \quad (12)$$

The main design considerations and steps involved for LNA design are explained in next section.

#### A. Choice of Optimum Current Density ( $J_{opt}$ )

For LNA design, choosing the current density at the minimum noise figure ( $NF_{min}$ ), maximum cut-off frequency and maximum oscillation frequency ( $f_{MAX}$ ) is necessary to determine the transistors biasing point [11]. The maximum gain and  $NF_{min}$  are the main design goals, the circuit should support peak  $f_{MAX}$ . However, in this case, the  $J_{opt}$  values lies between the optimum  $J_{opt}$  at minimal noise and  $f_T$  (transit frequency). The cascode topology comprises biasing at the minimum noise current density  $J_{opt}$ , which ensures simultaneous input impedance and noise impedance.

#### B. Choice of Q-Factor

The selection of Q-factor is important in the design of LNA. For mm-wave and UWB (ultra-wide band) applications low Q-factor and for narrow band a high Q-factors are preferred. The inter dependence of the Q-factor, bandwidth, gain,  $C_{gs}$ , resonance frequency and inductance (input matching) is considered. The Q-factor can be derived by using source resistance ( $R_S$ ) and load resistance ( $R_L$ ).

#### C. Introduction of Source Degeneration Inductor

The addition of source inductor ( $L_S$ ) in the first stage helps to stabilize the amplifier, improves the linearity and reduces the noise [19]. For optimum matched network, the impedance at the input side is equivalent to the complex conjugate of the source impedance ( $Z_S$ ). The  $Z_S$  is calculated by using equation (13), where  $Z_{in}$  is the input admittance.  $Z_{sopt}$  is the optimum source admittance,  $r_s$  is source inductor resistance and  $r_g$  gate inductor resistance [19].

$$Z_s = Z_{in} = Z_{sopt}^* \quad (13)$$

The resistive component of  $Z_{sopt}$  is used for analysing the input matching network.

#### D. Source to Gate Capacitance ( $C_{gs}$ ) Computation

The LNA gain and noise performance is adversely effected by  $C_{gs}$ . The  $L_g$  is necessary for ensuring optimal input matching. The relationship between the  $C_{gs}$ , trans-conductance  $g_m$ , and angular transition frequency ( $\omega_T$ ) is given by equation (14),

$$C_{gs} = \frac{g_m}{\omega_T} \quad (14)$$

$$L_g = \frac{X_{sopt}}{\omega} - L_s \quad (15)$$

#### E. Series Inductor across CS and CG Transistor

The cascode topology is chosen which consists of two stages with each stage the series inductor is placed between transistors of  $M_1, M_2$  and  $M_3, M_4$ . The optimised values are computed by simulating and plotting of NF and  $f_T$  against  $L_{M1}$  and  $L_{M2}$  [3]. The gain, NF,  $P_{1dB}$ , IIP3 and stability factor simulation result analysis is discussed in next section.

### IV. RESULTS ANALYSIS

The LNA was designed and simulated using 90 nm CMOS PTM model [20]. The LNA performance is analysed by considering the parameters such as linearity, gain, NF and power consumption. The schematic is captured in ADS and process parameters of the PTM model is imported for simulation.

#### A. Power Gain ( $S_{21}$ ) and NF Analysis

The cascode LNA is analysed for its gain response in the frequency of 56 GHz to 66 GHz. The  $S_{21}$  and NF are obtained with respect to frequency of LNA in ADS simulation and the corresponding results are presented in Fig. 5.

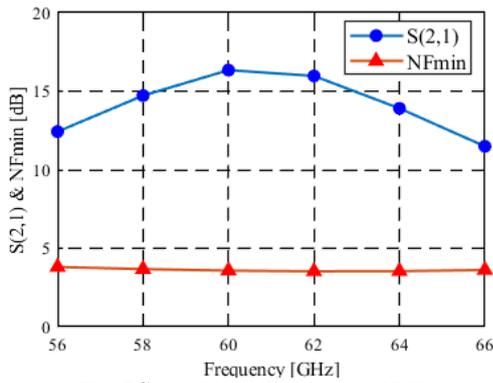


Fig. 5 S<sub>21</sub> and NF of the proposed LNA

From the results obtained the following observations are made. Maximum gain of 16.34 dB and NF<sub>min</sub> of 3.57 dB are obtained at 60 GHz. The gain of LNA is less than 15 dB from 56 GHz to 58 GHz and from 63 GHz onwards. The gain more than 15 dB is observed from 58.5 GHz to 63 GHz. The simulation result of NF is less than 4 dB in the entire frequency band of 56 GHz to 66 GHz.

**B. P1dB and IIP3 Analysis**

The Third-Order Intercept point (TOI or IIP3) and the 1-dB compression point (P<sub>1dB</sub>) are the two important parameters to determine the amplifier efficiency. These quantities are required to compare amplifier specifications and performance for specific frequency range. Amplifiers have definite gain for particular frequency range and input power. The gain starts decreasing or saturates and goes to compression for further increase of input power. The gain flattens, implying that at high power levels greater than -19 dBm the amplifier becomes saturated with a flat response.

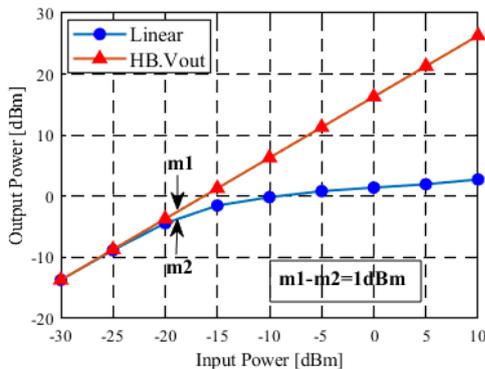


Fig. 6 P1dB of the proposed LNA

Fig. 6 shows P<sub>1dB</sub> of the proposed LNA. The real response (V<sub>out</sub>) follows linear response from -30 dBm to -20 dBm. The difference of 1 dB occurs at -19 dBm. The gain saturates or starts decreasing by further increase of input power. The saturated or overdriven amplifier generates signals that are of least preference in addition to required signal which is defined as Intermodulation Distortion (IMD). The third order harmonic is much harmful because its frequency is close to the fundamental tone. Two harmonics are compared with the input power. Fig. 7 shows IIP3 of the LNA, the third order and first order harmonic meet at -9 dBm of input power. The proposed cascode LNA has -9 dBm of IIP3 which is better than the existing LNAs.

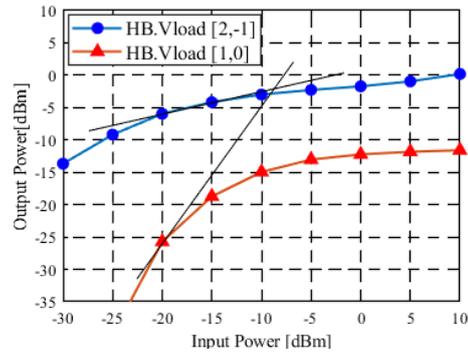


Fig. 7 IIP3 of the cascode LNA

**C. Stability and FoM Analysis**

In amplifier design, the stability factor K is required to be satisfied as provided in equation (16) [16, 17]. LNA is set to be stable only if stability factor K greater than 1 and Δ factor is required to be less than 1, defined in equation (17).

$$K = \frac{1+|\Delta|^2+|S_{11}|^2-|S_{12}|^2}{2|S_{12}||S_{21}|} > 1 \tag{16}$$

$$\Delta = |S_{11}| \cdot |S_{22}| - |S_{12}| \cdot |S_{21}| < 1 \tag{17}$$

The value of stability factor (K) is greater than 1 for frequency range of 56 GHz to 66 GHz as depicted in Fig. 8. The Δ is found to be less than 1 and satisfying the condition in equation (17) in the entire frequency spectrum. The FoM of proposed LNA includes the properties such as gain, linearity and NF which is 15.

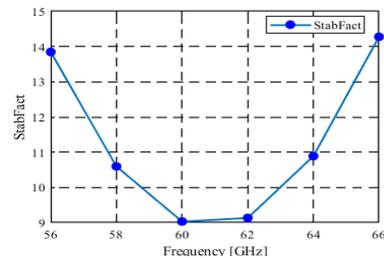


Fig. 8 Stability Factor (K) of the LNA

**D. Analysis of Gain and Noise Figure against V<sub>GS</sub>**

Fig. 9 shows the gain of the proposed LNA with different gate bias voltage (V<sub>GS</sub>) of transistor M<sub>1</sub>. The gate to source voltage (V<sub>GS</sub>) is varying from 0.5 V to 1.2 V. The gain and NF are analysed with respect to V<sub>GS</sub>. The S<sub>21</sub> is found to be 14.11 dB to 16.33 dB when V<sub>GS</sub> is varying from 0.6 V to 0.7 V. Further increase of V<sub>GS</sub> from 0.7 V to 1 V S<sub>21</sub> is reported between 16.33 dB to 16.16 dB. The NF is less than 5 dB from 0.6 V to 0.7 V and constant value of 4 dB from 0.7 V to 1.0.

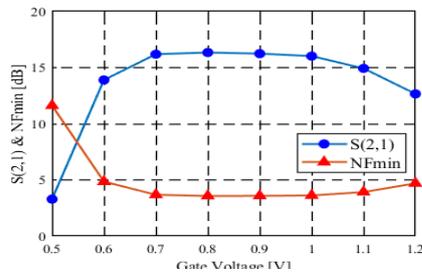


Fig. 9 60 GHz LNA gain and NF versus  $V_{GS}$  of LNA  $M_1$

**E. Gain and NF versus  $V_{DD}$  Analysis**

Fig. 10 shows the NF and gain of the cascode LNA with different supply voltage ( $V_{DD}$ ). The maximum gain of 15.66 dB at 60.5 GHz is found with a supply voltage of 1.2 V. The  $NF_{min}$  of 3.62 dB is found at 1.2 V. The maximum gain of 16.37 dB at 60.5 GHz and  $NF_{min}$  of 3.53 dB at 62.5 GHz are observed for 1.5 V supply voltage. The LNA has a peak gain of 16.34 dB and  $NF_{min}$  of 3.57 dB with a supply voltage of 1.5 V.

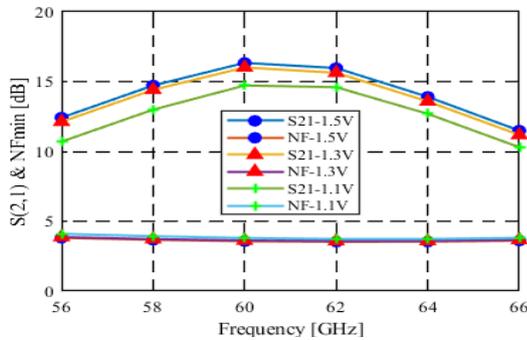


Fig. 10 Gain and NF against different  $V_{DD}$

Table 1. Comparison with published CMOS-90nm LNAs

Parameters	[5]	[3]	[9]	This Work
Stage/ Topology	2/CB & CE	2/Cascode	3/CS	2/Cascode
Freq. [GHz]	61.5	58	60	60
$S_{21}$ [dB]	14.7	14.6	12.2	16.34
NF [dB]	4.5	< 5.5	6.5	3.57
$S_{11}$ [dB]	-6.0	-7.5	-5.0	-8.75
$S_{22}$ [dB]	-17.0	-7.0	-5.0	-2.43
IIP3 [dBm]	-8.5	-6.8	--	-9.00
P1dB [dBm]	-20.0	--	+4.0	-19.00
$P_{DC}$ (mW)	10.8	24(1.5)	10.5	12
FoM	11.6	5.7	--	15.3

Comparison of different LNA topologies for mm-wave applications with 90 nm CMOS is shown in Table 1. The presented LNA achieves better gain, FoM and optimum  $NF_{min}$  among past LNAs in technologies. The simulation results indicate that the gain is improved by a factor of 25.33%, NF is improved by a factor of 42% and FoM improved by a factor of 62.74%. The MOSFETs width of first and second stages are considered 20  $\mu m$  and 30  $\mu m$ .

**V. CONCLUSION**

A low noise figure, high-gain inductively loaded LNA across the V-band is presented using the 90 nm RF-CMOS process. The LNA is designed using two-stage cascode topology with degenerative source to reduce the NF of the

circuit. The LNA is biased at an optimal point to reduce the NF of the circuit significantly. The transistor geometries are imported for simulation in ADS. The simulation results show that the designed LNA is appropriate for mm-wave applications of 58 GHz - 64 GHz with maximum gain of 16.34 dB and NF of 3.77 dB, with excellent linearity, stability and FoM.

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