Design of Area Efficient Beam Steering Control System for Phased Array Radar

S. Ramya Sri, Shaik Fayaz Ahamed, A. Anitha, K. Naga Sunanda

Abstract*: Phased array radar architecture consists of the multiple antenna elements that are controlled by the active electronic circuits called T/R modules. Transmit/Receive modules (T/R modules) plays vital role in the modern phased array radar system for different radar applications. The problem asserted with electrically scanned phased array radar suffers from two main limitations. First one is the high hardware cost in terms of area and second one is the design complexity. To overcome the above issues, architecture has been developed by implementing single control unit, distributive memory elements and data control logic to design an area efficient control system. The entire system is implemented on Artix-7 FPGA.

Index Terms*: Central *Control Unit, Distributive memory elements, data control logic, Phased array radar.

I. INTRODUCTION

Since 1950s, Phased array radars are used in military and civilian applications. Traditionally, these radars have been steered mechanically and then they are replaced to the active electronically steered arrays. Removing mechanical part and distributing a single source power electrically to the number of elements makes a system more robust, reliable and cost effective [1] [2].

Currently, they play a prominent role in defining the type of radar and communications system that will be installed on the next generation. Radar is an electromagnetic system for detection and location of target object. Phased array is a directive antenna made up of a number of individual antennas, or radiating elements, which are fed coherently and uses variable phase values associated with "transmitter-receiver" (TR) modules that are controlled by the digital controllers.

Phase shifters have been used at the end of the antenna array to shift the beam in required direction. They can be controlled digitally or employ digital to analog converter at some level [3]. Phased-Array radars require large number of active microwave components to scan electronically in both the azimuth and elevation planes, thus significantly increasing the area cost of the entire radar system. To address the issue, CASA has designed "Phase-Tilt" radar that scans electronically in azimuth and mechanically in elevation [5]. In this paper, architecture is developed for 14 array channel offers a phase shift range of 0 to 360º. The digital phased shifters used in this array are of 5-bits each. The paper also reports the area and timing factors that are occupied by the entire system.

II. SYSTEM DESIGN

This section discusses the beam steering control system architecture, which is comprised of a digital controller that consists of three main functional blocks, UART control unit, and Distributive memory elements and data control logic as illustrated in fig.1 that implemented to the T/R modules. UART control unit that passes the received data and the programmable look-up tables which store the phase values that are given to the antenna array, output of it is send to the buffer.

The architecture has been implemented to 14 element array and the same can be extended to more number of antenna arrays. Let us consider, for the nth scan angle, the control unit generates a serial stream of 8 bit data which passes through transceiver which includes the scan angle and frequency as an integer binary number.

The data is supplied in parallel to the corresponding input terminals of the look-up table, designed to generate phase values for a particular angle and frequency. The output data returned by the look-up table contains the 5 bit phase value PS [5:0] to steer the beam. It sends the data to the buffer to store the data that have been distributed to the antenna elements

A. Distributive memory elements:

The main task of it is the conversion of the received values into the settings for phase shifters. To make this conversion a possible solution, preload the settings into memory blocks for all considered and quantized azimuth values rather than calculating the settings from time to time, in this way can obtain two advantages, decrease of the time required to switch the beam angular position and simplification of process executed by the memory elements.

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S.Ramya Sri, Electronics and Communication Engineering, V R Siddhartha Engineering College, Vijayawada, India.

Shaik Fayaz Ahamed, Electronics and Communication Engineering, V R Siddhartha Engineering College, Vijayawada, India.

A.Anitha, Electronics and Communication Engineering, V R Siddhartha Engineering College, Vijayawada, India.

K.Naga Sunanda, Electronics and Communication Engineering, V R Siddhartha Engineering College, Vijayawada, India.

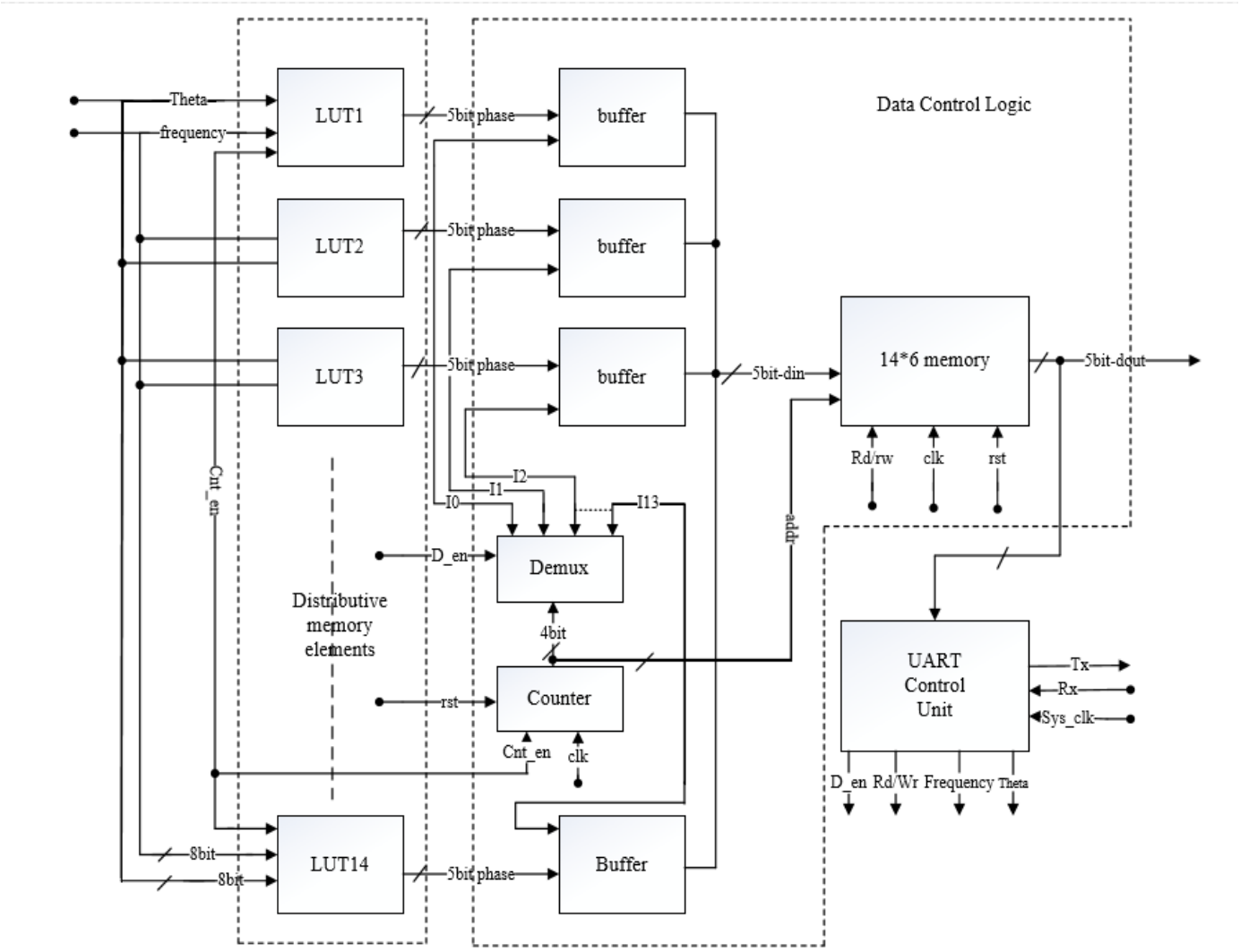

Fig1. **Block diagram for 14 element antenna array.**

Therefore this solution is adopted to design the distributive memory elements architecture in order to reduce the hardware complexity. LUT of size 45 x 6 bit stores the phase values which are pre-calculated to select phase shift settings for a given T/R module based on the received angles. Output from it is sent to buffer.

To activate the elements with phase values data control logic have been designed, consists of counter, demultiplexer and memory unit as shown in fig1. The output of the Lut gives the phase value that is stored in its memory by receiving the data from the control unit. After receiving the data counter enables cunt_en of 14 LUTs, each LUT consists of 4 blocks that stores the 5-bit phase values of particular angle for four different frequencies (F1,F2,F3,F4) and a demultiplexer is used for selection of block as illustrated in fig2.

The output of the counter is given as input to the demultiplexer which enables the buffer and memory as address. The output from buffer is given as input to the memory and finally phase value is obtained as the output which is represented as [5:0]dout.

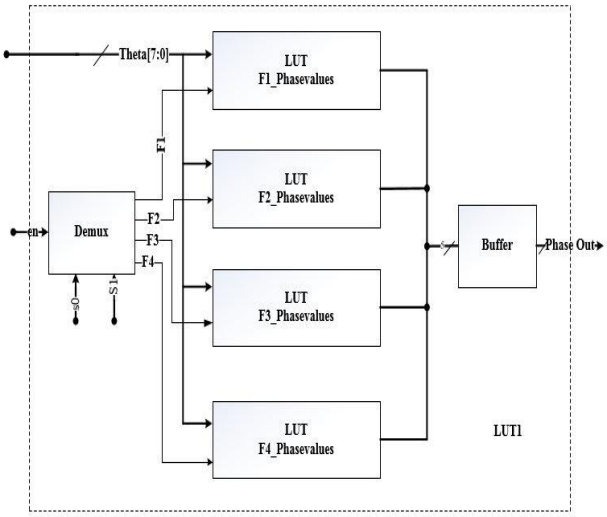

Fig2. Block diagram for single LUT in distributive memory elements

B. UART control unit

UART is a type of serial communication protocol. Transmitter that accepts the 8bit parallel data and the inputs of it are given to the transmitter control unit to obtain a string of data either to enter theta or frequency. Then the values of theta and frequency are received by the receiver that accepts the serial data, and finally output of it is given to the receiver control unit to obtain theta and frequency values. The architecture is designed with clock signals up to 100MHz with baud rate of 9600 kbps.

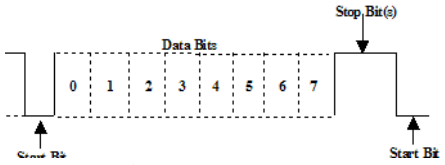

Fig3. Bit Frame

The proposed optimized for implementation on FPGA architecture to meet the area requirements. The described beam steering control system can be realized using a platform equipped with a single FPGA. In fact, the necessary I/O resources are easily provided by a single commercial off-the-shelf FPGA and also the implementation on a device should not present particular problems.
Tools used for the implementation of 14 element antenna array are given below.

- Matlab for the phase values generator.
- ISE for generating programming language logic.
- ISE simulator for functional simulation.
- Artix-7 FPGA for hardware implementation.

III. THEROTICAL ANALYSIS

Phase values for different angles and for different frequencies are calculated using the formula shown below. Here theta ranges from 0º to 45º, i define the number of antenna elements (i.e 1 to 14) and d is the spacing between antenna elements. The phase shifter offers a phase shift range of 0 to 360º with a phase shift resolution of 11.25º, operating in the 6,10,14,18 GHz frequency ranges.
Phase value calculation:

$$\text{Phase value} = (2\pi/\lambda) * dh * \sin(\text{tetha})$$

dh =0.96 cm (horizontal spacing between array elements)

$$\lambda = 30/f$$

f is the operating frequency

Calculated phase values for the phase shifters are stored in the look up tables, by loading the phase values to T/R modules to steer the antenna elements. The communication is done through the UART control unit to transmit and receive the frequency and angle values to load phase values to phase shifters from LUTs.

IV. EXPERIMENTAL RESULTS

1. Hardware Implementation:

The implementation for forming beam for 14 element antenna array is done on Artix-7 FPGA. The device utilization summary obtained in Xilinx ISE after the synthesis of the verilog HDL code is given in table 1.

Table1. Resource utilization for implementation of beam forming on Artix-7 FPGA.

Sr.No.	Slice Logic Utilization	Used	Available	Utilization
1	Number of Slice Registers	394	126,800	1%
2	Number of Slice LUTs	680	63,400	1%
3	Number of occupied Slices	253	15,850	1%
4	Number of bonded IOBs	28	210	13%
5	Number of BUFG	3	32	9%

2. Simulation Waveforms:

The programming is customized in verilog HDL language; all Simulations were done and verified functionally on Xilinx ISE design suit. The following figures show the final results achieved. The architecture can be controlled with the frequency up to 100MHz.

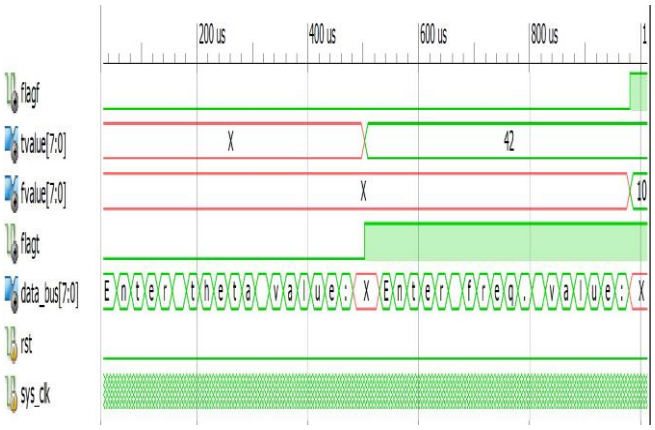

Fig4. Simulation waveform of UART control unit.

The simulation waveform of the UART control unit is shown in fig4. data_bus, tvalue and fvalue are the signals which indicate the successful transmission and reception of data words with respective to the given clock. T_byte is asserted initiates the stop and start bit in the word during the transmission.

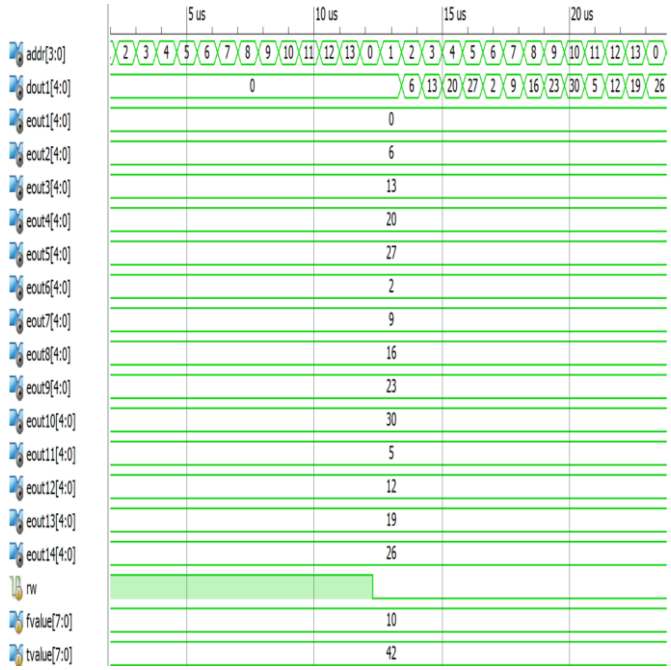

Fig5. Simulation waveform of obtaining and loading the phase values

The 5 bit phase values are stored in the LUTs that are to be loaded for the selected angle and frequency is shown in fig5. When flagf signal is enabled, the 14 LUTs are enabled with the data stored and send the output data through dout. The memory unit has been implemented to read and write the data which is stored in memory (14*6). When rw is '1' write is enabled and when rw is '0' read is enabled.

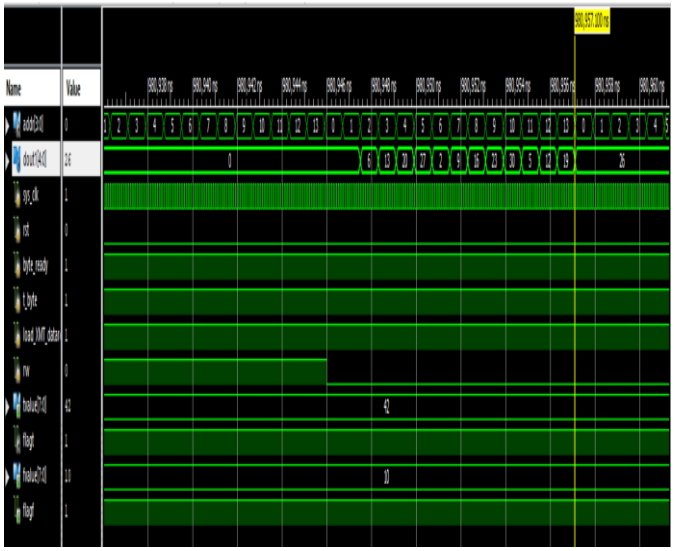

Fig6. Simulation waveform for proposed architecture

3. Computation Time:

Time taken to compute 5 bit phase value for an angle of single antenna element = 1*0.01μs=0.01μs.

Time taken to compute 5 bit phase value for an angle of 14 antenna array elements = (14*0.01μs) =0.14μs.

Total time taken to compute 5 bit phase value for 90 angles for 14 antenna array elements= (90*0.01μs*14) =12.6μs.

V. HARDWARE RESULTS

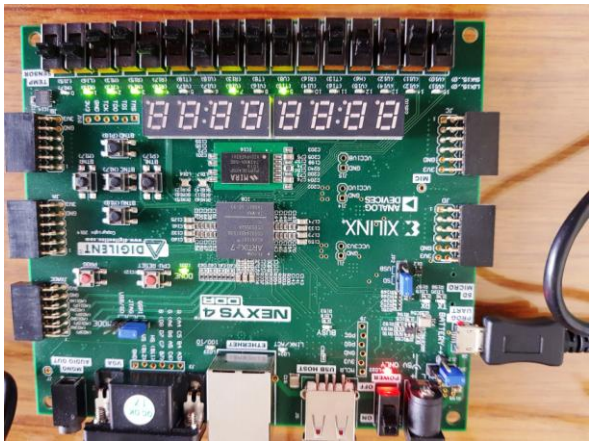

Fig7. Hardware implementation for proposed architecture.

VI. CONCLUSION

Proposed architecture is developed to achieve beam steering of 14 channel phased array radar consists of control unit and distributive memory elements. Data control logic was developed in order to perform continuous data flow from the developed system to the antenna elements. Hardware is implemented on Artix 7 FPGA, and its functionality is verified. From the results it is observed that the area occupied by the proposed architecture is 1% of FPGA slice registers. So the architecture can be extended further for more number of elements in a single FPGA which reduces the hardware area cost. So the design has an advantage of being flexible and fast switching time. Beam steering and scanning can be carried out in azimuth direction for radar applications.

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AUTHORS PROFILE

S.Ramya Sri from vijayawada Aandhra Pradesh, India. She received her B.Tech degree in the year 2016 from PVP Siddhartha Institute of Technology., Kanuru (A.P), India.
Currently pursuing M.Tech in V R Siddhartha Engineering college, Vijayawada (A.P), India. Her researches interests on Digital Design Circuits

Dr. Shaik Fayaz Ahamed He completed his Ph.D. in GPS signal processing. Currently he is an Associate Professor in V R Siddhartha Engineering College, Vijayawada (A.P), India. He completed his research projects as investigator in CARS – ANURAG –DRDO, Hyderabad -Rs9.5L and CARS Project - DLRL-DRDO, Hyderabad-Rs9.9L.His research interests on signal processing.

Dr. **A. Anitha** from Vijayawada, Andhra Pradesh, India. She completed her Ph.D in 2018 from JNTK . Currently she is an Assistant Professor in V R Siddhartha Engineering College, Vijayawada (A.P), India. Her research interests on VLSI system design and VLSI signal processing.

K Naga Sunanda from Vijayawada, Andhra Pradesh, India. She received her M.Tech degree in the year 2015 from VR Siddhartha engineering college, kanuru (A.P), India. Currently she is an assistant professor in V R Siddhartha engineering colleges. Her research interests in Digital Design, Low Power VLSI and Analog Circuit Design.