Design and Analysis of Gate All Around Tunnel FET based SRAM

Umesh Dutta, M.K Soni, Manisha Pattanaik

Abstract: ***Tunnel FETs (TFETs) possess all required characteristics for replacing MOSFET device in circuits with stringent requirements particularly for Internet of Things (IoT) and Biomedical applications. In particular Gate-All-Around (GAA) TFET device configuration exhibits higher ION/IOFF ratio and strong control of the gate terminal over the channel. The main objective of this research work is to explore the prospects of using GAATFET device topology for designing low power and reliable SRAM cell. In this work both n-type and p-type Tunnel FET devices have been designed and simulated using Cogenda Visual TCAD tool. Verilog-A model relying on look up tables that are extracted through device simulations has been designed for performing circuit simulations of 6T and 8T SRAM cell involving these novel devices. Device simulation results show that both NTFET and PTFET devices exhibits excellent ION/IOFF ratio and steep subthreshold slope. NTFET device simulation results show 21.2 mV/decade of subthreshold slope and ION/IOFF ratio of 10^{13}. PTFET device has ON current of the similar order as that of NTFET and has extremely low value of OFF current of less than 1 pA. Circuit simulation results show that by using optimized sizing of transistors in outward NTFET access transistor based 6T SRAM cell leads to reliable and fast read and write operation with acceptable values of noise margin. 6T TFET based SRAM cell achieves leakage power reduction by 77.5% in comparison to leakage power consumed by 8T TFET based SRAM thereby making it a favorable choice for memory design.***

Index Terms: ***Subthreshold Slope, Miller Capacitances, Leakage Current, Ambipolarity, BTBT model, Static Random Access Memory (SRAM), Leakage Current.***

I. INTRODUCTION

Interband tunneling transistors have shown the promise of replacing MOSFETs in designing the low power memory circuits. These transistors have the inherent property of having extremely low value of the OFF current [1]. Low value of OFF current can lead to a good amount of power saving in the memory cells that are operating in the standby mode. Memory occupies most of the on-chip area of the processor and power saving in this module can lead to better power performance of the overall system. These devices can prove to be extremely useful for IoT and biomedical applications which have strict power budgets ranging from 3 mW to 19 µW for the devices which are operated through a battery or from the harvested energy [2]. TFETs have overcome the bottleneck of 60 mV/decade on the subthreshold slope which is a major issue in the MOSFETs operating at room temperature [3]. Besides these merits, TFETs suffer from several issues which include: poor ON current, ambipolarity and unidirectional conduction. The problem of poor ON state current has been solved by fabricating TFETs using lower energy band gap materials, for example: InAs, Ge and III-V semiconductor materials [4, 5]. Various researchers had proposed device engineering techniques which aims at improving the TFET device performance through modifications in the conventional device structure. Boucart et al. [6] had proposed a double gate TFET device which utilizes dielectric material with high dielectric constant for enhancing the ON state current of the TFET device. Jhaveri et al. [7] had proposed pocket doping approach which leads to increase in the electric field across the tunnel junction thereby leading to increase in the ON state current of the device. Vertical TFET and STBFET devices also have improved ON current than the conventional TFET device structure [7, 8]. Ambipolarity issue has been addressed by either using lightly doped drain in comparison to source region or by using underlap between gate and drain region [9,10]. Circuit designers face lot of challenges particularly due to the unidirectional conduction property of TFETs and mere replacement of MOSFET with TFET in a circuit will not be enough. Circuit topologies needs to be modified so as to achieve the correct logic functionality at the circuit level. In particular for the SRAM implementation various researchers had proposed different circuit topologies based on TFET device which are robust and provide reliable read and write operation without much area overhead [11,12,13]. Rapid advancement in the fabrication technology has led to good results in terms of manufacturing these novel devices and experimental data published by various research groups signify that TFETs can be the future device for replacing MOSFETs particularly for low power applications. Gate all around TFET topology are almost also immune to short channel effects (SCEs) and also have superior channel control as compared to other TFETs topologies [14]. Experimental data published shows that these devices can provide high ION/IOFF ratio and less than 60 mV/decade subthreshold slope. These devices have superior analog and RF performance thereby making them an ideal candidate for designing high frequency applications like amplifier [15]. The aim of this work is to investigate the feasibility of using the gate all around TFET devices in designing low power SRAM. The remaining paper is structured as follows: Section II highlights the architecture of proposed GAA-TFET device. The simulation flow followed for carrying out device and circuit level analysis has been discussed in Section III. It also elaborates the process of extracting Verilog-A model for TFET devices. Section IV describes implementation of SRAM cell using TFETs particularly focusing on outward NTFET access transistor based 6T SRAM and 8T transmission

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gate-based SRAM cell designs. Section V presents comparative analysis of 6 transistor and 8 transistor based TFET SRAM cells on the basis of stability, timing information and leakage power dissipation. Timing information is extracted by calculating the read and write time of SRAM cell. Section VI presents the conclusions of the research work.

II. ARCHITECTURE OF GATE ALL AROUND TUNNNEL FET

In Gate All Around (GAA) tunnel FET device, the gate metal covers the entire channel region which leads to excellent control of channel electrical characteristics. In this work we have used three different materials for the gate terminal with different work functions in order to achieve better control over the band bending across the tunneling junction and also the in-channel barrier. In the proposed TFET device configuration a high K dielectric material is used under the gate metal M1 and SiO_2 is used in the remaining region i.e. under M2 and M3 region. This causes an increase in the ION value of the tunneling device. Source and drain region doping are kept asymmetric so as to suppress the ambipolar conduction in TFET device. Table I highlights various important device parameters that are used for designing both NTFET and PTFET devices in Visual TCAD tool. PTFET device is designed with the silicon core radius value of 20 nm and high K dielectric with dielectric constant of 21 is used. In order to match the transfer characteristics of both NTFET and PTFET devices few modifications are done in the PTFET device which includes introduction of gate source underlap of 4 nm and tuning the work function of three metals used for the gate. Fig.1 shows the device architecture of NTFET device showing its various important regions. The working of the device can be understood as follows: At zero gate bias and positive drain source voltage the energy barrier height blocks the charge carrier movement across the tunnel junction keeping the IOFF value to extremely low level. Increase in the gate to source voltage leads to both band bending and band gap narrowing which enhances the tunneling probability across the source-channel interface thereby leading to increase in the drain current [16]. The energy band diagram of NTFET device at two different Vgs voltage values (Vgs = 0V and Vgs = 0.5V) is shown in Fig.2. Here the drain source voltage is kept fixed at 1V. The ON current in TFET strongly depends on the material used for device fabrication. The prime reason for enhancement in the ON current by introduction of high K dielectric under gate metal M1 is enhancement in the magnitude of electric field's lateral component that exists across tunnel junction. The enhancement in the magnitude of lateral electric field reduces the energy band gap thereby causing an increase in the drain current.

Table I. Device parameters for NTFET and PTFET

Parameter	NTFET device	PTFET device
Source Doping Concentration	1e20 {p-type}	1e20 {n-type}
Drain Doping Concentration	1e17 {n-type}	1e18 {p-type}
Intrinsic Channel Doping Concentration		
Gate Length (nm)	60	60
Oxide Thickness (nm)	2	2
Work Function of Gate represented by ϕ_1, ϕ_2 and ϕ_3 (eV)	4.4, 4.8, 4.6	5.0, 5.4, 5.2
Radius of Silicon Core (nm)	8	20
High K Dielectric Constant in the source channel region	7.9	21
Gate Source Underlap (nm)	0	4

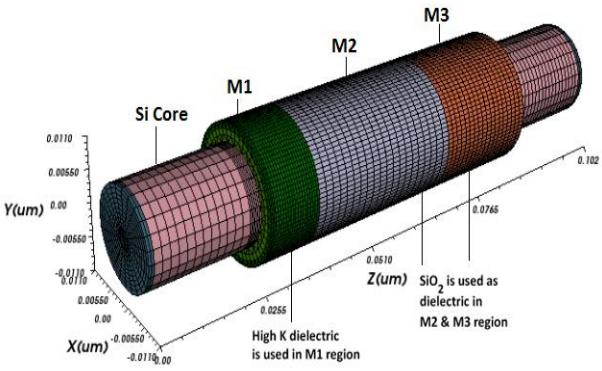

Fig.1. Proposed NTFET device (HD-TMGTFET) in GAA topology

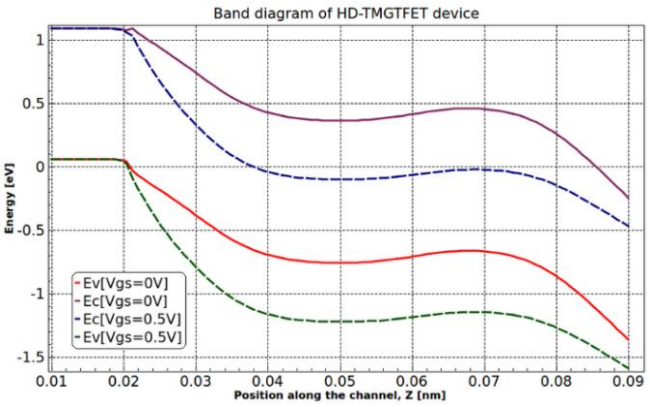

Fig.2. Band gap energy profile at different Vgs values for N-type HD-TMGTFET device

Device simulations have been carried out using BTBT model proposed by E.O. Kane. This model considers the fact that electric field is uniform in the entire tunneling region. This model is fairly accurate and particularly well suited for designing gate all around devices without much convergence issues which may come into picture when the devices are simulated using non-local tunneling model. The other models that are also invoked during the simulation includes: Fermi Dirac statistics and SRH model. According to Kane's BTBT model as discussed in [17], the BTBT generation rate/volume is given by-

$$G^{BB} = A.BTBT.\frac{E^2}{\sqrt{E_g}}\exp\left(-B.BTBT.\frac{E_g^{3/2}}{E}\right) \quad (1)$$

where E is electric field, A.BTBT, B.BTBT represents Kane's parameters. Here symbol E_G represents energy band gap. Kane's parameters are tuned to match the experimental data published in [18]. The drain current Id is obtained using the G^{BB} parameter extracted using equation (1).

$$I_{ds} = q\int G^{BB} dV \quad (2)$$

It is important to note here that device matching is extremely crucial for digital application circuits like SRAM as device mismatch may lead to read and write failure. Fig.3 shows the transfer characteristics obtained for NTFET and PTFET device designed and simulated as per the details given in Table I. Both these devices exhibit extremely low OFF current of less than 1pA and high ON current in the µA range. It is clear from Fig.3 that TFET has unidirectional conduction which means that it is not possible to interchange the source and drain terminals as it is in case of a MOSFET device. TFETs have extremely low value of current under reverse bias condition which indicates that the device remains in the OFF state when reverse voltage is applied at gate source terminals.

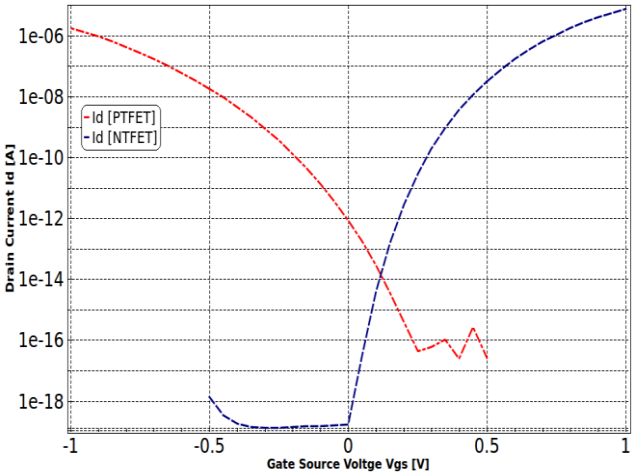

Fig.3. Transfer characteristics of NTFET and PTFET device

III. SIMULATION FLOW AND VERILOG-A MODEL

This section presents the simulation flow that is used for carrying out both the device and circuit level simulations involving gate all around tunnel FET devices. Unavailability of compact model leads to difficulty in performing TFET device-based circuit simulations. In order to perform circuit simulations involving TFET device, researchers have relied on the Verilog-A model that makes use of look up tables extracted through device simulations. The Verilog-A model based simulation approach is widely followed to simulate the emerging devices for which no validated compact model is available. Fig.4 shows the simulation flow that is followed in this work. It is clear from Fig.4 that device simulation is first carried out on the Visual TCAD tool to extract important parameters that are used for developing Verilog-A model which includes: capacitances (C_{GS} & C_{GD}) and drain current (I_{DS}). The Verilog-A model has been used in SPICE tool for performing simulations of different benchmark SRAM circuits. The output waveforms are visualized in the Symprobe tool and further data analysis and plotting is done using MATLAB tool. In order to extract the look up tables from device simulations it is important to first understand the work flow of the Visual TCAD tool. Fig.5 shows the schematic diagram of the Visual TCAD workflow that is used for simulating both NTFET and PTFET devices. The device is created by writing a script which is saved in .inp format and various models are invoked in the simulation which includes mainly: BTBT model, Mobility model and SRH model. The device script contains the definition of the device which includes different regions, material parameters and bias voltage that are applied to different electrodes. Meshing plays a very important role and it should be dense near the tunneling junction to analyze the tunneling of charges at the source-channel interface. Different output files are created by Cogenda Genius device simulator which are analyzed to see the energy band profile, device structure and output waveforms. A tabular template is shown in Fig.6 that can be easily used in the model designed using Verilog-A language. Device capacitance and transfer characteristics are used to extract the tables as shown in Fig.6. This tabular information is used in Verilog-A code that is invoked in the SPICE tool for simulating TFET based SRAM cell. A sample template of the Verilog-A code for performing dc as well as transient simulations of the TFET device is highlighted in Fig.7. The equivalent circuit of verilog-A model is shown in Fig.8. This clearly signify that the parisitic resistance and capacitance are not included in the model but they can be incorporated in the SPICE code. Drain charge ($Q_{gd} = C_{GD}V_{GD}$), source charge ($Q_{gs} = C_{GS}V_{GS}$) and voltages (V_{GS} and V_{GD}) are used in the trasient analysis. DC characteristics of the tunneling device are determined through idvg.tbl file. Device width parameter W can be varied in the simulation for analysis of SRAM circuit for obtaining optimal performance from read and writeability point of view.

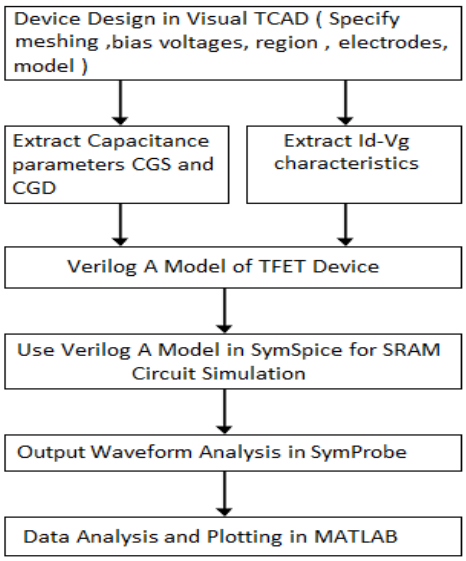

Fig.4. Simulation flow diagram

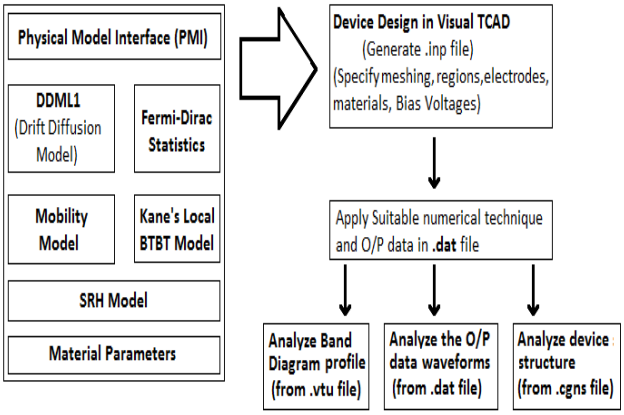

Fig.5. Schematic of Visual TCAD workflow

V_{DS}	V_{GS}	I_{DS}
……	……	……
……	……	……

V_{DS}	V_{GS}	C_{GS}
……	……	……
……	……	……

V_{DS}	V_{GS}	C_{GD}
……	……	……
……	……	……

Fig.6. Table based template for use in Verilog-A model

```
parameter real W=1;// W is device width parameter
analog begin
Ids=$table_model(V(d,s), (V(g,s)), "IdVg-NTFET-Si.tbl","1LL,1LL");
Cgd=$table_model(V(d,s), (V(g,s)), "CGD-NTFET-Si.tbl","1LL,1LL");
Cgs=$table_model(V(d,s), (V(g,s)), "CGS-NTFET-Si.tbl","1LL,1LL");
if(analysis("dc")) begin
I(d,s) <+ 1*Ids*W;
end
else begin
if(analysis("tran")) begin
Qgd = (W*1*Cgd)*(V(g,d));
Qgs = (W*1*Cgs)*(V(g,s));
Qg=Qgs+Qgd;
I(d,s) <+ 1*Ids*W ;
I(d) <+ ddt(1*Qgd);
I(s) <+ ddt(1*Qgs);
I(g) <+ ddt(-1*Qg);
end
```

Fig.7. Sample Verilog-A code for NTFET device

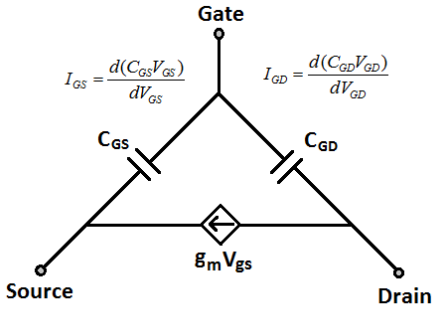

Fig.8. Equivalent circuit diagram of Verilog-A model

IV. TFET BASED SRAM CELL DESIGN

Tunnel FET is a unidirectional device and due to this it becomes difficult to get the access of the internal data storage nodes using a single TFET device during both read and write operation. Various options that can be considered for the implementation of 6T TFET based SRAM cell are shown in Fig.9. Various researchers in the have shown that it is not possible to implement TFET based symmetric 6T SRAM cell. Strangio et al. [19] has proved that by choosing the proper cell sizing it is possible to achieve reliable read and write operation in case outward access transistor is used. Outward access transistors can be used in 6T SRAM cell in case the architecture allows both BL and BLB lines to be clamped at 0V instead of the supply voltage VDD during hold operation. Various alternative implementations of TFET based SRAM cell had been proposed which includes: 8T transmission gate-based SRAM cell, Schmitt trigger-based SRAM [20], 7T TFET SRAM cell, 7T Driver Less TFET SRAM [21]. Successful demonstration of TFET-MOSFET based SRAM cell that makes use of write assist technique has been presented in [22]. All these configurations have proved to be effective in providing robust read and write operation without much performance overheads. In this section the effectiveness of the HD-TMGTFET devices proposed in section II for the implementation of two benchmark configurations namely: 8T TG based SRAM and O-AT based 6T SRAM has been explored.

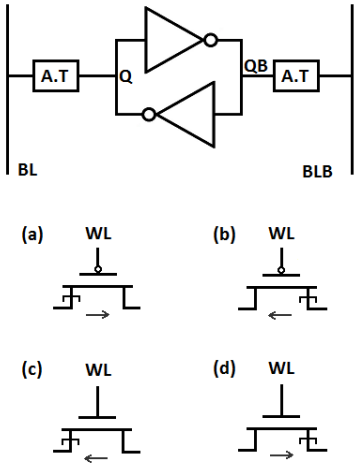

Fig. 9. Different option for access transistors in 6T SRAM cell Inward-PTFET (b) Outward-PTFET (c) Outward-NTFET (d) Inward-NTFET

Fig.10 shows the implementation of 8T-TG based SRAM cell which can provide reliable read and write operation.

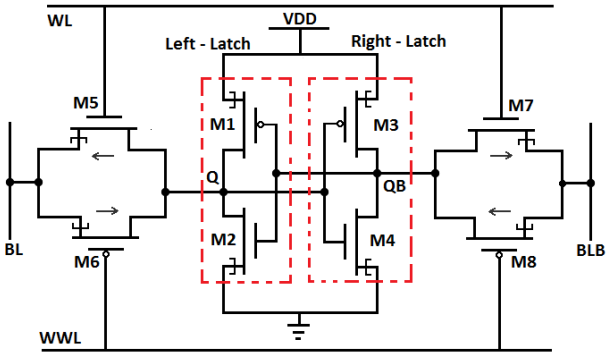

Fig.10. 8T-TG based SRAM cell

It is clear from Fig.10 that both inward (M6, M8) and outward (M5, M7) TFET based transistors are used to get access of the data storage nodes Q and QB. For performing the write operation both WL and WWL lines are enabled. For example: Assume that initially node Q stores logic '1' and node QB stores logic '0' and it is required to write logic '0' into the cell. When both WL and WWL lines are enabled then transistor M5 tries to pull down the node Q to logic '0' and transistor M8 supports the write operation by pulling up the voltage of node QB which ultimately leads to improved write delay. Read operation is performed by enabling only the inward access Tunnel FETs (M6 & M8). Read operation can be achieved by enabling only the WWL line and pre-charging both bit line and bit bar lines to VDD. If the cell is storing a logic '0' at node Q then BL will discharge from VDD and the voltage at BLB remains almost same since node QB stores logic '1'. When sufficient voltage difference is generated between BL and BLB lines then the sense amplifier gets triggered. Current mode sense amplifiers are preferred in SRAM cells as compared to voltage sense amplifiers primarily because of the fact that they have better signal sensing speed which is independent of the bit line load capacitance. Fig.11 and Fig.12 shows the simulated waveforms corresponding to read & write operation of 8T-TFET SRAM cell.

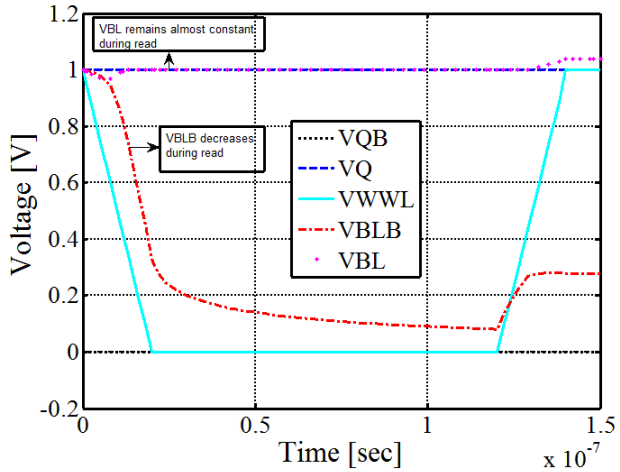

Fig.11. Simulated waveforms of 8T-TMGTFET SRAM during read operation when both bit line (BL) and bit line bar (BLB) lines are pre-charged to voltage VDD.

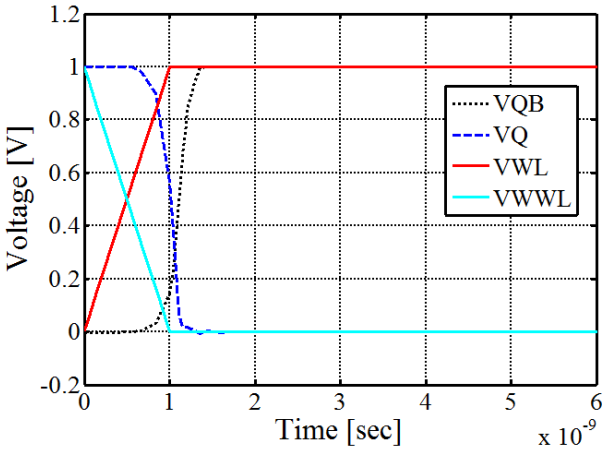

Fig.12. Write operation waveform 8T-TGTFET SRAM Cell

Fig.13 shows the circuit topology of six transistor based TFET SRAM cell designed using outward NTFET as access transistors. As we have used (W5/W2) and (W6/W4) ratio of 2.0 for achieving acceptable read and noise margins. The only limitation that comes while using outwards NTFET device as access transistor is that it can not achieve the read operation correctly with both bit and bit bar lines precharged to the supply voltage. Read operation is performed correctly when both bit line and bit bar lines are precharged to the voltage level of VDD/2 and then activating the WL signal. Fig. 14 and Fig.15 shows the simulated waveforms for SRAM cell read and write operation respectively. SRAM cell write operation is performed by applying proper voltage levels at BL and BLB lines before raising the word line signal (WL). This configuration does not require any addition of extra transistor for achieving reliable read and write operation.

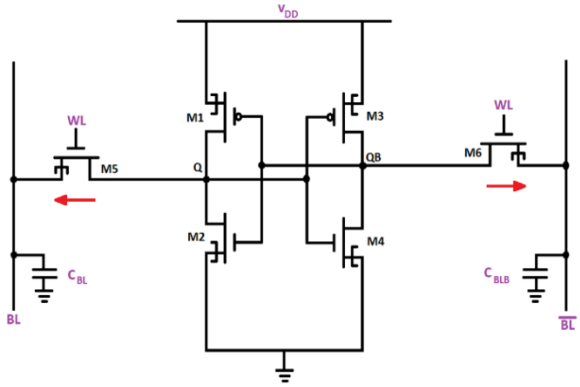

Fig.13. 6T TFET SRAM cell using outward NTFET as access transistors

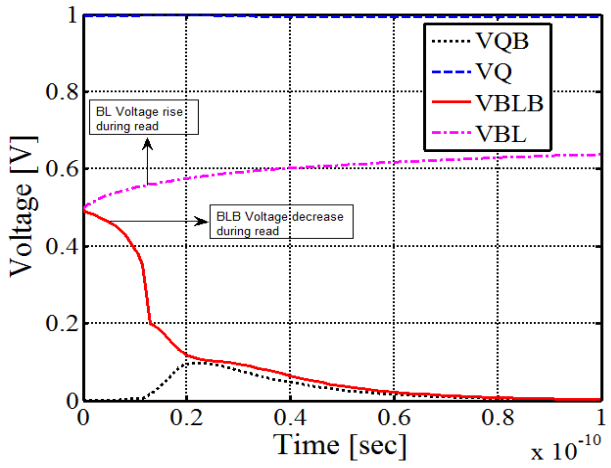

Fig.14. Read Operation in outward access transistor based 6T SRAM cell with bit line pre-charged to VDD/2

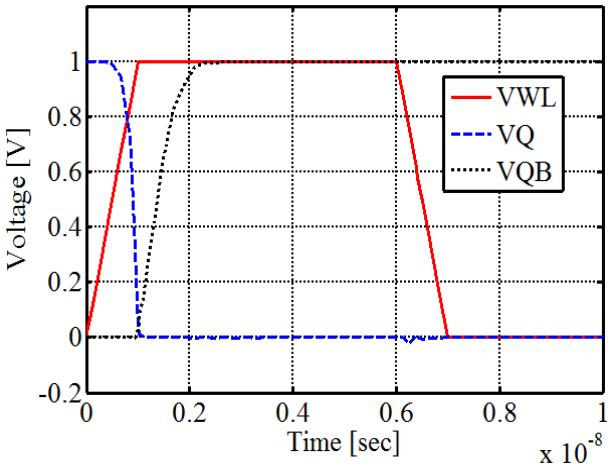

Fig.15. Write '0' waveform of outward access NTFET based 6T SRAM Cell

V. COMPARATIVE ANALYSIS OF 6T AND 8T SRAM CELL

This section elaborates the findings of the comparative analysis of the performance of both 6T and 8T TFET based SRAM cells. The analysis is done keeping in view various important parameters of SRAM cell such as: stability, timing information and leakage power dissipation. Stability is determined by calculating the noise margins, timing information is extracted from read and write delay. Leakage power dissipation is calculated when WL signal is in the inactive state.

Stability Analysis

It is extremely important to critically examine both 8T and 6T TFET based SRAM cell from stability point of view considering: read, write and hold stability. Static Noise Margin (SNM) parameter is an indicator of the stability of the SRAM cell and it is calculated by finding the maximum amount of noise voltage that can be introduced at the outputs of two inverters such that the cell retains its data [23]. SNM can be calculated graphically by plotting the voltage transfer characteristics (VTC) of left latch and inverse VTC of right latch. This combined VTC plot is commonly known as butterfly curve and SNM is calculated by finding the length of the largest square that can be inscribed inside the two lobes of butterfly curve. Fig.16 shows the butterfly curve obtained from the simulation of 8T TFET based SRAM cell.

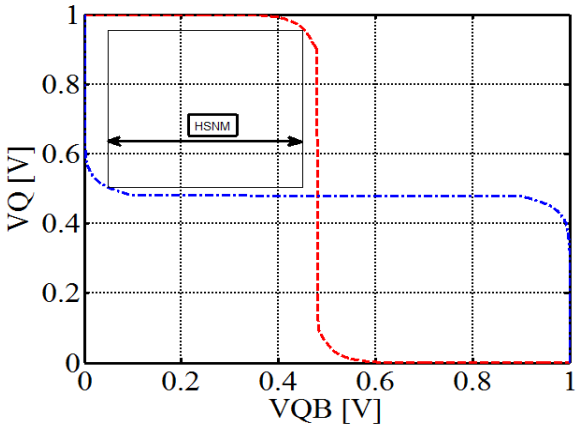

Fig.16. Hold SNM plot for 8T TFET SRAM cell

Hold SNM is calculated using butterfly curve by keeping WL signal in the inactive state. HSNM for both the SRAM cell configurations considered here are almost same as the cross coupled inverters have transistors which are of same strength. HSNM in case of 8T SRAM is 0.48 V while its value is 0.47 V for 6T SRAM cell. Write-ability of SRAM cell is analyzed by finding the write margin which is determined as follows: Assuming that the SRAM cell initially stores logic '0' and it is required to write logic '1' into the cell. The cell is configured in the write mode where BL voltage is raised to logic high and voltage at BLB line is swept from VDD to GND during simulation. The BLB voltage at which the stored contents of the cell get flipped is known as write margin [24]. Lower value of write noise margin signify that it is difficult to write the SRAM cell. Fig.17 and Fig.18 shows the simulated waveforms obtained for 8T and 6T SRAM cells respectively.

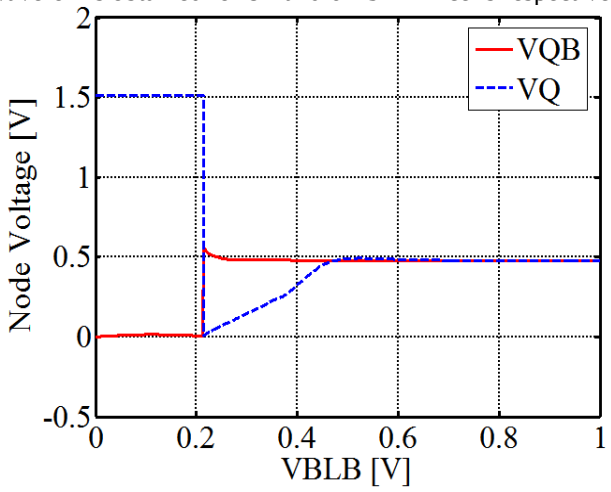

Fig.17 Write margin in 8T TFET SRAM is the BLB voltage at which stored data in the cell gets flipped

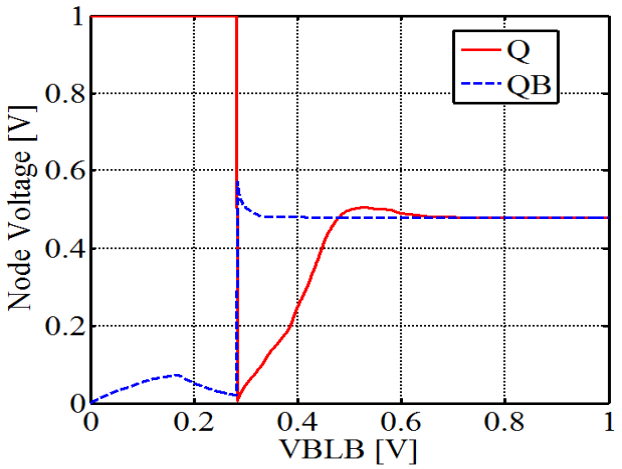

Fig.18 Simulation waveforms for WM calculation in 6T SRAM cell

Write Margin for 8T TFET SRAM cell is 0.214 V while for outward access transistor based 6T-SRAM its value is found to be 0.282 V. This analysis reveals that it is harder to write the 8T SRAM cell in comparison to 6T SRAM cell. Now in order to analyze the cells from readability point of view the read margin is calculated using the setup shown in Fig.19. Read Margin in case of outward access transistor based 6T-SRAM cell is calculated by inserting two noise sources at the internal storage nodes. The noise voltage is varied and read SNM is the noise voltage at which the contents of the internal storage nodes gets flipped [25]. Read SNM for 6T SRAM cell is found to be 0.44 V and its value is 0.45 V for 8T SRAM cell. Read SNM of 8T SRAM cell is calculated using the same method as described for 6T SRAM cell. Higher value of RSNM shows that both the cells are capable of performing robust read operation.

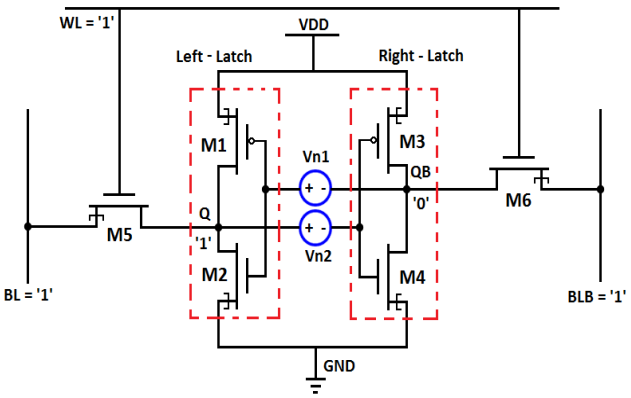

Fig.19. Setup for calculating read margin of 6T SRAM cell

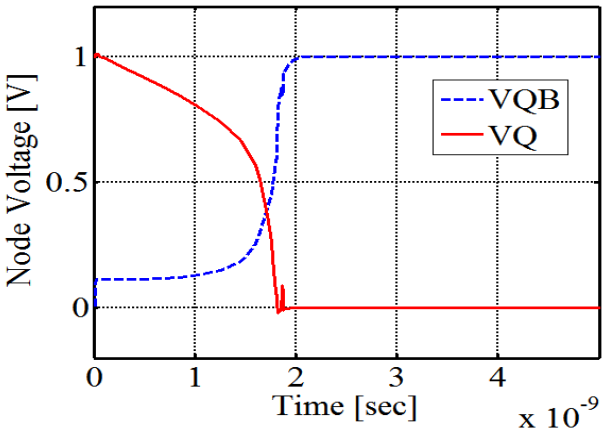

Fig.20. Simulated waveform showing internal storage node voltage flip during read operation

a. Timing Information

Timing information is extracted by calculating the SRAM cell read and write delay [25]. Read delay is the time delay between 50% of the WL activation to the time when the voltage difference between BL and BLB lines reach 10% of its pre charged value. On the other hand, write delay is the time interval between the 50% activation of the word line (WL) to when the internal data storage node Q is flipped to 90% of its full swing. Read delay for 6T SRAM cell is found to be 9.57 ps while for 8T SRAM cell its value is found to be 9.9 ps. The write delay calculation shows that write delay improves by 30.25% for 8T SRAM cell in comparison to 6T SRAM cell.

b. Leakage Power

In case of processors when there is no activity going on, the SRAM cell goes to standby mode so as to minimize the overall power consumption. It is required that the device used for designing SRAM should consume less amount of power in the standby mode which ultimately leads to optimization in the overall power consumption of the memory cell. Here a comparison is made between the leakage power consumption of the conventional 6T and 8T TFET based SRAM cell both operating in the standby mode. Tunneling devices are known for their extremely low OFF current and this is an inherent advantage over conventional MOSFET device. Simulations are carried out at 1V supply voltage and results show that 6T TFET based SRAM cell can provide 77.5% saving in terms of the leakage power in comparison to 8T TFET SRAM cell. These results convey that TFET devices can provide excellent power performance and despite the challenge of unidirectional conduction it is a promising choice for replacing conventional MOSFETs in the memory applications. Table II summarizes the results of the comparative analysis performed on 8T and 6T SRAM cells.

Table II. Performance Comparison Table

Circuit Topology	Leakage Power [pW]	Read Delay [ps]	Write Delay [ns]	RSNM [V]	HSNM [V]	WSNM [V]
6T TFET SRAM Cell	0.3915	9.57	1.35	0.44	0.48	0.282
8T TFET SRAM Cell	1.74	9.9	0.9416	0.45	0.47	0.214

It is evident from the observations made in Table II that 6T SRAM cell outperforms 8T SRAM cell on leakage power dissipation parameter and it also possess better write ability. There is not much significant difference observed in the HSNM, RSNM and read delay values, however 6T SRAM takes more time to write to the cell in comparison to 8T SRAM cell.

VI. CONCLUSION

It is clear from the simulation results that GAATFET device can be used for designing SRAM cell that consumes less area and also consumes low power. The unidirectional conduction in TFET device has been a challenge for the memory designers as it forces the designer to either opt for the new SRAM topologies with higher number of transistors and separate bit lines for read and write operation. Simulation results show that using NTFET as access transistor and carefully choosing the cell ratio can lead to reliable read and write operation with 77.5% leakage power reduction in comparison to 8T transmission gate-based SRAM cell. The sizing of the transistors in SRAM cell is very important factor that significantly affects the performance of the SRAM cell. Literature supports the fact that cell ratio of 2.0 leads to reliable operation with good read and write margins respectively. The only limitation with 6T TFET SRAM cell is that both BL and BLB lines are pre-charged to half the supply voltage (VDD/2) for read operation and this requires a bit of modification in the pre-charge circuitry involved with SRAM cell. 6T TFET SRAM cell exhibits better write noise margin, similar read and hold noise margins as compared to 8T TFET SRAM. Timing analysis results show that both the TFET SRAM cells are extremely fast in performing read and write operation with read delay of the order of few pico-seconds and write delay of the order of nano-seconds. However, 8T TFET SRAM exhibits 30.25% improvement in write delay as compared to 6T SRAM cell. The future work will focus on the analysis of the TFET based SRAM cell from ageing degradation point of view.

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