Design and Implementation of Scalable Beam Steering Control System for Phased Array Radar

K. V. S. Siva Prasad, R. V. H. Prasad, A. Anitha

Abstract*: *Transmit/Receive (T/R) modules plays important role in advanced phased array radar system consists of array of antenna elements. In order to produce beam pattern for multiple radiating elements, the phase angle for each T/R module should be assigned with calculated value. When phase gradient is sent to T/R unit, phase values are calculated for array of elements associated with them. The paper presents a beam steering control system architecture consists of Graphical user interface, group controller with scalable T/R control unit (TRCU) having two hexa decagon T/R module controllers (HTRMCs) and control logic unit for parallel data flow. Calculation of 6 bit phase value from the phase gradient carried out using FPGA. Also, use of logic core and quantization of phase values are discussed. The paper also reports the area factor for the proposed architecture.

Index Terms*: *Transmitter/ Receiver module (T/R), HTRMC (Hexa decagon T/R module controller), T/R control unit (TRCU), data logic controller.

I. INTRODUCTION

RADAR is an initial system for detecting objects. It uses radio waves to determine the range. As earlier, to steer the beam mechanical positing of large and heavy antenna is needed, to overcome this disadvantage phased array antenna is used to scan a beam electronically in particular angle by changing its phase of each radiating elements. Behind to radar, phased array antenna is composed with group of individual radiating elements that are controlled by T/R module. Each of it consists radiating element provides beam steering. In phased array radar, beam steering unit plays an important role to steer the beam electronically in particular direction. The importance of active phased array antenna lies in the high speed beam switching from one direction to another direction with effective T/R modules. In addition T/R modules can provide wider band width and higher average transmit power. The beam forming unit of active phased array radar carries the phase angle to all radiating elements. Digital beam former consists of spatial filtering of a signal where beam phase shifting amplitude scaling and phase values are implemented digitally. It can accomplish minimization of side lobe levels, interference canceling and multiple beams operation without changing the physical architecture of the phased array antenna. In order to from a beam, each T/R module must be assigned with specific phase shift value. If the different values sent individually to T/R modules, beam switching will be delayed due to the transmission of multiple command words spanning over few seconds duration. This paper discusses about calculating and assigning phase angle to each T/R module in which phase angles could be calculated at each T/R module level with corresponding phase gradient for azimuth angle sent from the user. The architecture is developed for 32 T/R modules of 6bit phase value.

II. ANTENNA ARRAY DESIGN

Due to the threat environments, requirement for target detection have driven designers to use active phased array antennas. In active phased array antennas the amplitude can be generated either by the T/R module or at the receive beam former. In the proposed architecture, the antenna array is designed for 4480 radiating elements. Each radiating element is implemented in a T/R module. The antenna array is sub divided into two parts one is upper and the other is lower. Each sub array consists of 70 TRCUs that are having 14 TRCUs controllers. Each TRCU consists of two hexa decagon T/R module controllers (HTRMC). HTRMC controls sixteen antenna elements. For adapt individual controlling mechanism, the antenna array is sub divided. In an antenna array each radiating element can be identified by two coordinate representations. (a,b). ‘a’ represents the TRU control unit number varies from -70 to +70 and ‘b’ represents radiating element number varies from -16 to +16. The upper radiating element varies from +1 to +16 and the lower varies from -1 to -16. Let us consider, (45,-5) represents the element corresponding to 45^{th} T/R controller unit and 5^{th} T/R module of lower HTRMC.

A. *System Architecture*

The overall system architecture is discussed about beam steering control system design. Conceptually, the entire system is designed with four distinct subsystems. Namely, front end graphical user interface, group controller, T/R unit and control logic unit. Beam steering controller plays prominent role for electronically scanned active phased array radar.

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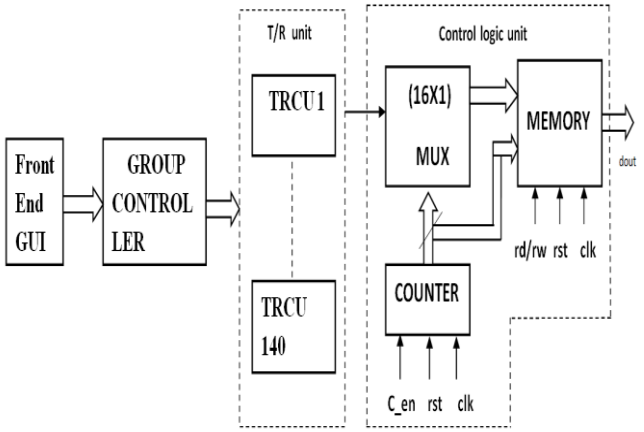

Fig1. Beam steering unit of the distributed architecture in active phased array radar.

Since, the phase values have to be sent to the phase shifters from all T/R modules, group controller establishes communication between graphical user interface (GUI) and the T/R unit controllers. However, the calculation of the phased gradients is developed at the front end GUI that is sent to the T/R unit. Group controller establishes the communication between GUI and TRU unit. UART is used for communication interface between GUI and group controller with baud rate 9600 kbps. After receiving the phase gradient (Pg) value, HTRMC calculates 6bit phase values that are sent to the digital phase shifters that convert the digital phase value to corresponding analog phase values for further beam forming. The 6bit phase value is calculated and is controlled by the control logic unit for continuous flow of data.

B. *Control Logic Unit*

The HTRMC of sixteen 6 bit phase output is controlled by the control unit that consists of (32*1) multiplexer and 5bit counter. The output of the counter is taken as input for the multiplexer as selection lines and memory as address. Output of multiplexer is given as input to the memory. When phase gradient is received by the T/R unit from group controller, counter gets enabled and enables the logic unit. 'rw' signal in memory indicates the data read and write. When 'rw' is '1' memory reads the data and when 'rw' is '0' memory writes the data. Finally, 6 bit dout is obtained. In the existing work [1], five T/R modules of each 6 bit phase values are implemented in single FPGA which consists of 30 pins and the same can be implemented to maximum of 10 T/R modules because of having 50 to 60 I/O pins. By increasing the number of T/R modules requirement of FPGA's also increases that occupies more area and hardware cost. To overcome the disadvantage, control logic unit is developed for parallel 6 bit data out.

C. *Phase Gradient Calculation*

The phase gradient is calculated at the developed front end GUI. Pg is calculated with elevation angle to steer the beam and is calculated by the following standard formula.

$$Pg=(2\ \pi/\lambda) * dh* \sin (theta)$$

Where,

theta = azimuth angel in degree varies from -90 º to +90 º.

λ= operating wavelength in cm.

dh=horizontal spacing between T/R modules in m.

Pg= phase gradient.

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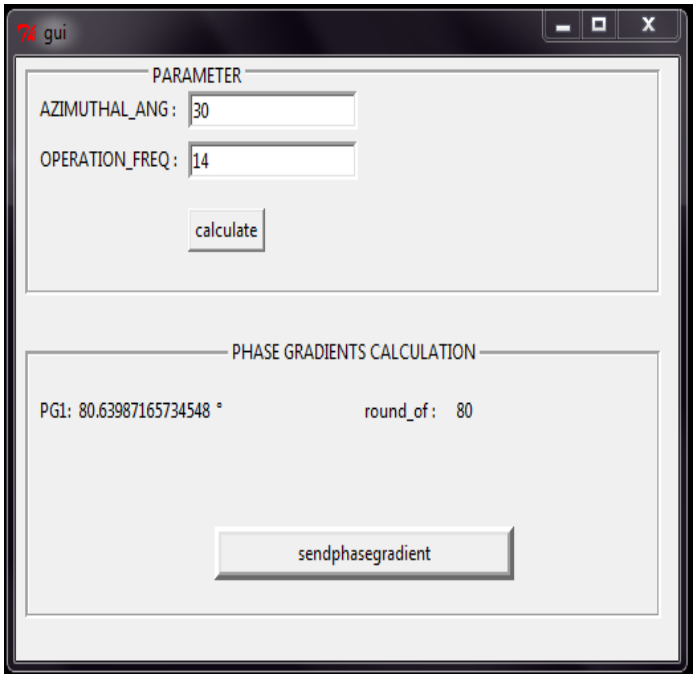

Fig2. Front end GUI.

The parameter frame of GUI consist of azimuth angle varies from -90 to +90 and operating frequencies of (6, 10, 14, 18). After entering the values, calculate button in the GUI is clicked. The calculated phase gradient and round of value is developed at phase gradient frame. As soon as completion of the calculation, send phase gradient button is clicked for transmission of calculated phase gradient value to the group controller.

D. *Phase* angle calculation at HEXA DECAGON T/R modules from phase gradient

The 6bit phase angle calculation from the phase gradient is carried to all HTRMC by the following formula.

Phase product= (a + b) * pg.
Where a = TR controller unit number.
b = HTRMC number.
Pg, phase gradient received from the group controller.

The algorithm for 6bit phase value calculation of HTRMC from phase gradient is shown following block design consists of five steps.

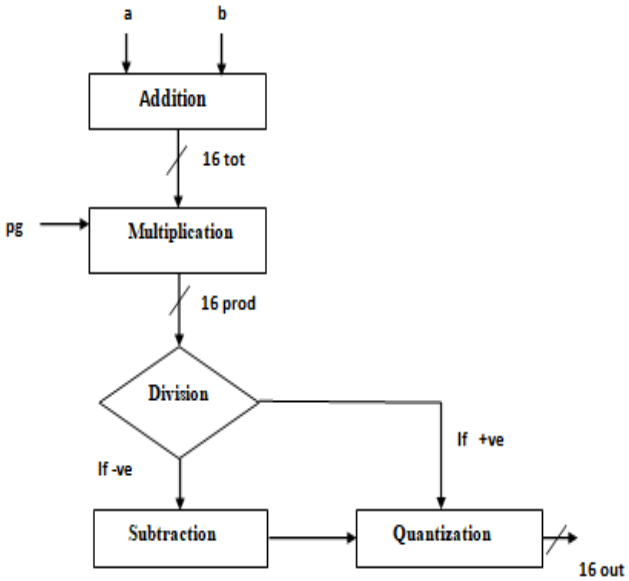

Fig3. Flow chart for 6-bit phase angle calculation of HTRMC.

Step1:
Received phase value is stored and obtains the total for (a + b). Where, 'a' varies from -70 to +70 and 'b' varies from -16 to +16.
Step2: (multiplication)
Here total from above step obtained is multiplied with the received Pg value from the group controller resulting phase product= (a + b)*pg.
Step3: (division)
Divide the product obtained in step2 by 360 using logic core and store the remainder.
Step4: (subtraction)
Subtract the remainder by 360, if the sign of the remainder is negative else if the sign of the remainder is positive no subtraction is required.
Step5 :(quantization)
Quantize the phase values to 6bit by dividing the remainder value by 56.

For the division operation, Xilinx core divider generator V3.0 is used. The divider generator core has features to create a circuit for integer division based on radix-2 non restoring division. The radix-2 algorithm exploits fabric to achieve a range of throughput options that includes single cycle.
In HTRMC two division operations are performed during the computation of 6-bit phase values of each T/R modules. The division of the divider generator is taken as 19-bits. During phase computation, phase product is divided by the maximum value 360 and at the quantization the phase product is divided by maximum value 56.

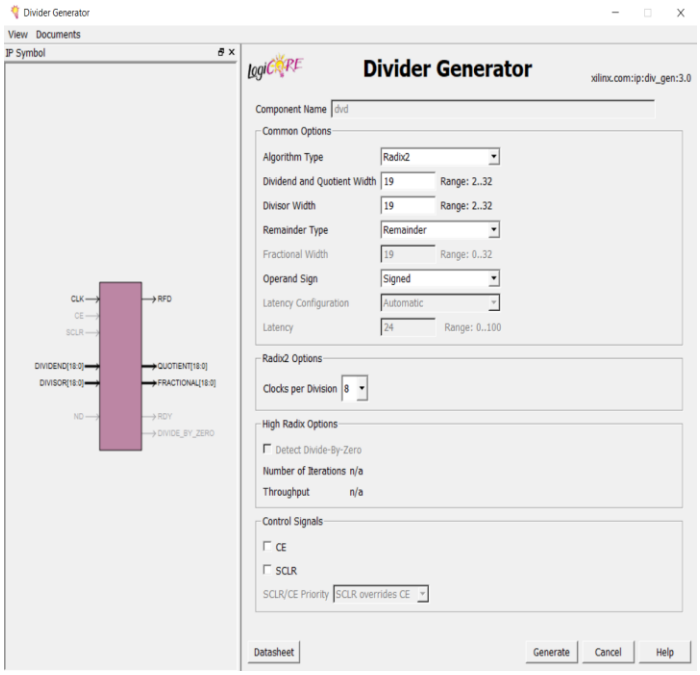

Fig4. Xilinx divider generator logic core with dividend and divisor

Tools used for the implementation of 14 element antenna array are given below.

- Python for phase gradient calculation.
- ISE for programming language.
- ISE simulator for functional simulation.
- Artix-7 FPGA for hardware implementation.

III. THEORITICAL ANALYSIS

The 16 T/R modules in a HTRMC are pointed by signals b0 to b15. Finally, upper antenna elements get activated. The values of T/R modules become b0=1, b1=2, b2=3, b3=4, b4=5, b5=6, b6=7, b7=8, b8=9, b9=10, b10=11, b11=12, b12=13, b13=14, b14=15, b15=16. The computations of the phase value for the first T/R modules are performed as follows.

Pg=01010000 (80)

a=26

b1=1

Product1 = (a + b)*pg

= (26+1)* 80

=2160 (100001110000)

After computing the product the resulting value is assigned to dividend1 signal. The dividend value is divided by common divisor1. The aim of this division is to reduce the phase value within 360.

Dividend1=2160
(100001110000)

Divisor=360 (101101000)

The remainder of the above division operation is considered for further manipulation. The remainder is. The other 15 remainders are calculated in the same manner. In the second division process divisor is taken as 56.This division aims to quantize the output value to 6bit.

Phase out =000000

The same process is repeated for the lower HTRMC with signals b17=-1, b18=-2, b19=-3, b20=-4, b21=-5, b22=-6, b23=-7, b24=-8, b25=-9, b26=-10, b27=-11, b28=-12, b29=-13, b30=-14, b31=-15, b32=-16.Here, the sign of the product is negative so the resultant is subtracted with 360 to continue the quantization in order to eliminate the sign of the value and to quantize the value to 6 bit phase out.

IV. EXPERIMENTAL RESULTS

1. Simulation Results:

6bit phase angle performed at HTRMC for the phase gradient Pg=80 which is taken as out in the simulation. The phases are calculated with 100 MHz clock reference. Fig.5. shows the computation of 6-bit phase angle calculation performed at Hex decagon T/R Module Controller for the phase gradient pg = 80. The simulation result corresponds to TRU number 45 represented in 19 bits. As MSB of the TRU number is '1' indicates upper HTRMC. The 16 T/R modules in a HTRMC are pointed by signals b0 to b15. Finally, upper antenna elements get activated. Fig.6.shows the computation of 6-bit phase angle calculation performed at Hex decagon T/R Module Controller for the phase gradient out = 80. The simulation result corresponds to TRU number 130 represented in 19 bits. As MSB of the TRU number is '0' indicates lower HTRMC. The 16 T/R modules in a HTRMC are pointed by signals b17 to b32. Finally, lower antenna elements get activated.

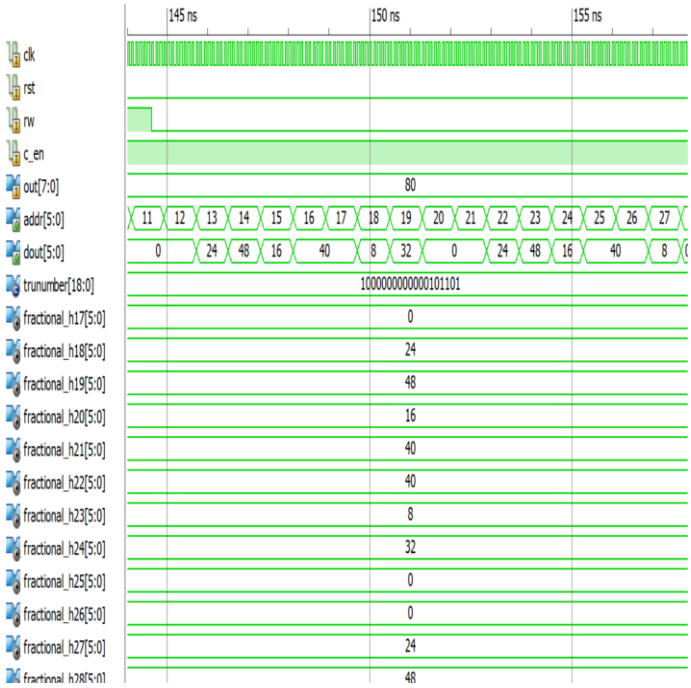

Fig5. Simulation results for upper HTRMC of 6-bit phase values from phase gradient

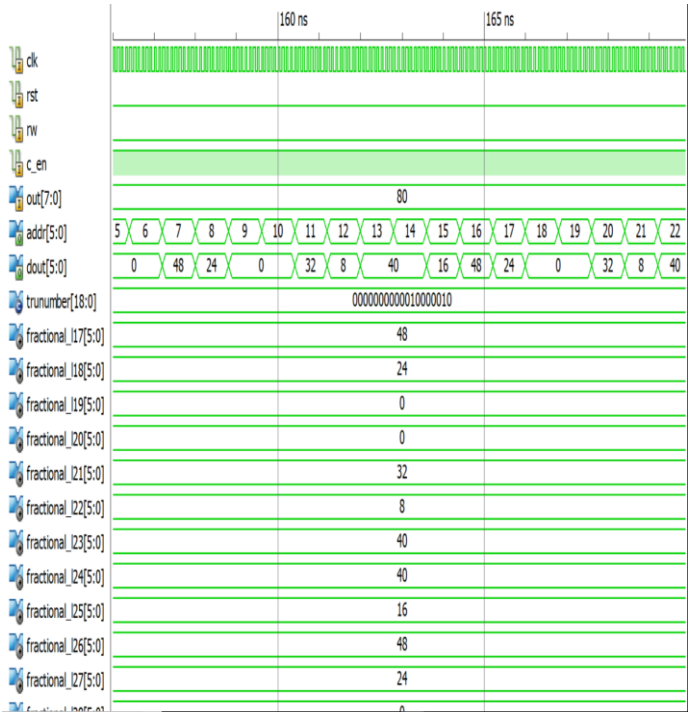

Fig6. Simulation results for lower HTRMC of 6-bit phase values from phase gradient

2. Hardware Implementation:

The hardware implementation of HTMRC design was done with Xilinx ISE design. Divider logic core in this chip was generated by Xilinx divider generator version 3.0.The design is operated with the frequency 100 MHz The proposed system is functional verified with the simulations results and synthesis report as follows below. The device utilization summary is Xilinx ISE after the synthesis of the verilog HDL code is given in table 1.

Table1. Resource utilization for implementation of beam forming on Artix-7 FPGA.

Logic utilization	Used	Available	Utilization
Number of slice Registers	17796	126800	14%
Number of slice LUTs	10999	63400	17%
Number of fully used LUT-FF Pairs	6455	22340	28%
Number of bonded IOBs	21	128	10%
Number of BUFG/BUFGCTRL/BUFHCEs	2	128	1%
Number of DSP 48E 1s	16	240	6%

3. Hardware results:

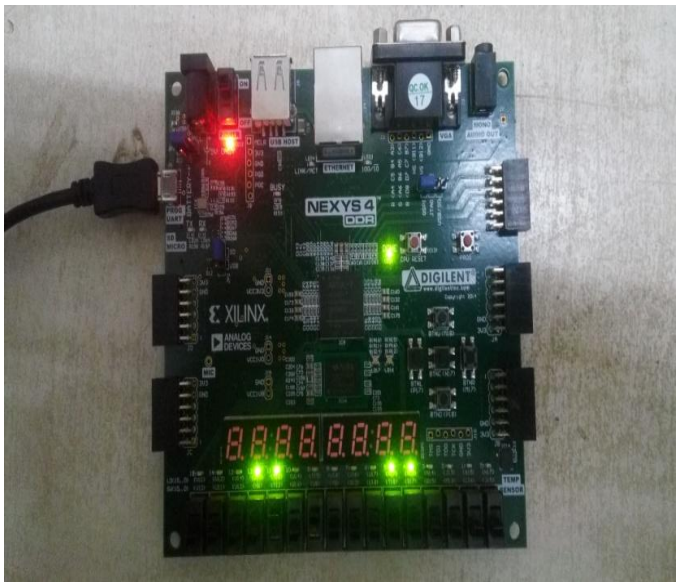

Fig7. Hardware implementation on Artix 7 FPGA for two antenna elements.

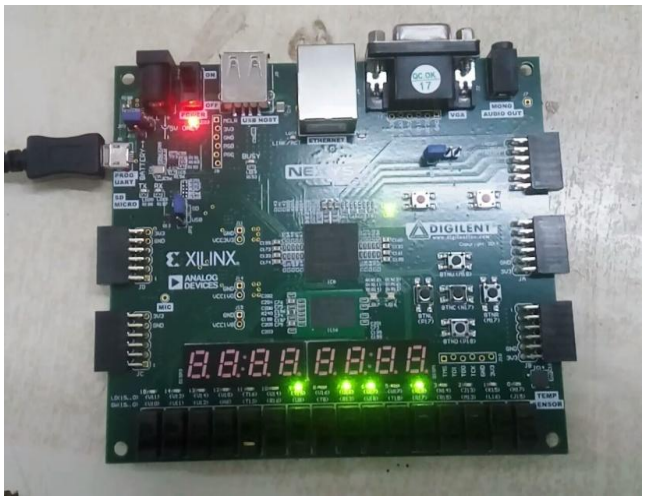

Fig8. Hardware implementation for proposed architecture with data logic unit

In fig.7 hardware is implemented for the two T/R modules in single FPGA. In fig.8 proposed system is implemented on the Artix 7 FPGA with 6 pins assigned for data out and 5 pins are assigned for the address. The output phase values will obtain with respect to the address value for all the 32 T/R modules in parallel.

V. CONCLUSION

Proposed architecture is designed and developed for 32 T/R modules implemented in an FPGA in order to steer the beam of antenna elements. Beam steering and scanning can be carried out in azimuth direction for radar applications. As survey relies on developing five T/R modules in single FPGA which are assigned to 30 pins for 6 bit phase values. In this manner only 10 T/R modules can be implemented in single FPGA that implies as number of T/R modules increases number of FPGA requirement also increases which increases the hardware area cost. From the results obtained, area occupied by the developed architecture is 14% of slice registers and the same can be implemented to more number of T/R modules in single FPGA with help of control logic unit that process continuous flow of data to all T/R modules reduces the hardware cost. These T/R modules sent the phase values to phase shifters for further beam forming. So, the design has advantage of being flexible, scalable and area efficient in terms of hardware cost.

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