Delay Efficient Vedic Multiplier for DSP

Nidhi Gaur, Anu Mehra, Shikha Bathla, Pradeep Kumar

Abstract*: Multipliers are very essential blocks in any arithmetic and logic unit, accumulators and Digital signal processors. Due to the enlarging check on delay, design of faster multipliers is desired. Amidst numerous multipliers, Vedic multipliers are favored for their speed of operation. There are sixteen sutras in Vedic mathematics out of which four are multiplication techniques. "URDHVA TIRYAKBHYAM" is the most efficient vedic multiplication technique in terms of speed. In this paper we aim to develop a multiplier using Ripple Carry Adder and parallel prefix adders which carry out the "URDHVA TIRYAKBHYAM" sutra with improved speed of operation by providing the minimum delay for the multiplication of numbers regardless of their bit sizes. A vast majority of the engineering domain consists of ubiquitous technologies like DSP. As it is one of the most rapid growing technologies of the 21st Century, it faces challenges and improvisation at each step. Engineers are working diligently to improve the quality of Digital Signal processors and major breakthroughs are being made at a very good rate. Proposed multiplier could be applied for such DSP applications. Verilog language has been used for the coding. Xilinx Vivado Tool is used for synthesis and Model Sim 5.4 has been used for simulation.

***Index Terms*: Urdhva Tiryakbhyam, Vedic Multiplier, Ripple Carry Adder, Parallel Prefix Adder.**

I. INTRODUCTION

India has been a land of discoveries in the field of mathematics from the very ancient times, be it the conception of 'zero' or the very famous Vedic mathematical Sutras. We have a rich ancient heritage. The ancient Indian texts named as 'Vedas' which is interpreted as knowledge, provide the key to Vedic Mathematics and in the year 1911 to 1918 Sri Bharati KrishnaTithaji rediscovered Vedic Sutras from these texts [1]. According to his study, Vedic Mathematics works on or is based on sixteen formulae or 'sutras'. "Urdhva-Tiryagbhyam" is one of the sixteen sutras and is translated as vertically and crosswise. It is one of the most used and generalized sutra because human mind also calculates in the same way as described by this sutra: vertically and crosswise. In this paper, Vedic multiplier has been proposed using "Urdhva- Tiryagbhyam" sutra which helps in achieving faster bit multiplication rates and renders the multiplier more delay efficient.

In the present times high speed multipliers [2] can be designed using various approaches. Array multiplier, Booth multiplier, Tree multiplier are few of the many examples of high speed multipliers. Speed of the multiplier can be bettered using reversible logic too [3]. The more speed efficient a multiplier is; the more operations can be implemented on it. A number of DCT [4], DSP and data path operations are feasible through the use of Vedic multipliers. Implementation of Vedic multipliers in the digital signal processing domain could be quite booming. Technologies such as image compression, video recording, speech recognition all involve the use of convolution, filtering and fast Fourier transform which comes under the field of DSP. Since multiplication is the fundamental step in the execution of these operations, the use of a high speed multiplier will surely improve the efficacy of the operation.

Many formulas and algorithms have been derived keeping a check on fast multiplication in mind such as Baugh-Wooley Algorithm, Modified Booth Algorithm and recording bits algorithm. Albeit these algorithms are fast and efficient but poor time efficiency is one of their drawbacks. To optimize the standard arithmetic operations, Vedic mathematics came into use and Vedic multipliers can be relied upon to increase the computational speed of the processor. When number of bits increase in an operation, a similar rise is observed in the delay and area of a multiplier. Thus proposed multiplier is studied for 2 bit, 4 bit, 8 bit, and 16 bit respectively.

II. PROPOSED VEDIC MULTIPLIER

In this paper, Vedic multiplier architecture is realized through structural modelling. First a basic 2X2 vedic multiplier is designed. This multiplier is used as component for the design of higher bit multipliers along with the ripple carry adders and parallel prefix adders as components.

A. 2×2 Vedic Multiplier

A 2 bit Vedic multiplier is designed with direct use of "Urdhva- Tiryagbhyam" sutra for the arithmetic operation of two binary numbers. Two binary numbers of two bits each, for example P and Q are taken. A comprise of P1P0 and Q is comprise of Q1Q0. Vertical multiplication of P0 (LSB) and Q0 (LSB) takes place first. The resultant product is kept as the LSB of the final result. Use of AND gate comes forward for the multiplication of P0 and Q0. The following step is to cross multiply LSB of number P that is P0 with the MSB of number Q that is Q1 and add them with the product generated as a result of cross multiplication of MSB of number P that is P1 with the LSB of number Q that is Q0. The circuitry required here is two AND gates and one Half Adder. This results in an output of two bits. LSB of the resultant output is employed as second bit of the final product and MSB is used as pre carry for the succeeding step. The

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concluding step is the vertical multiplication of the MSB's of the two numbers that is P1 and Q1. The pre carry of the preceding step is added with the resultant product. Thus, the need of a new half adder again arises. The third and the fourth bit of the final result is the two bit output generated by the half adder. The final result is D2T2T1T0. Such is the 2X2 Vedic multiplication (Figure 1) process. Resulting equations are shown.

$$T0 = P0Q0 \quad (1)$$
$$D1 = P0Q1 + Q0P1 \quad (2)$$
$$D2T2 = D1 + P1Q1 \quad (3)$$

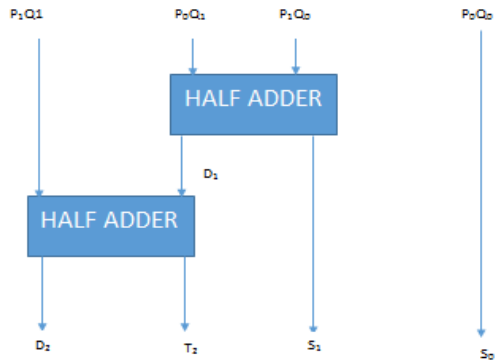

Fig 1. 2X2 Vedic Multiplier Architecture

B. 4X4 Vedic multiplier

Delay efficient 4X4 Vedic multiplier (Figure 2) is realized using the modules of the 4 bit Brent Kung adder and the module of the 2X2 Vedic multiplier realized initially. Since Brent Kung adders are area efficient, so they are used here to make the design area efficient along with delay efficiency.

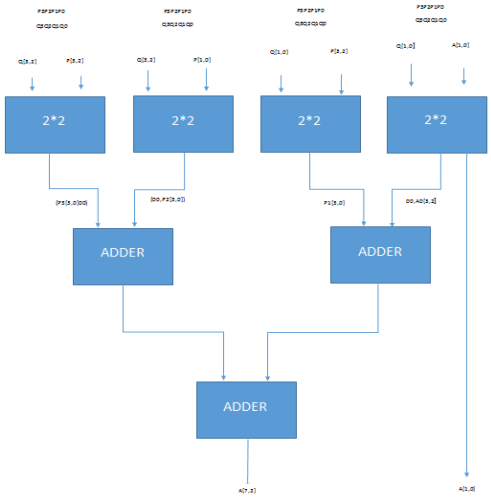

Fig 2. 4X4 Vedic Multiplier Architecture

C. 8X8 Vedic Multiplier

Using the same modelling structure, Delay efficient 8X8 Vedic Multiplier (Figure 3) is realized using the modules of 8 bit ripple Carry Adder and 4X4 Vedic Multiplier.

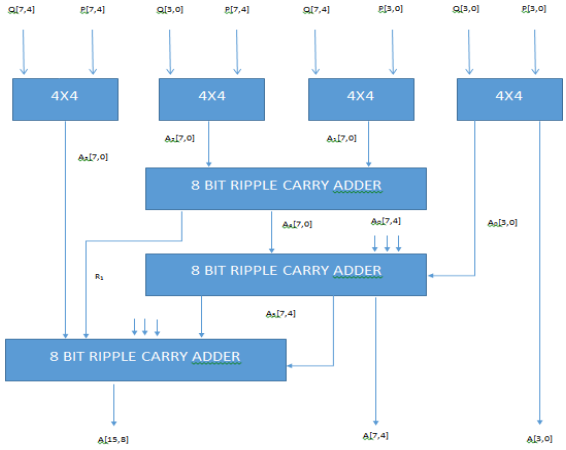

Fig 3. 8X8 Vedic Multiplier Architecture

D. 16X16 Vedic Multiplier

Through the use of structural modelling, delay efficient 16X16 Vedic Multiplier (Figure 4) is realized using the modules of sixteen bit adder and the modules of 8X8 Vedic multiplier.

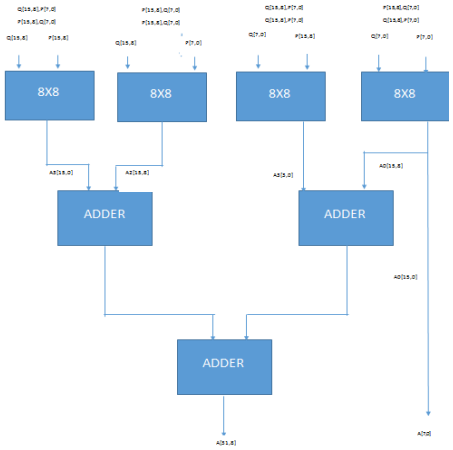

Fig 4. 16X16 Vedic multiplier Architecture

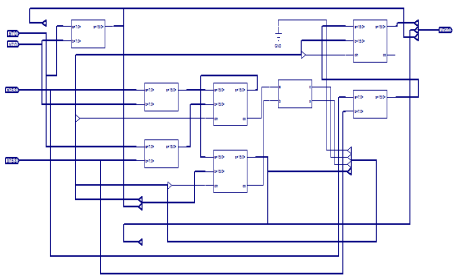

Fig 5. 16X16 RTL Schematic View

III. SIMULATION RESULTS

RTL schematic of 16X16 Vedic Multiplier is shown in figure 5. Simulation result waveforms of 4X4 vedic multiplier, 8X8 vedic multiplier and 16X16 vedic multiplier are presented in figures 6,7 and 8 respectively. The delay measured is reported in Table 1.

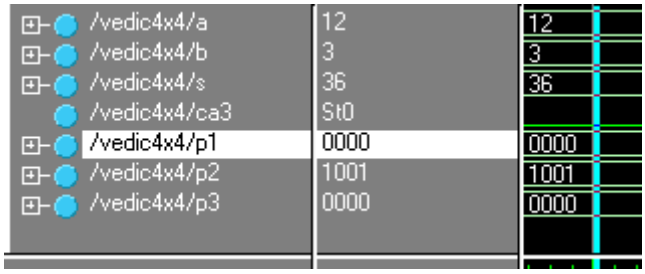

Fig 6. Simulated Result of 4X4 Vedic Multiplier

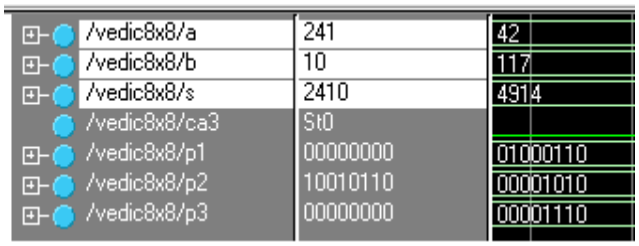

Fig 7. Simulated Result of 8X8 Vedic Multiplier

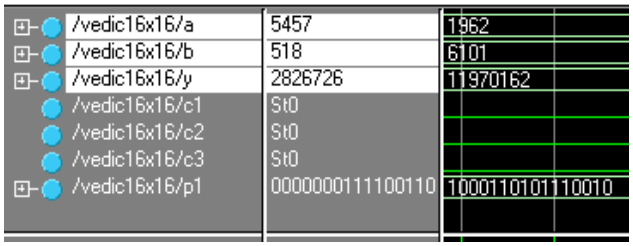

Fig 8. Simulated result of 16X16 Vedic Multiplier

IV. RESULTS AND DISCUSSION

As is evident from Table 1, the combinational path delay of the proposed Vedic Multiplier is reduced by approximately 15%. Less delay is equivalent to prompt and quick response of the processor. Results are compared with conventional booth multiplier implemented in [5]. Arithmetic operations through a Vedic multiplier could be performed in less time as compared to a conventional booth multiplier.

TABLE 1.Delay comparison of Conventional and Proposed Vedic Multiplier

Multiplier (No. of bits)	Conventional Booth Multiplier [5]	Proposed Vedic Multiplier
4×4	17.86 ns	16.437 ns
8×8	39.28 ns	32.395 ns
16×16	75.23 ns	58.909 ns

V. CONCLUSION

This paper implements a delay efficient Vedic multiplier for DSP applications. The architecture could be directly implemented in a DSP block requiring multiplier for further calculations. Vedic multiplier could be further implemented for 32 bits and 64 bits which finds application in processor design as well.

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