Power Analysis of Digital Circuits for VLSI Applications

Shikha Bathla, Nidhi Gaur, Ayush Uniyal

Abstract*: In this modern world, power plays a very important role in designing of electronic circuits. Portable devices like mobile phones, laptops require electronic circuits that consume less power. Power dissipation causes invariably rise in temperature of electronic circuits. As the temperature increases, the power gets dissipated more. MTCMOS (Multi-Threshold Complementary Metal Oxide semiconductor) power gating is a design technique that reduces power dissipation. It results in the prevention of sub-threshold leakage in standby mode and high speed operation with low power consumption in active mode. In this paper, MTCMOS based MUX is designed and is compared with CMOS MUX and PTL (Pass Transistor Logic) based MUX. It has been concluded that MTCMOS based MUX consumes 16.56% and 15.19% less power than CMOS MUX and PTL MUX respectively. Results are simulated in Mentor Graphics version 10.2.

***Index Terms*: PTL, power gating, power dissipation, MTCMOS**

I. INTRODUCTION

With the increase in the development of portable devices, the demand of increasing speed and decreasing power dissipation has been increasing. MTCMOS technology plays a vital role to reduce power dissipation. The name MTCMOS (Multi- threshold CMOS) says that it has multiple threshold, high Vt (Threshold Voltage) which prevents sub threshold leakage in standby mode and low Vt which is required for high speed operation with low power consumption.[1] There are three types of power: dynamic power, switching power and the leakage power. In the earlier technology, it has been found that out of total power, dynamic power comprises of typically 75% power, circuit power comprises of 20% and leakage power comprises of 5%. As the advancement in technologies has taken over from last 10-15 years, the devices are becoming smaller in both length and width and due to this there is an increase in leakage power. MTCMOS technology is a better way to implement circuits designed for low power applications [1],[6].

II. LITRATURE SURVEY

The idea to enhance the performance of logic circuits results in the development of many logic design techniques during the last two decades. Digital Circuits like multiplexer, shortened to "MUX is basically implemented using CMOS Technology which is not power efficient. To mitigate this problem either PTL or power gated design circuit using MTCMOS technology can be used in designing MUX.

A. MTCMOS

MTCMOS is an increasingly popular circuit approach that enables high performance and low power operation. This technique is used for improving the performance by increasing the speed of the circuits. One method is to reduce threshold voltage, V_t, but the leakage current starts increasing due to which power dissipation is more.

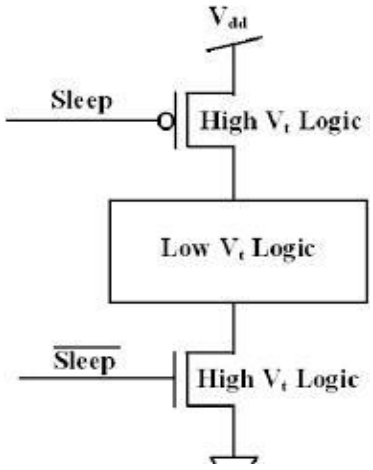

Fig 1 power gated circuit

In MTCMOS Technology, an additional hardware is provided as shown in Figure 1 , there is one extra p-MOS and one n-MOS in CMOS based MUX. These transistors have high threshold value by design, then they are given a signal sleep and sleep bar. When sleep is 0 and sleep bar is 1, p-channel and n channel conducts and therefore a circuit runs in active mode and behaves as a normal CMOS MUX and works at high speed but in standby mode, one can make sleep bar 0 and sleep 1, both p-channel and n-channel are in cut off region and due to high threshold value of these transistors , less leakage current flows through the circuit and therefore , power dissipation is minimized.[2]

B. PTL

In Pass transistor logic (PTL), transistors are used as switches to pass logic

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levels between nodes of a circuit, instead of as switches connected directly to supply voltages [3]. By using this logic, number of transistor can be reduced.

PTL concept is based on relay switches. Thus to reduce the area overhead either p-channel MOS or n-channel MOS sleep transistors are used. Due to the fact that for same equivalent resistance n-channel MOS transistors take less area than the p-channel MOS transistors. Implementation of n-channel MOS sleep transistors are most commonly used.[4]

III. SOFTWARE IMPLEMENTATION

The 2 bit MUX has been designed and simulated by different logics on mentor graphics version 10.2 at 180 nm technology node. The following figures illustrate the implementation of MUX using CMOS technology (Figure 2), PTL (Figure 3) and hybrid MTCMOS PTL [5] , [7] (Figure 4).

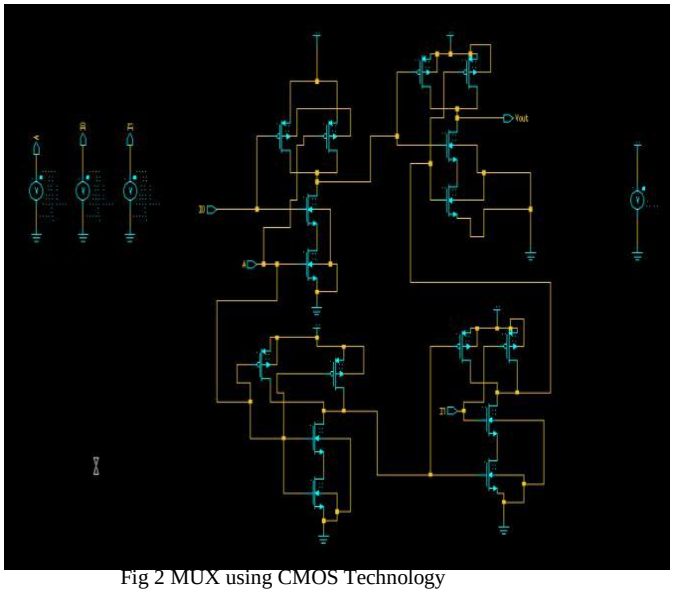

Fig 2 MUX using CMOS Technology

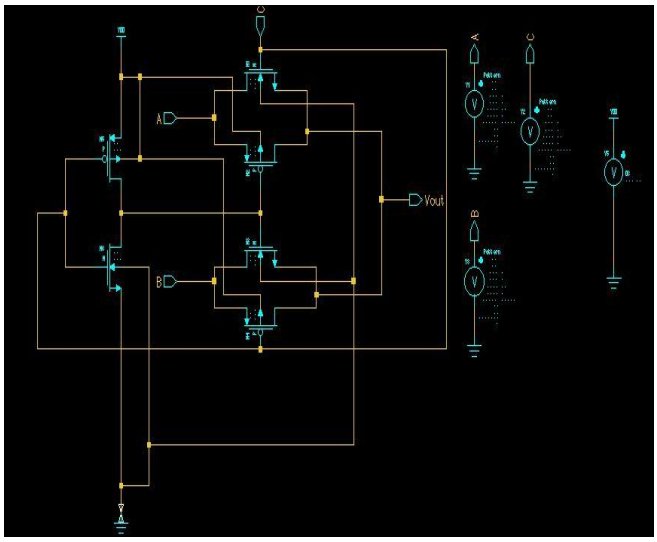

Fig 3 MUX using PTL

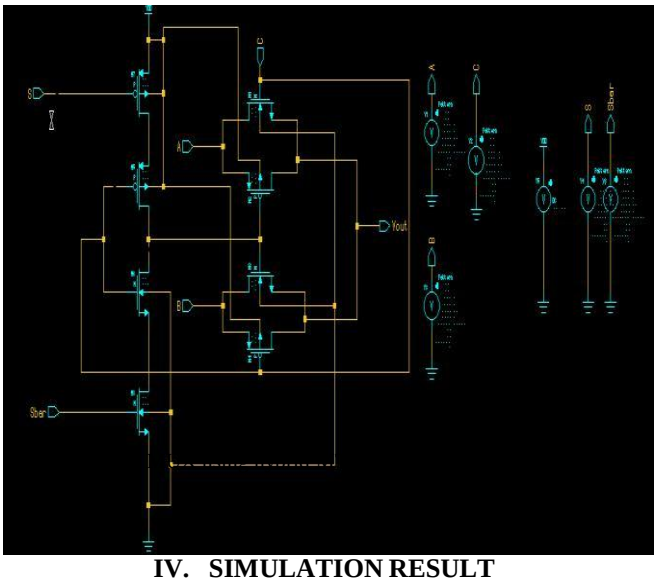

Fig 4 MUX using hybrid MTCMOS PTL

IV. SIMULATION RESULT

The target technology is the mentor graphic pyxis schematic editor. The results are simulated using this technology and are illustrated as follows:

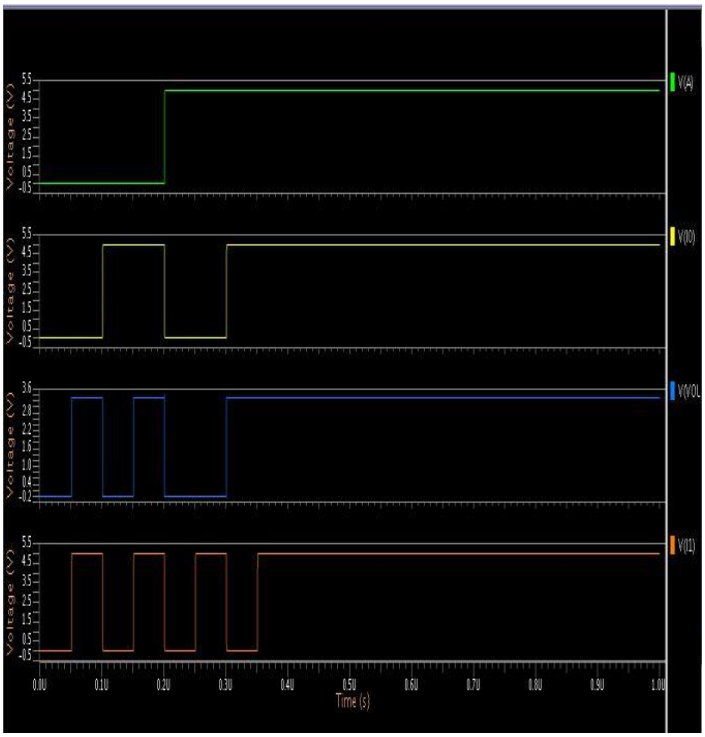

Fig 5 Simulation result of MUX using CMOS Technology

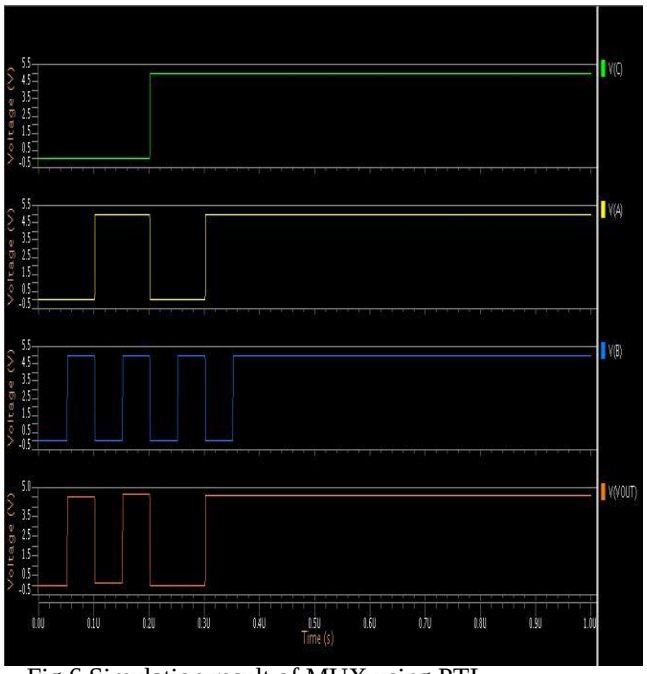

Fig 6 Simulation result of MUX using PTL

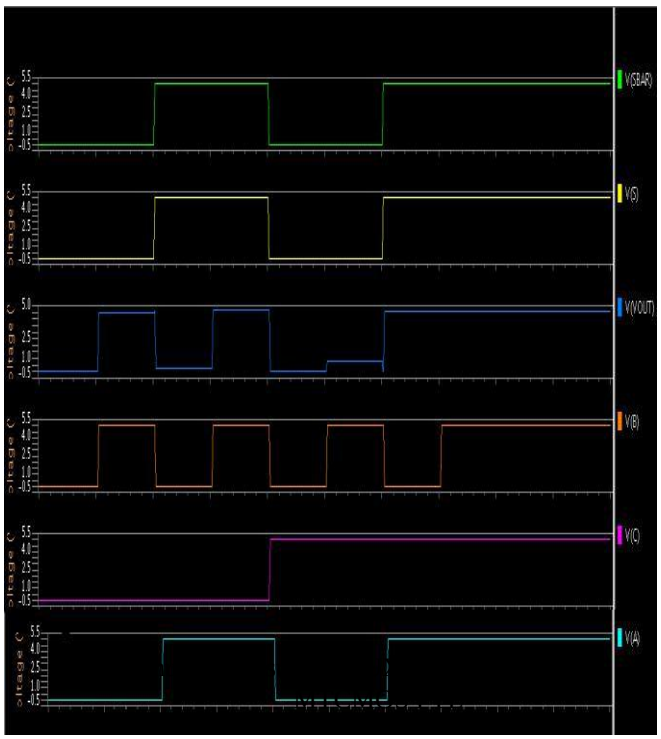

Figure 5 represents simulation result of MUX using CMOS Technology, Figure 6 represents simulation result of MUX using PTL Technology and Figure 7 represents simulation result of MUX using hybrid MTCMOS PTL. Table 1 and Figure 8 represents Average power dissipation of 2:1 MUX using CMOS Technology, PTL and Hybrid MTCMOS PTL at different voltages. Table II represents the Average power dissipation, delay, PDP (power delay product) and transistor count of different circuits i.e 2:1 MUX using CMOS Technology, PTL and Hybrid MTCMOS PTL at 3.3 V.

Figure 9 represents power delay product (PDP) of 2:1 MUX at 3.3V

Table I : Average power dissipation of 2:1 MUX using CMOS Technology, PTL and Hybrid MTCMOS PTL at different voltages.

	Average Power dissipation		
Voltage	CMOS Technology (pW)	PTL (pW)	Hybrid MTCMOS PTL (pW)
1	5.5763	5.343	5.165
1.5	12.5593	12.1146	11.5442
2	22.69	21.9739	20.4527
2.5	36.581	35.5361	31.889
3	55.861	54.4223	45.8579

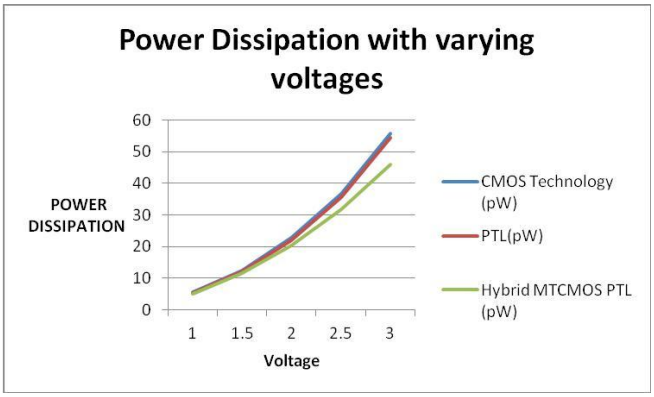

Fig 8 Average power dissipation of 2:1 MUX using CMOS Technology, PTL and Hybrid MTCMOS PTL at different voltages

Table II Average power dissipation, delay, PDP (power delay product) and transistor count of different circuits i.e 2:1 MUX using CMOS Technology, PTL and Hybrid MTCMOS PTL at 3.3 V

	Average Power (pW)	Delay (ns)	PDP (10^{-16} Ws)	Transistor count
CMOS Technology	**72.0149**	**99.957**	**7.198**	**16**
PTL	**70.6492**	**99.957**	**7.061**	**6**
Hybrid MTCMOS PTL	**55.4532**	**99.957**	**5.542**	**8**

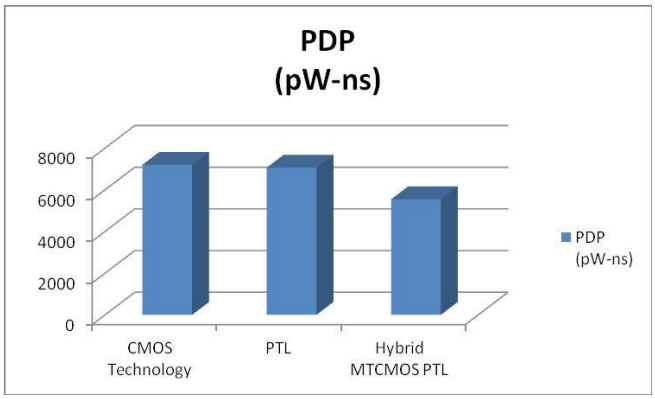

Fig 9 Power Delay Product (PDP) of 2:1 MUX at 3.3V

V. CONCLUSION

The 2 bit MUX has been designed and simulated by different logics i.e CMOS Technology, PTL and Hybrid MTCMOS PTL on mentor graphics version 10.2. Experimental results show that MTCMOS based MUX consumes 16.56% and 15.19% less power than CMOS MUX and PTL MUX respectively. The circuit designed with hybrid MTCMOS PTL is giving a better performance by optimizing the Average power dissipation. A comparative analysis of power delay product of these logics is also carried out (Figure 9). The results again confirmed that lowest PDP is achieved with MTCMOS PTL.

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Shikha Bathla, born in Haryana in India, on March 06, 1985. After completing, Bachelor of Technology in the field of Electronics and Communication Engineering from Kurukshetra University, Kurukshetra in 2006. She did her Masters in Technology in the field of Electronics and Communication Engineering with specialization in "VLSI Design" from Banasthali Vidyapith, Rajasthan in 2009. Presently, she is working as an Assistant Professor in the Department of Electronics and Communication Engineering at Amity University, Noida. Her fields of interest lie in VLSI Design and Embedded Systems. She has more than 10 publications in International journals and conferences.

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