Leakage Power Consumption of Address Register Interfacing with Different Families of FPGA

Bishwajeet Pandey, Keshav Kumar, Shabeer Ahmad, Amit K Pandit, Deepa Singh, D M Akbar Hussain

Abstract—In this paper, we are designing an address register which is sensitive towards rising in voltage. We analysed the power variation of address register on Xilinx 14.1 ISE Design Suite and the code of address register is written in Verilog hardware description language. In this paper, we have used two FPGA of two different families, one is of Virtex family which is Virtex 6 and the other is of Spartan family which is Spartan 6, to study the power consumption of address register. We have observed the different on chips power which are consumed by address register by varying the voltage from 0.75V to 2V for Virtex 6 FPGA and 0.75V to 3V for Spartan 6 FPGA and we observed that when we lower the voltage, lower will be the power consumption. At 2V, Virtex 6 FPGA stops working and the interface of address register with FPGA burns out. For Spartan 6 FPGA, the same happens at 3V voltage.

Keywords—Power variation, Xilinx, Verilog, Voltage Scaling, FPGA.

I. INTRODUCTION

Today's world is facing a very enormous problem with the energy crisis. Day by day the demand of people towards natural resources i.e. nonrenewable resources is increasing rapidly. The three main causes of this energy crisis are overconsumption, overpopulation and poor infrastructure [1]. To ensure the less wastage of the natural resources of the planet, we are making an address register which will consume low power in the communication system. As our address register will consume low power, there will be less use of electricity and thus less use of natural resources of the planet. The design of address register is interfaced with two FPGA of different families one is Virtex 6 and the other is Spartan 6 FPGA. The address register is used in the communication network to store data bit and to manipulate the stored bit [2]. In our design, we are scaling the voltage of address register from 0.75V to 2.00V for Virtex 6 FPGA and 0.75V to 3.00V for Spartan 6 FPGA for analysing the different on chips power which is fabricated on this device. The RTL schematic and technology schematic of the address register is shown in Fig. 1 and 2 respectively.

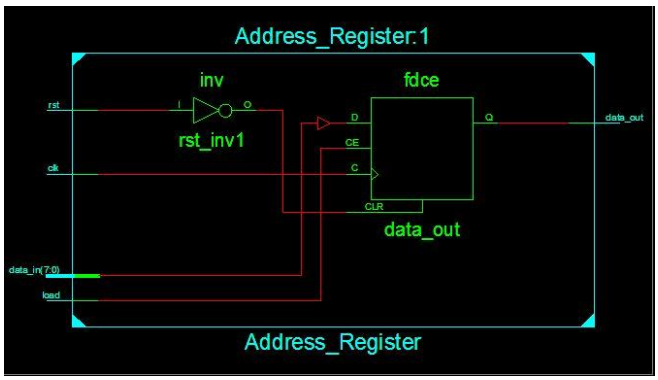

Figure 1. RTL schematic of the address register.

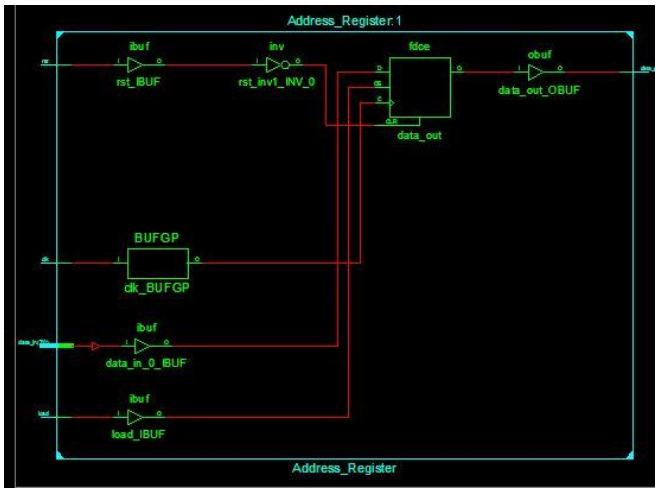

Figure 2. Technology schematic of the address register.

II. EXPERIMENTAL SETUP

We performed our experiment on Xilinx ISE Design Suite and the code of address register is written in Verilog Hardware Language. The power consumption of address register is analysed on X Power analyser tool. The ambient temperature of both the FPGA is 50oC and has an airflow of 250 LFM [Linear Feet Meter].

III. RELATED WORK

I.Kabin et.al [3] designed FPGA implementation of ECC. In this work, authors discussed hardware implementation of

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address bits on FPGA. W.Tang et.al [4] designed hardware design of genetic algorithm on FPGA. In this work author designed parallel configuration with PCI board. M.Chmiel [5] implemented Central Processing Unit with Virtex 4 FPGA. This work represents a specific timer and control hardware solution. B. Pandey et.al [6] worked on designing a low voltage and low power VLSI circuit on FPGA. They used Virtex 6 FPGA and RAM-UART to analyse power reduction. B. Pandey et.al [7] implemented energy efficient ALU [Arthemetic Logic Unit] on 40nm FPGA. Spartan 3 and Virtex 6 FPGA are used to analyse dynamic power reduction with LVCMOS12. E.B.Kavun et.al [8] designed FPGA implementation of lightweight cypher PRESENT on Xilinx Spartan XC3S50 device. But in our work we have interfaced address register with two FPGA, Virtex 6 and Spartan 6 to analyse the leakage power consumption.

IV. POWER ANALYSIS & RESULTS

A. Power analysis of Address Register interfaced with Virtex 6 FPGA.

When the voltage of Virtex 6 FPGA scaled from 0.75V to 2V, it is observed that there is only consumption of leakage power in the address register. All the other on chips power e.g. clocks, logic, signal, I/O are negligible. As voltage increases, there is an increment in leakage power. Thus we can state that lower the voltage lesser will be the consumption of leakage power. The power chart of Virtex 6 FPGA is shown in Table 1. The magnitude of 1.75V is the last operating voltage of Virtex 6 FPGA, beyond this voltage i.e. at 2V the interfacing of address register with Virtex 6 FPGA burns out. The power v/s voltage figure of Virtex 6 FPGA is shown in Fig. 3.

Table 1. Leakage power with Virtex 6 FPGA.

Voltage Value (V)	Leakage Power (W)
0.75	0.887
1.00	1.293
1.25	2.396
1.50	5.625
1.75	16.596
2.00	39.641

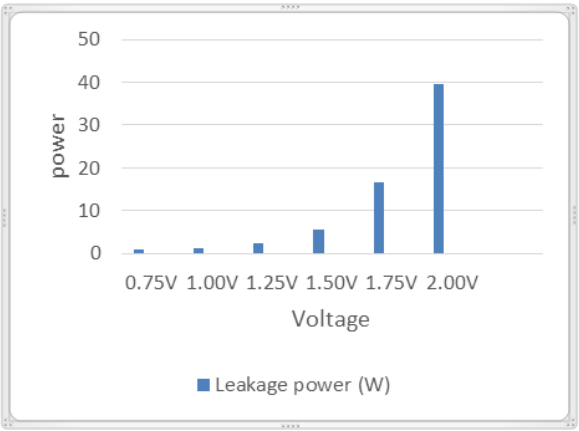

Figure 3. Power V/S Voltage with Virtex 6 FPGA.

B. Power analysis of Address Register interfaced with Spartan 6 FPGA.

Interfacing of Virtex 6 with address register burns at 2V, but in case of Spartan 6 FPGA the interfacing burns at 3V. In the case of Spartan 6 FPGA also as the value of voltage increases, there is an increment in leakage power. The power chart is shown in Table 2 and power v/s voltage figure is shown in Fig. 4.

Table 2. Leakage power with Spartan 6 FPGA.

Voltage Value (V)	Leakage Power (W)
0.75	0.010
1.00	0.011
1.25	0.015
1.50	0.024
1.75	0.049
2.00	0.115
3.00	20.125

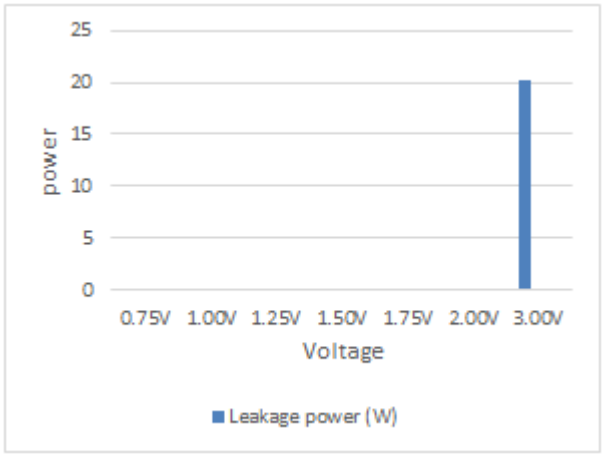

Figure 4. Power V/S Voltage with Spartan 6 FPGA.

C. Power Analysis of Virtex 6 V/S Spartan 6 FPGA.

The leakage power consumption of Spartan 6 FPGA is lower than Virtex 6 FPGA at every value of voltage. Also, Spartan 6 FPGA gives more voltage range of operating address register since it burns at 3V were as Virtex 6 at 2V. The power comparison table of both FPGA is shown in Table 3.

Table 3. Leakage power of Virtex 6 V/S Spartan 6.

Voltage (V)	Leakage power (Virtex 6)	Leakage power (Spartan 6)
0.75	0.887	0.010
1.00	1.293	0.011
1.25	2.396	0.015
1.50	5.625	0.024
1.75	16.596	0.049
2.00	39.641	0.115
3.00	0.000	20.125

V. CONCLUSION

From the power analysis of both the FPGA, it is observed that Spartan 6 FPGA consumes the least amount of power. Spartan 6 takes 98.87%, 99.14%, 99.37%, 92.90%, 99.70%, and 99.70% less leakage power than Virtex 6 FPGA at 0.75V, 1.00V, 1.25V, 1,50V, 1.75V, and 2.00V respectively. On interfacing address register with Virtex 6 and Spartan 6 FPGA on Xilinx ISE Design Suite, we found that Spartan 6 is a most power-efficient device at all values of voltage and also gives a wide range of voltage value for the operation.

VI. FUTURE SCOPE

This work describes the interfacing of address register with Virtex 6 and Spartan 6 FPGA. But we can also interface address register with other FPGAs like Cyclone FPGA, Artix-7 FPGA, and Kintex-7 FPGA etc. for analyzing the power. We can also scale the current value, frequency value and change I/O standards to observe the variation in the power consumption that will be helpful in green communication.

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