Power Efficient Frequency Scaled and Thermal-Aware Control Unit Design on FPGA

Keshav Kumar, Shabeer Ahmad, Bishwajeet Pandey, Amit K Pandit, Deepa Singh, D M Akbar Hussain

Abstract-: ***These works describe the implementation of a control unit which is an important part of Central Processing Unit (CPU) with the Field Programmable Gate Array (FPGA). In this work a frequency scaled and thermal aware energy-efficient control unit is designed with the help of 28 nanometer (nm) technology based FPGA. Frequency varies from 100MHz to 5GHz and the rise in frequency also gives rise in power consumption of control unit with FPGA. The thermal properties of FPGA also increase with increment in frequency. This whole experiment is done on Xilinx 14.1 ISE Design Suit and it is observed that lower the frequency, lower will be the power consumption of FPGA.***

Keywords: FPGA, Control Unit, Frequency, Thermal Properties

I. INTRODUCTION

Today's era is receiving new attention towards green communication [1]. The demand of the world towards technologies of energy-efficient communication and devices is increasing rapidly [2]. This work gives a ray of light on designing an energy-efficient control unit with the help of 28nm Artix-7 FPGA. In this working frequency of operation of the control unit is scaled from 100MHz to 5GHz. The different set of frequencies for which power consumption is analysed is shown in Fig. 1.

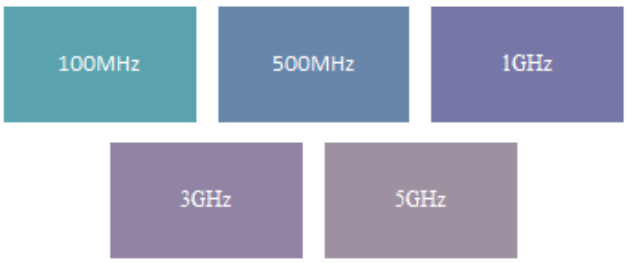

Figure 1. A different set of frequencies for the operation of the control unit.

A control unit is a circuitry component that governs the operation within the computer's processor [3]. It gives direction to the computer's logic unit, memory, input and output devices on how to respond to the instructions sent by the program to these devices [4]. The block diagram of the control unit is shown in Fig. 2.

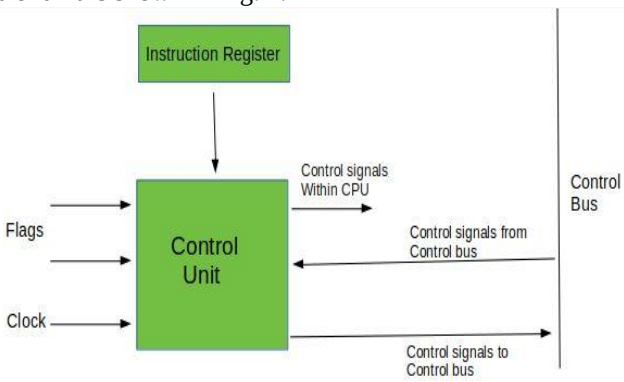

Figure 2. Block diagram of the control unit [4].

II. RELATED WORK

In [5] the authors used FPGA to generate a true random number by inducing meta-stability and bi-stable circuit. In [6] developed photovoltaic modules for real-time simulation using FPGA. In [7] researchers implemented the Arithmetic Logic Unit (ALU) design on FPGA by changing frequency values. In [8] researchers used Virtex-6 FPGA to design four-bit unsigned up counter by enabling clock and with an asynchronous clear. In [9] authors interfaced Random Access Memory (ROM) design on Virtex-6 FPGA.

III. EXPERIMENTAL SETUP

This experiment is performed on Xilinx 14.1 ISE simulator and the code of control unit is written in Verilog Hardware Description Language (HDL). Power analysis of control unit is done with X Power Analyser tool. The schematic of the control unit obtained from Xilinx simulator is shown in Fig. 3.

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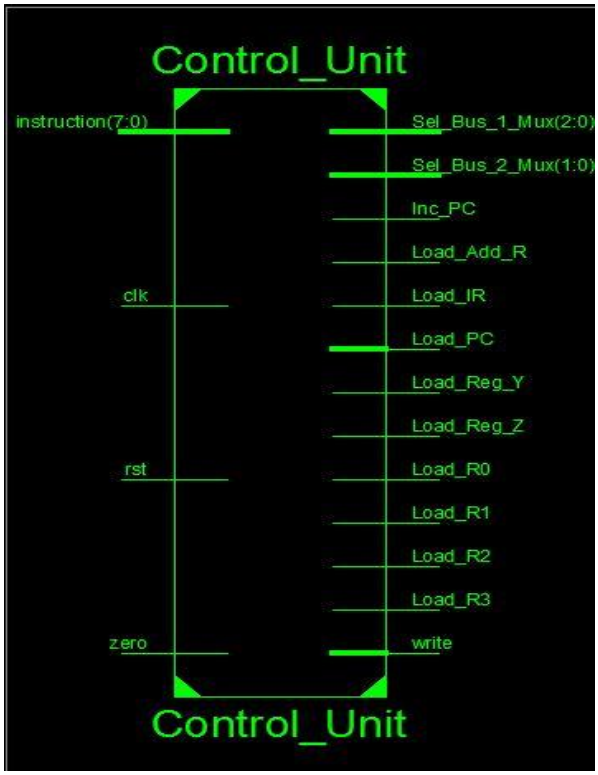

Figure 3. Schematic of the control unit.

IV. POWER ANALYSIS

4.1 Power Analysis for frequency 100MHz.

When the frequency is 100MHz, there is no consumption of logic and signal power of FPGA. Total power consumption is 0.048W which constitutes 0.001W clock power, 0.005W input/output (I/O) power and 0.042W leakage power. Fig. 4 represents the power consumption graph of Artix-7 FPGA at 100MHz frequency.

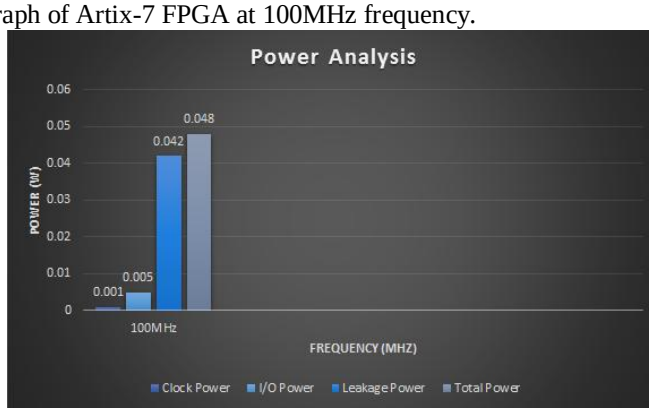

Fig. 4. Power Analysis for frequency 100MHz.

4.2 Power Analysis for frequency 500MHz.

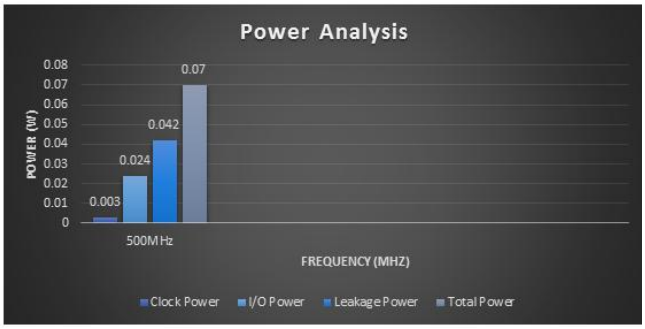

Fig. 5 Power Analysis for frequency 500MHz.

4.3 Power Analysis for frequency 1GHz.

At 1GHz of frequency, logic power is 0.000W. Total power consumption of 0.097W comprises of clock power which is 0.005W, signal power which is 0.001W, I/O power which is 0.048W and leakage power which is 0.043W, which can be seen in Fig. 6.

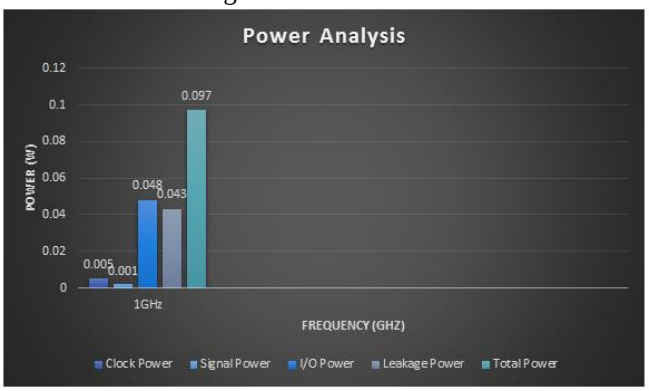

Figure 6. Power Analysis for frequency 1GHz.

4.4 Power Analysis for frequency 3GHz.

When the frequency is 3GHz then all the on chips power of FPGA contributes to total power consumption. At 3GHz of frequency, clock power is 0.016W, logic power is 0.001, and the signal power is 0.002W, I/O power 0.144W and leakage power 0.043W. Power analysis at 3GHz frequency is shown in Fig. 7.

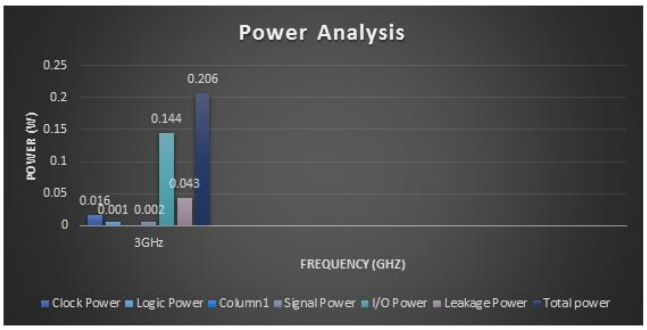

Figure 7. Power Analysis for frequency 3GHz.

4.5 Power Analysis for frequency 5GHz.

At 5GHz of frequency, clock power, logic power, signal power, I/O power and leakage power are 0.026W, 0.001W, 0.004W, 0.241W and 0.043W respectively. All this on chips power contributes to total power consumption of 0.315W. Power analysis graph is described in Fig. 8.

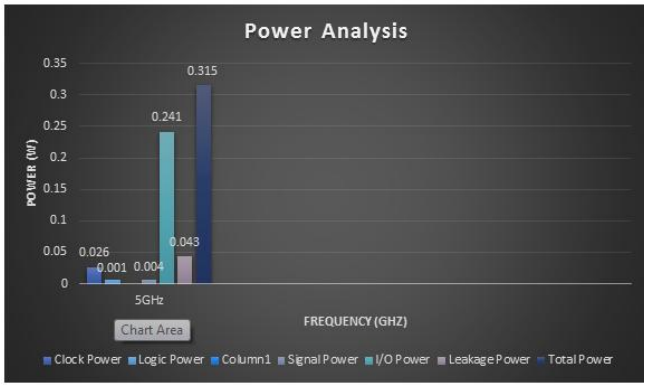

Figure 8. Power Analysis for frequency 5GHz.

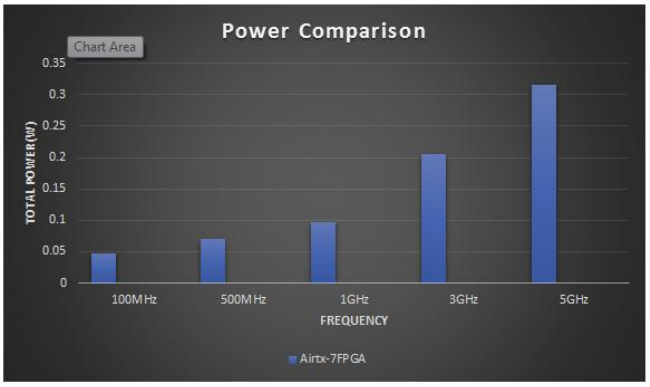

Figure 9. Total Power comparison.

V. THERMAL CONDITIONS FOR FREQUENCIES 100MHZ, 500MHZ, 1GHZ, 3GHZ AND 5GHZ

Thermal condition of a device plays an important role in device power consumption. The three major parameters which govern key role in FPGA power consumption are as follows:

A. Effective Thermal Resistance to Air (ΘJA (°C/W)) - It is also known as Theta-JA and TJA.

B. Maximum Ambient Temperature (°C).

C. Junction Temperature (°C).

The effective thermal resistance to air (ΘJA (°C/W)) is the same at all values of frequencies that is 3.3 (ΘJA (°C/W)). The maximum ambient temperature of FPGA decreases with increase in frequency and junction temperature of FPGA increases with increase in frequency. Table 1. Represents the thermal properties of Artix-7 FPGA.

Thermal Properties	100MHz	500MHz	1GHz	3Ghz	5GHz
Effective Thermal Resistance to Air (ΘJA (°C/W))	3.3	3.3	3.3	3.3	3.3
Maximum Ambient Temperature (°C).	84.8	84.8	84.7	84.3	84.0
Junction Temperature (°C).	25.2	25.2	25.3	25.7	26.0

Table 1. Thermal Properties of Artix-7 FPGA.

VI. RESULT ANALYSIS

The power consumption of control unit circuitry interfaced with Artix-7 FPGA increases with increase in frequency. The total power consumption for 100MHz, 500MHz, 1GHz, 3GHz, and 5GHz is as 0.048W, 0.070W, 0.097W, 0.206W and 0.315W respectively. There is an increment of 45.83% of total power consumption from 100MHz frequency to 500MHz frequency, also there is an increment of 102.08%, 329.17% and 556.25% of total power consumption, when frequency increases from 100MHz to 1GHz, 3GHz and 5GHz frequency. Fig. 9 describes the comparison of the total power consumption of Artix-7 FPGA for different values of frequencies.

VII. CONCLUSION

In this experiment control unit is implemented on Artix-7 FPGA and it is observed that as the value of frequency increases, there is also increased in power consumption. For low power consumption, the frequency must be as low as possible. In this experiment it is found that at 100MHz frequency power consumption is lowest, hence it can be concluded that control unit interfacing with Artix-7 FPGA is the most power-efficient at 100MHz frequency.

VIII. FUTURE SCOPE

Unlike Artix-7 FPGA, researchers can use other FPGAs also like Spartan family FPGA, Virtex family FPGA, Cyclone FPGA etc. to analyse the power consumption of control unit. Not only control unit researchers can implement other circuits also with FPGA to promote a step towards green communication.

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