Design and Implementation of Low Noise Amplifier At 60ghz using Current Mirror Feedback

S. B. Rashmi, Siva S Yellampalli

Abstract*: This discourse used 45nm CMOS technology to design a Low noise amplifier for a Noise figure < 2dB and gain greater than 13dB at the 60GHz unlicensed band of frequency. A single stage, primary cascode LNA is modeled and its small signal model is analyzed. Common source structure is hired in the driver stage to escalate the output power with single stage contours. To enhance small signal gain, simple active transistor feedback and cascode feedback configurations are designed and appended to the basic LNA. In addition to this, current re-use inductor is designed and added to the cascode amplifier which is deliberated to give low power and low noise figure. Small signal analysis of simple active transistor feedback and current re-use inductor has been presented. The measurement results indicated that the input match and the output gain at 60GHz achieves -8dB and 13dB respectively with the supply voltage of 900mV. The frequency response obtained is a narrow band response with 6GHz of bandwidth. The circuit is simulated by Cadence Virtuoso tool. The layout of the related circuit is drawn by means of the Virtuoso Layout editor with total size of 0.1699µm2.

***Index Terms*: 60GHz, Current mirror feedback, LNA, low noise figure, RF amplifier.**

I. INTRODUCTION

The contemporary evolution in CMOS technology at unlicensed 60GHz band. Suitable enough to meet the requirement at large scale wireless transceiver. The solitary promising application for 60-GHz for an increasing demand of multi-gigabit wireless networking. The efforts still have widely concentrated to operate on the 60-GHz band for point-to-point communication in consign with its low noise figure and gain. A low noise amplifier is one of the major blocks in the transceiver system. It is generally the first block of the receiver subsequent after the antenna. The LNA amplifies the input signals so that the noise generated in this block has a minor impact on the system signal to noise ratio (SNR) ratio. LNA circuits in CMOS technology are designed as Common Source (CS) or Common Gate (CG) stages. Another, cascode stage that is widely used in CMOS RF LNAs, can be considered as current –reuse configuration of a CS stage, followed by a CG stage. Common Source and Common Gate are two widely used transistor configurations in CMOS LNA circuits. CS LNA has high gain and good noise performance. Additional inductor in the source of a CS stage which is known to be Inductive Source degenerated. This additional inductor affects the gain and noise performance of LNA as discussed earlier. CG configuration has weak noise performance. Some techniques, such as capacitive cross coupling, have been presented to improve the CG stage noise performance. In this paper, the provocation and the research problem of 60-GHz networking are surveyed and illustrated. An amplifier elevates the power of both the signal and the noise present at its input. LNAs are sketched to attenuate additional noise.

The design in this paper has achieved a minimal noise figure by considering trade-offs that include impedance matching, selecting low-noise biasing conditions and output impedance matching circuit.

II. TRANSISTOR MODEL

In RFIC's design transistors are normally biased at a constant drain current density. The transistor's power consumption normally a resultant of current and drain-source voltage V_{DS}. Further VGS is applied to achieve desired current density and it has no effect on dissipated dc power.

A. MOSFET high frequency performance

To characterize transistors RF performance at a chosen bias point following figure of merit are employed.

i. Cutoff frequency f_T
ii. Maximum oscillation frequency f_{max}

An evaluation of f_T and f_{max} performance for selected MOSFET from gpdk45 library. Figure 1 depicts the f_T is plotted against different gate-source voltage Vgs. Figure 2 shows the current density is plotted against cutoff frequency f_T. This plot ensures the maxima of fT are achieved for a current density of mA/um. This proves the selected MOS can yield a low power consumption and high frequency gain.

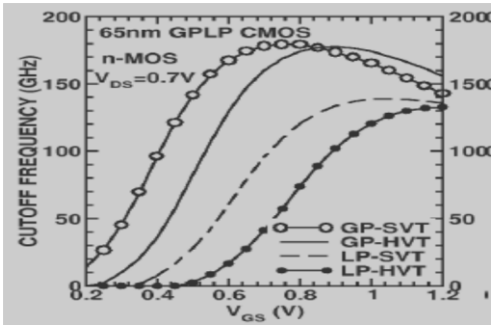

Figure1: f_T versus gate source voltage

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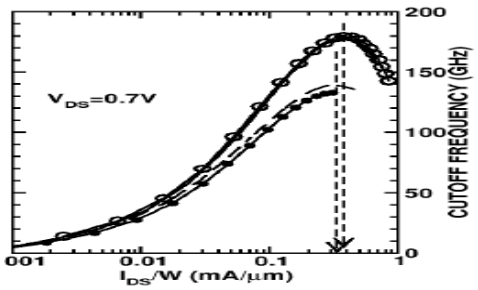

Figure 2: current density versus cut-off frequency

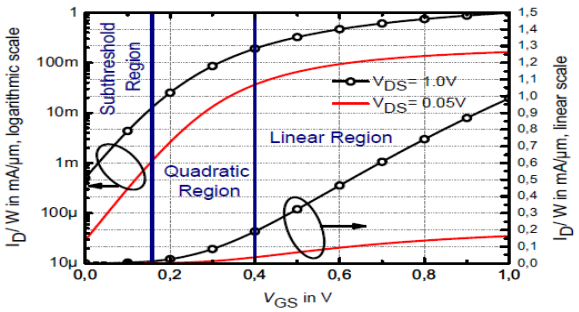

Figure 3: Normalized DC transfer characteristic

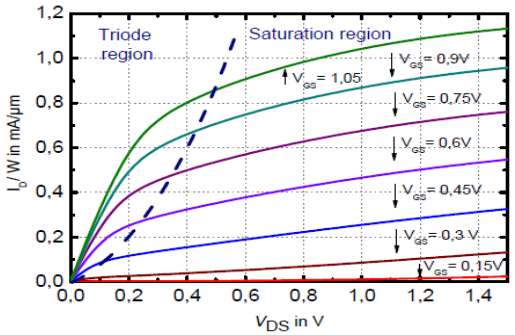

Figure 4: output characteristics of 45nm nmos1v

Figure 3 shows the simulated DC transfer characteristics of a nmos1v n-channel MOSFET with L=45nm gate length. The graph depicts the pinch-off voltage of MOSFET is around 250-280mV. Figure 4. output characteristics of 45nm nmos1v n-channel MOSFET based on the simulation using gpdk models. Here to bias the low noise amplifier it need to be biased at Vgs=0.4V and Vds=1.2 V which yields a current density of 500uA/um.

III. PERFORMANCE METRICS OF LOW-NOISE AMPLIFIER

The performance metrics to be considered in designing an amplifier are small signal gain, input matching network, and output matching network, stability and band width. The general two port network of an amplifier is depicted in Figure 5.

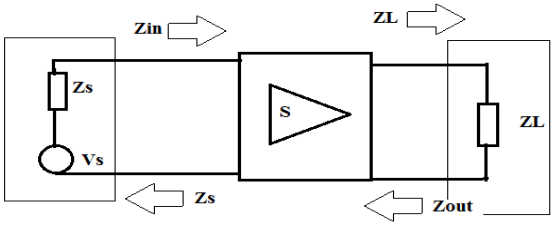

Figure 5: Two-Port network of an amplifier

A. Power Gain:

Power Gain is defined as

$$G = \frac{P_L}{P_{in}} = \frac{power\ dissipated\ at\ load}{power\ delivered\ to\ input} \quad (1)$$

Transducer gain G_T is defined as

$$G_T = \frac{P_L}{P_a} = \frac{power\ dissipated\ in\ load}{power\ available\ from\ source} \quad (2)$$

Available gain G_A is defined as

$$G_A = \frac{P_{AT}}{P_a} = \frac{power\ available\ from\ two\ port\ network}{power\ available\ from\ source} \quad (3)$$

B. Linearity

The linearity issue existed depending on type of modulation scheme incorporated in modulation. In transmitter section if the amplitude modulation is incorporated then the power amplifier need to be linear region. In power amplifier the trade-off exist between efficiency and linearity. Assume that the input given to designed power amplifier is amplitude modulated wave ($V_{in}(t)$), if the power amplifier is highly non-linear in nature. Then output of the amplifier V_d is given by

$$V_d = AV_{in}(t) = a_1V_{in}(t) + a_2V^2{}_{in}(t) + a_3V^3{}_{in}(t) \quad (4)$$

This non-linearity need to be minimized in amplitude modulated output for recovering the information present in the envelop of the output.

C. Matching and Linearity

To get minimum noise figure using transistor the power reflection coefficient should match with Γ_{out}^* and load reflection coefficient should match with Γ_{out}

$$\Gamma_s = \Gamma_{opt}$$

$$\Gamma_L = \Gamma_{out}^* = \left(S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \right) \quad (5)$$

The overall performance of power amplifier is determined by calculating GT. The proposed power amplifier MOSFET works at a power supply voltage of 1.8V. It is designed to deliver a output power of 10mW. It ensures the P1dB of 11.7dB and Γ_{opt} of 0.815+j0.2209. The stability of the design is ensured with the equation given 6 and 7.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} = 1.57 > 1 \quad (6)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} = 0.19 < 1 \quad (7)$$

D. Noise Figure

The one more component which need to be considered in designing low noise amplifier is its noise figure. Generally it is difficult to design an amplifier which gives low noise figure and high gain. Considering this issue

trade-off is done between gain and noise figure to design consider constant gain circle and circle of constant noise figure. The noise figure is defined as

$$F = F_{\min} + \frac{R_N}{G_S}\left|Y_S - Y_{opt}\right|^2 \quad (8)$$

Where
Ys= source admittance
Yopt=source admittance results in minimum noise figure
Fmin=minimum noise figure when Ys=Yopt
R_N= Equivalent noise resistance
Gs= real part of source admittance

IV. DESIGN OF LNA AT 60GHz

The important objective of LNA is to boost the low signals without appending the noise and for large signals it should intensify without establishing any distortion. As operating frequency is elevated, the threat in depicting LNA to endure its essentials increases. Some are (i) distributed parasitic affects the terminal impedance disturbing the resonant frequency of interest (ii) Scaling introduces short channel effects which degrade the performance of the circuit. Limit in the FOMs (Figure of Merit) of the device such as f_T and $f_{max.}$ The basic LNA structure is shown in the figure 6. Which comprises of source degenerated cascode amplifier. Proper DC bias has been given. This circuit is based on attaining concurrent input matching with power contrived specification for attaining optimal noise figure. The transistor Q_2 is in common gate configuration and configures cascode with Q_1. Size of Q_2 transistor is approximately equal to that of Q_1. The transistor Q_2 is included in the circuit to minimize the direct coupling between the input and output. The load inductance increases the gain, as the current in an inductor will not change instantaneously. At the input side proper selection of L_g and L_s cancels the reactance offered.

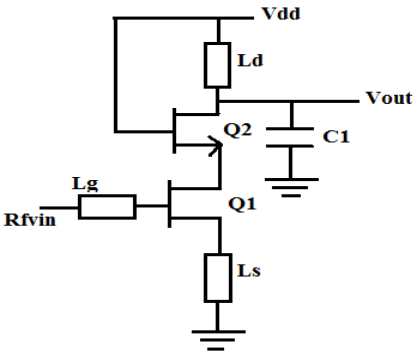

Figure6: Basic source degenerated LNA

Current mirror circuit

Directed towards the evaluation of the proposed circuit, we have chosen a basic current mirror circuit as shown in the Figure 7. It consists of two branches that are parallel to each other and create two approximate equal currents. Let us consider the transistor M1 and M2 to be in saturation region

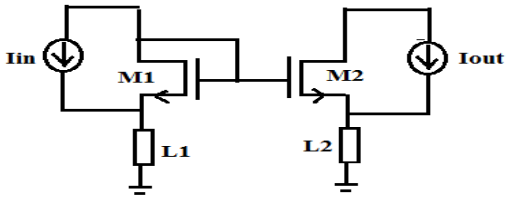

Figure7: Basic current source

$$\frac{I_0}{I_{ref}} = \frac{W_2}{W_1}$$

For foremost enforcements, transistors should be matched and collector-base/drain-gate voltages should also be matched. This choice of circuit that has been taken as the output feedback plays a major role in elevating the gain of the LNA. The small signal model of current mirror and small signal model for low noise amplifier is shown in figure 8 and figure 9 respectively.

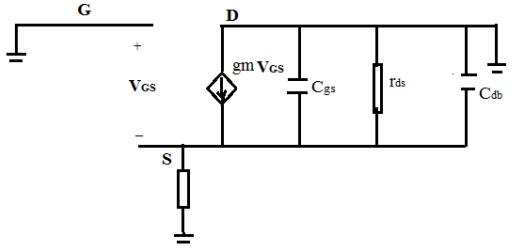

Figure8: Small signal model of current mirror

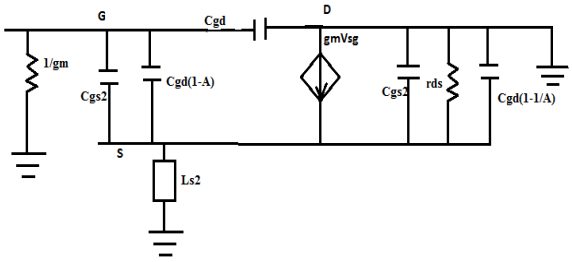

Figure9 Small signal model low noise amplifier

$$Zin_{CM} = \frac{1}{g_m} \parallel \left[\left(\frac{1}{SC_1} \parallel \frac{1}{SC_2}\right) + SL_{S2}\right]$$
$$Zin = Zin_{LNA} \parallel Zin_{CM}$$

A. Diode connected load

One more crucial criterion for LNA is to have a low noise figure. This can be achieved by a perfect input impedance matching.

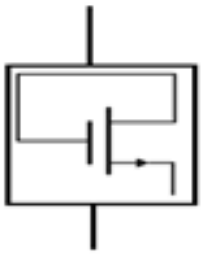

Figure10: basic diode connected load

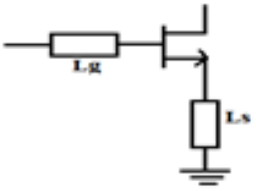

Figure11: Source degenerated low noise amplifier

This can be achieved by a resistor placed at the gate. Rather than using a resistor which is a noisy component, a MOSFET which acts a

resistor by connecting gate and drain. This MOSFET can be used as diode connected load. The circuit diagram of basic diode connected load is depicted in figure 10.

B. Source degeneration

Source degeneration can help obtaining a minimum noise figure and good input return loss simultaneously. In source degeneration either source may be connected to resistor or inductor. As resistor occupies more space in the layout inductor is used. Usage of inductor acts as a negative feedback to the circuit which increases the noise figure by decreasing the gain. The small signal equivalent model of source degeneration for proposed circuit. In reality the input of device is reactive, with real capacitive impedance due to $C_{gs.}$ In order to remove the capacitive reactance and therefore restore the FET input to a pure resistance, one way of achieving this is to add inductive feedback to the source. Additionally another inductor is added in series with the gate Lg that is selected to resonate with the C_{gs} capacitor. The circuit diagram of source degenerated block of low noise amplifier is depicted in figure 11. Lg is designed so that at the resonate frequency it cancels out Cgs. The overall performance of low noise amplifier is determined by calculating GT. The proposed LNA MOSFET works at a power supply voltage of 1.8V. It is designed to have noise figure of 1.002dB. It ensures the P1dB of 11.7dB and Γ_{opt} of 0.815+j0.2209. The stability of the design is ensured with the equation given 10 and 11.

$$K = \frac{1-\left|S_{11}\right|^2-\left|S_{22}\right|^2+\left|\Delta\right|^2}{2\left|S_{12}\right|\left|S_{21}\right|} = 1.57>1 \qquad (10)$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} = 0.19<1 \qquad (11)$$

The equation for K and Δ ensures the unconditional stability of the circuit. From the figure it arbitrary assumed that the current density considered for low noise amplifier is 450uA/um. To enhance the gain and maintain the P1dB and noise figure number of active amplifying stages are increased.

V. PROPOSED METHODOLOGY

Figure 12 shows the proposed LNA circuit comprising of all the components designed in the subsections from I to iii. This is an cascoded amplifier which constitutes the inductive load Ld and Lg2 to nullify the capacitive reactance effects that is C_{gs} and Cdb on the circuit. The output matching is achieved with the better matching circuit which improves the stability. The proposed LNA is shown in figure 7. Here cascode transistor Q2 is used to reduce the interaction of tuned output with tuned input. The Zout of the circuit is purely capacitive in nature, Ld load inductance used to resonates the total capacitance at the drain of Q2. This gives desirable higher gain at designed frequency. If narrow band response is required the input and output are commonly set. Transistor Q3 and Q4 forms a current mirror width of Q3 and Q4 are maintained to generate the desired current. The current through Q3 is set by output voltage. Gate biasing is provided by resistor designed by transistor Q5 implemented as diode connected load. The dc blocking capacitor C1 and C2 are used to prevent the variation of gate to source voltage of Q1 and output.

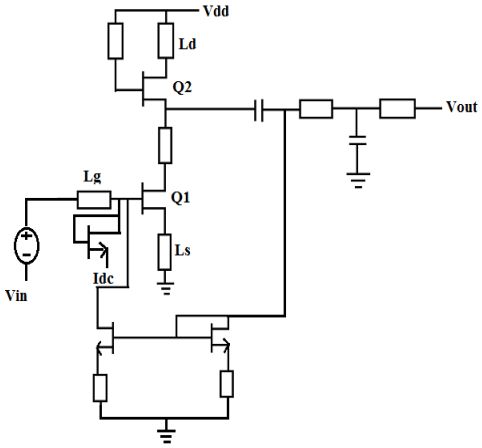

Figure12: proposed LNA with active current feedback

At designed frequency these blocking capacitors have negligible reactance. Some-times these capacitors are off-chip depending on the die area required. The circuit can be designed for operating frequency 60GHz, a 50Ω source resistance and a 50uA of bias current of Q1. Let's assume the data for 45nm technology Leff is 38nm Cox=5fF/mm2. With this basic information width of main transistor Q1=7.5um at a bias current of 50uA. The unity gain frequency of this 45nm technology is about 120GHz, and the factor of α is found to be 0.85. Pessimistically assume that γ=2from the equation. From the equation 8 minimum noise figure is computed as 1.51dB, next the value of source degeneration inductance. To generate an input impedance of 50Ω Ls must be approximately 12nH considering the effect of Cgd. In order to compute Lg, Cgs of the selected device is approximately 200fF, to resonate this capacitor at resonating frequency 60GHz total inductance is about 35pH. Therefore Lg can be computed as 23pH. The design can be completed with the design of dc blocking capacitor which will be selected as 1pF in this design. In current mirror circuit to generate similar current same width is maintained for both main transistor and bias transistor. Here simple reference current source is used, it is advantageous to use constant –gm bias source to stabilize gain and input impedance temperature and supply. The cascode transistor is selected to have the same width as main transistor to some extent it can reduce the effect of miller capacitor. The gate and drain overlap capacitor can reduce the impedance looking in to the gate and drain terminals of M1 which in turn degrades the noise performance and input match. Figure13, depicts the small signal equivalent model of overall circuit

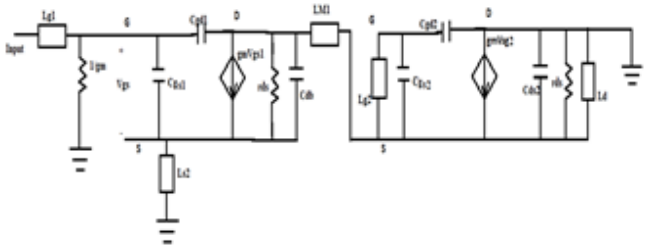

Figure13: small signal model of proposed LNA

The input impedance of the overall circuit is given

$$Zin = \frac{g_m L_s}{C_{gs}} + SL_s + \frac{1}{SC_{gs}}$$

VI. RESULTS & DISCUSSION

The simulation of power amplifier is done by using a standard 45 nm CMOS process using Cadence virtuoso.

A. S- Parameter Analysis

The abbreviation S refers to scattering. Throughout the high frequencies, it is favorable to construct a given network in terms of microwaves than with voltages or currents. In occurrence, if we have 2 ports, then S11, S12, S21 and S22 represents input voltage reflection, reverse voltage gain, forward voltage gain and output voltage reflection respectively. S-parameters interpret the input-output analogy in the midst of ports in an electrical system. S11 expresses the power echoed from the antenna, Accordingly the input return loss(S11) simulated is -18dB at 63GHz as depicted in Figure 14.Through designing input matching circuit of maximum S11 can be accomplished. Extended with the above framework, the proposed PA attains an average gain S21 of10dB at 63GHz which is recognized as the frequency forward transmission coefficient is depicted in the Figure 15.

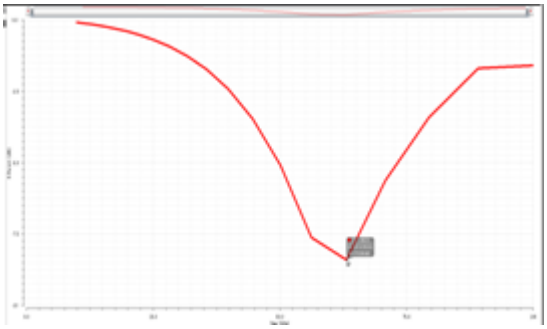

Figure14: S-Parameter S11 output

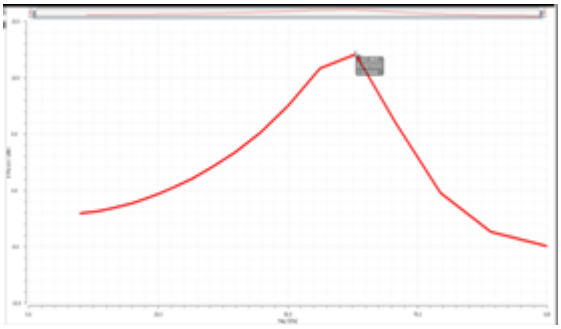

Figure15: S-parameter S21 output

B. Noise Figure

Noise figure (NF) is measures of degradation of the signal-to-noise ratio (SNR), caused by components in a radio-frequency (RF) signal chain. It is a number by which the performance of an amplifier or a radio receiver can be specified, with lower values indicating better performance. For a low noise amplifier the noise figure should be as low as possible. Obtaining an optimum noise figure at 60GHz is laborious job. The proposed circuit has obtained a noise figure less than 2 at the operating frequency. The Figure 16 shows the noise figure at operating frequency.

C. Layout of proposed LNA

Part of the manufacturing process which allows for the repetitive assembly of highly standardized products. When a manufacturing operation utilized product layout, production work can be layout in a straight line with labor and equipment subdivided in a smooth line. The process of calculation the positions of the objects in space give the layout. The layout may be an arrangement, plan or a design. The layout has been simulated in layout editor which has been depicted in Figure 17 for the proposed circuit. The die area of the proposed PA occupies 0.1075μm^2.

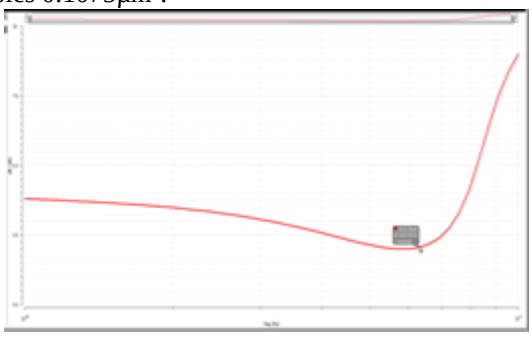

Figure16: Noise Figure

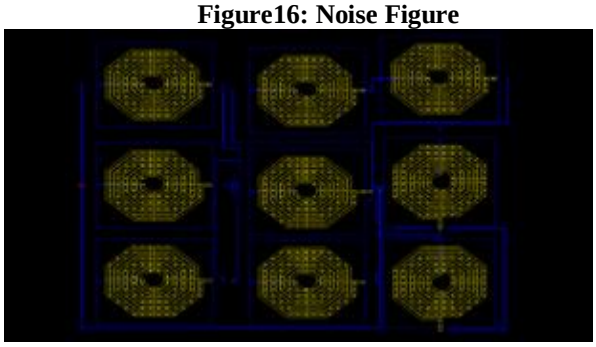

Figure17: Layout of proposed LNA

VII. CONCLUSION

In this paper, a narrow band LNA with a current mirror feedback technique has been presented. This circuit has been designed and simulated in a CADENCE VIRTUOSO 45nm technology. This LNA has a gain up to 13dB with a noise figure of 2dB for 60GHz frequency range.

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