Novel Architecture for Binary Multiplication

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ABSTRACT: ***Multipliers is the basic unit for all signal processing applications and other applications. In all technology advancement it plays a vital role, the targets are low power consumption, increase in speed, reduction in area etc. The computations that are done by a modern computers that includes microcomputers and microprocessor is astronomical. Even with the high speed computer chips the process of the data coming from the devices all over the world requires efficient algorithms and to achieve the compatibility we need to use the chip area effectively. The most often encountered computation in data processing or signal processing is the operation of multiplication. This architecture is to present a novice solution to reduce the total area of the multiplier by modifying the partial products addition multiplier. Generally, to compute the data with high speeds modern hardware uses the Wallace tree or dadda multiplication techniques. By reducing the number of partial products addition the number of gates can be reduced used to obtain the final result. In this proposed method we reduced the real-estate of the chip by using more number of full adder in the earlier stages of the partial products addition which is not present in the conventional multipliers.***

I INTRODUCTION

Multiplication is important unit in both general purpose and digital signal processors. A binary multiplier is a digital circuit which is used to multiply two binary numbers. But depending on the representation used to store and compute the data there will be some changes in the rules of multiplication and their complexity as well as efficiency.

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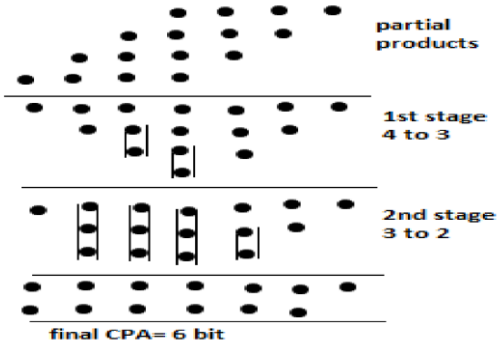
For example to multiply two large magnitude numbers which are commonly encountered in astrological computations we require more store registers and time taken by the hardware is more. Similarly, to calculate the product of two infinitesimal numbers it requires more space and tedious work for the hardware. In such cases regular representation of numbers is less effective. As a solution, the representation large or very small numbers is done by using Floating Point representation. For the representation of numbers in floating point IEEE 754 specified a standard on which the data is stored and processed. The basic rules of binary multiplication are governed by the way an AND gate functions when the two bits to be multiplied are fed as inputs to the gate.

Fig 1: A Wallace tree



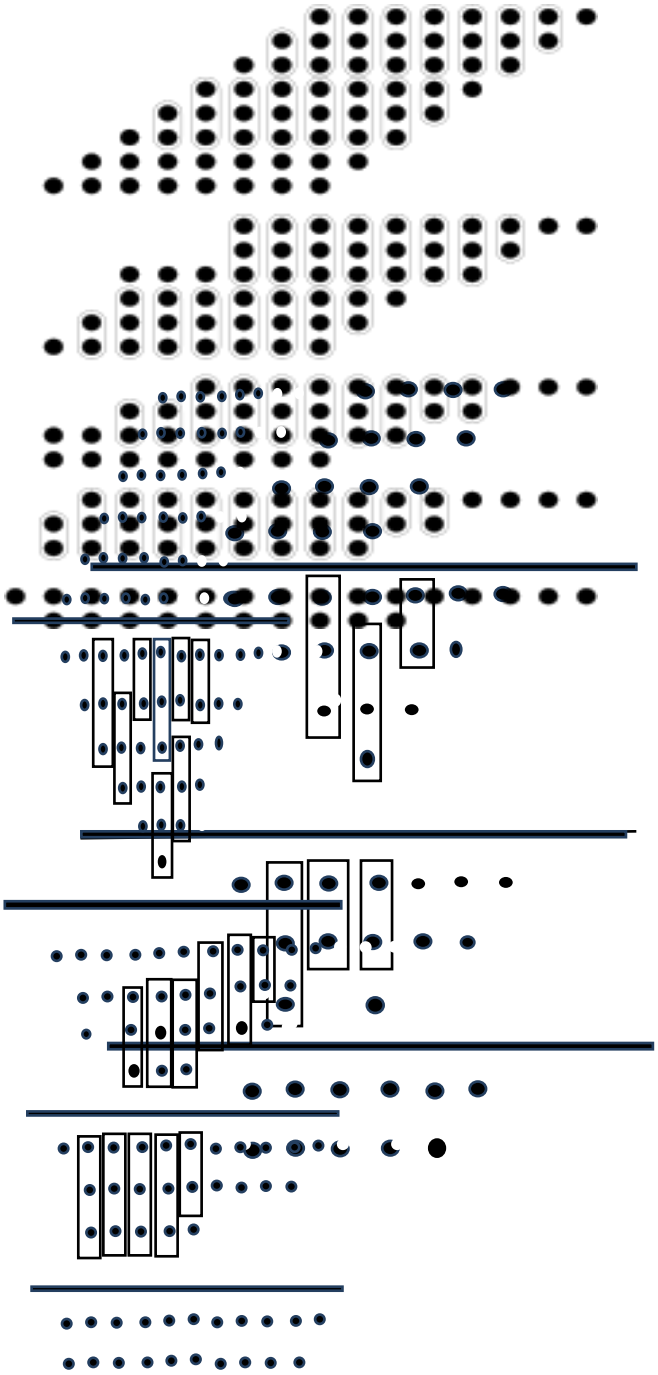
II.MULTIPLIERS

The multipliers use certain algorithms and hardware arrangement techniques to multiply the binary numbers depending on the application. Certain algorithms such as Booth's algorithm are efficient for some computations. The parallel multipliers are faster and more fancied. There are many ways and schemes available for multiplication, such as Array multiplication scheme, Booth multiplication and Vedic multiplication etc.

A .Wallace Tree Multiplier

A **Wallace tree** multiplier is devised by Chris Wallace in 1964. In Wallace tree architecture, partial products bits from columns are added together by a set of counters in parallel to

avoid propagating any carries, Which in turn reduces this new matrix and so on, until a two-row matrix is generated. The common counter used is the 3:2 counter which is a Full Adder.. The end results are added using usually carry propagate adder.



B. Dadda-Multiplier:

This multiplier reduces two-rowed partial products also reduces stages. Dadda succeeded this, by placing the [3,2] and [2,2] counters in the Critical path. Dadda reduced these Matrix height to a two-rowed matrix, through a sequence a reduction stages.

III.BY 4 ARCHITECTURE FOR MULTIPLICATION

This methodology is to multiply the two 4 bit

Fig 2: By 4 Architecture For Multiplication

numbers by using maximum number of full adders to reduce the unused bits at each level so that we are able to reduce the area that is required to perform the multiplication. As we are not using any generic methodology for all the bits it is hard to find the number of adders that are used at each stage and to the overall architecture. But by using this method the area occupied to generate the product of the binary numbers by binary multipliers can be reduced.

In the 4 by 4 architecture the partial products are obtained by using regular methods such as by using simple two input AND gates. These partial products are added at the first stage by using two full-adders and one half-adder which remain seven unused bits and 8 sum bits and 3 carry bits as well. These carry bits and the unused bits are propagated to the next stage where we use one full-adder and two half-adders. The whole process is depicted as below:

IV. RESULT

The following table gives the information about the hardware. It tells about the number of adders, CPA (carry propogation adder) in different multipliers that are DADDA Multiplier, FULL DADDA Multplier, WALLACE Multiplier, PROPOSED Multiplier.as you can see in below block diagram the number of half adders and the full adders used in DADDA multiplier, full dadda multiplier proposed multiplier are same compared to the Wallace multiplier but when compared to the CPA size Wallace multiplier is much better than the remaining multipliers.

TABLE1

	DADDA Multiplier		
	HA	*FA*	*CPA-Size (bit)*
4 by 4	*3*	*3*	*6*
6 by 6	*5*	*15*	*10*
	FULL DADDA Multiplier		
	HA	*FA*	*CPA-Size (bit)*
4 by 4	*3*	*3*	*6*
6 by 6	*5*	*15*	*10*
	WALLACE Multiplier		
	HA	*FA*	*CPA-Size (bit)*
4 by 4	*3*	*5*	*4*
6 by 6	*10*	*15*	*7*
	PROPOSED Multiplier		
	HA	*FA*	*CPA-Size (bit)*
4 by 4	*3*	*3*	*6*
6 by 6	*5*	*15*	*10*

As we explained in the above diagram we can say the Wallace multiplier is completely failed in order to reduse the adders but the CPA size,stage area in no.of unused bits will be reduced when coming to daddamultiplier,fulldadda multiplier are better in terms of adder but CPA size,theno.of unused bits,stage area will be increased so by considering these two issues wanted to modify the multiplier in terms of adders and stage area, no.of unused bits.when we observe below diagram we can simply say Wallace multiplier is less total stage area when compared to the remaining so in our proposed system we concentrated on no.of unused bits and we tried to reduce no.of unused bits from first stage itself using

less adders than Wallace but in terms of stage area proposed system is better than dadda multiplier and full dadda multiplier because of we used more number of bits in the earlier stage of multiplier.as we can see in the below diagram in the proposed system in the first stage used more no.of bits. that's why stage area will be reduced for the smaller multipliers the stage area of full dadda multiplier and proposed multiplier is almost equal but when we go increasing the multiplier size we can clearly observe the total stage area difference from multiplier to multiplier which will be explained in 6 by 6 multipliers**.**

TABLE 2

For 4 by 4 multipliers	Stage Number	Number of Used-Bits	Number of Unused-Bits	Stage Area
DADDA	1	4	12	4+12*2 = 28
	2	11	5	11+5*2= 21
TOTAL AREA				49
FULL DADDA	1	6	10	6+10*2=26
	2	9	5	9+5*2=19
TOTAL AREA				45
WALLACE	1	10	3	10+3*2=16
	2	8	3	8+3*2=14
TOTAL AREA				30
PROPOSED	1	8	8	8+8*2=24
	2	7	7	7+7*2=21
TOTAL AREA				45
Percentage Difference (45=100%)				8.888 %

As we said earlier the main disadvantage in daddamultiplier,fulldadda multiplier is stage area so if you observe the below diagram stage area is better in full dadda multiplier compared to the dadda multiplier so our target is to show the total stage area in our proposed system is better than the full dadda multiplier for that we used more no.of adders in the earlier stage of partial adding to reduce the no.of unused bits and stage area.by observing the below diagram we can clearly say the total area in proposed multiplier is reduced by two compared to the full dadda so we reduced 1.550% of total stage area in the proposed multiplier by using the less no.of adders this is the biggest advantage in proposed system as we go on increasing the size of multiplier we can reduce more stage area with less adders by using more adders in the earlier stage

TABLE3

For 6 by 6 multipliers	Stage Number	Number of Used-Bits	Number of Unused-Bits	Stage Area
DADDA	1	15	21	15+21*2= 57
	2	17	16	17+16*2= 49
	3	23	5	23+5*2=33
TOTAL AREA				139
FULL DADDA	1	17	19	17+19*2=55
	2	18	13	18+13*2=44
	3	20	5	20+5*2=30
TOTAL AREA				129
WALLACE	1	23	12	23+12*2= 47
	2	20	7	20+7*2= 34
	3	21	3	21+3*2=27
TOTAL AREA				108
PROPOSED	1	24	12	24+12*2=48
	2	17	13	17+13*2=43
	3	14	11	14+11*2=36
TOTAL AREA				127
Percentage Difference (127=100%)				1.550 %

REFERENCES

[1] W.J. STENZEL, W. J. Kubitz and G H Garcia, "A Compact High-Speed Parallel Multiplication Scheme," IEEE TRANSACTIONS ON COMPUTERS, VOL. C-26, NO. 10, OCTOBER 1977.
[2] R. S. Waters and E. E. Swartzlander, "A reduced complexity wallace multiplier reduction," IEEE Transactions on Computers, vol. 59, no. 8, pp. 1134–1137, 2010.
[3] K. C. Bickerstaff, M. J. Schulte, and E. E. Swartzlander, Jr., "Reduced Area Multipliers," in Proceedings of the 1993 International Conference on Application Specific Amy Processors, pp. 478-489, IEEE, 1993.
[4] K'Andrea C. Bickerstaff, Earl E. Swartzlander, Michael J. Schulte, "Analysis of Column Compression Multipliers",15th IEEE Symposium on Computer Arithmetic Proceedings, pp 33-39, 2001.
[5] A. Habibhi and P.A. Wintz "Fast Multipliers," IEEE Transactions on Computers, Vol. C-19, pp. 153-157, 1969
[6] C. S.Wallace, "A suggestion for a fast multiplier," IEEE Transactions on Electronic Computers, vol. EC-13, no. 1, pp. 14–17, 1964.
[7] J. Sklansky, "Conditional-sum addition logic," IRE Transactions on Electronic Computers, vol. EC-9, pp. 226–231, 1960
[8] R. P. Brent and H. T. Kung, "A regular layout for parallel adders," IEEE Transactions on Computers, vol. C-31, no. 3, pp. 260–264.
[9] Wesley Chu, Ali I. Unwala, Pohan Wu, and Earl E. Swartzlander, Jr., "Implementation of a High Speed Multiplier Using Carry Lookahead Adders," 978-14799-2390-8/13, 2013, IEEE.
[10] The Proposed Full-Dadda Multipliers Vikas Kaushik, Himanshi Saini, IJIRST –International Journal for Innovative Research in Science & Technology-2018.

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