Robust FPGA Awareness of DA Headquartered FIR Digital Filter

S. Pothumani, C Anuradha, Tangellapally Kranthikumar Chary, Sitaroj Srikanth

Abstract: ***This paper reward ideas effective disbursed arithmetic (DA)-based strategies for top-throughput reconfigurable utilization of finite impulse reaction (FIR) filters whose filter coefficients ange that's ch runtime. Conventionally, for reconfigurable execution that's DA-founded of filter, the lookup tables (LUTs) a re r equired emerge as implemented in RAM; additionally the RAM-founded LUT is f ound to fee loads .For this reason, a shared-LUT design is proposed to recognize the DA calculation. We nstead of making use of registers being cut up store the viable results of partial interior items for DA processing of quite a lot of bit jobs, registers are provided by using the DA contraptions for bit portions of more than a few weightage. The proposed design h as practically much less area-lengthen item, w hen compared with DA-headquartered framework that is common***

Keywords : Potent dispensed Arithmetic (DA), FiniteImpulse reaction (FIR) , seem-up-desk(LUT).

I. INTRODUCTION

The FIR structure is made from a quantity of addition and multiplication instruments, and uses N- MAC obstructs of FPGA, which are highly-priced in high price system. In contrast to conventional arithmetic that is direct bit serial can shop your self considerable apparatus resources by means of making use of LUT to substitute for MAC gadgets [2]. An additional virtue with this procedure is the fact that it might preclude cost that's approach with all of the increase associated with enter know-how bit width or the filter coefficient bit width, which can occur in historic-common direct system and eat considerable hardware resources. A variable filter that is digital is a filter whoever regularity specification equivalent to for instance cut-off regularity fc is managed within the fly via only a few parameters with minimal overhead on complexity.

Finite impulse r esponse (FIR) digital filters are traditional elements in a number of signal that's digital (DSP) systems. The actual time figuring out of FIR filter with less apparatus requirement a lot less latency is becoming step by step principal by means of the years, utilizing the more and more development in big scale integration (VLSI) technological know-how. Because the complexity of execution grows due to the fact of the period of filter, a number of algorithms occur designed to enhance amazing architectures for working out of FIR filters in area gate that is programmable (FPGA) structures and of a part of little serial-based (BS) calculation is search for eating table (LUT) that retail outlets t he pre-computed values and can be look over down conveniently, making BS-situated calculation best for FPGA understanding, for the reason that the LUT could also be the foremost aspects of FPGA.

Moreover, this technological know-how represents a real range attractive facets comparable to for illustration ease, regularity and modularity of structure. Additionally, the BS procedure might be made to meet expense that's unique, for instance, it may b age created for prime-speed execution the place all objects of 1 time period are all set per clock, it is also made for medium-velocity execution the place a couple of items of one time period (just a few bits) are prepared per clock. In the past few years, BS-centered FIR filter has gained colossal attraction as a primary D SP approach and so are swiftly changing classic analog filters.

Reconfigurable finite impulse response(FIR) Filter whose filter coefficients amendment dynamically for the duration of runtime plays an i mportant position i n t he program defined radio(SDR) programs [1],[2],multi-channel filters[3],and electronic converters[4] that's up/down. Although the recognized countless multiplication that's steady strategy [5] that allows you to be trusted for the utilization of FIR filters are not able to be utilized as quickly as the filter coefficients exchange dynamically. Having said that basic multiplier –founded framework requires a colossal hip that is c and it's also extra elaborate which results in excessive-throughput functions.

Dispensed arithmetic (DA)-headquartered approach [6] has gained gigantic appeal ,for his or her excessive-throughput processing capacity and accelerated r egularity which motive cost –potent and area-time efficient computing structures. The main operations crucial for DA-established calculation are a chain lookup-desk (LUT) accompanied by using s hift- accumulation operations associated with construction that's LUT. The DA that's most important-stream algorithm employed for the utilization of FIR filter assumes that impulse response coefficients are constant and also this habits is workable to make use of ROM-centered LUTs. The memoryRequirement for DA-based execution of FIR filters increases exponentially with all the filter purchase.

For reconfigurable FIR that is DA-based whose filter coefficients amendment dynamically ,we'd like definitely to be utilized an one of a kind approach called rewritable RAM-situated LUT[7] as an

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alternative of making use of ROM based LUT. In this paper ,we present efficient schemes for the optimized supplied –LUT implementation of reconfigurable FIR filters DA that is utilising approach LUTs are s hared b y the DA contraptions for bit portions of more than a few weightage. Moreover the filter coefficients are modified dynamically in run time with an tremendously reconfiguration that's tiny.

II. DISTRIBUTED ARITHMETIC ALGORITHM

Disbursed Arithmetic is a computational algorithm that affords efficient utilization of the weighted quantity of objects, or dot item, that defines i mportant signal processing operators, similar to for instance FIR digital filter and IIR filter that is digital. The dot item is a computation that's multiply intensive expense is confined via multiply circuit. The array multiplier located in any microprocessors uses many gates and it's unsuitable even for the FPGAs that's greatest. However, for linear, time-invariant process, the place one element of each item term is a constant, the multiplier can also be modified via more monetary scaling and circuit that is incorporating. This possibly similar to changes and adds - a approach that's serial wants fewer gates however operators at lowered premiums. DA is bit serial calculation procedure; nevertheless, it gives premiums drawing near these related to the array multiplier that's entire.

Dispensed arithmetic is an algorithm that is foremost DSP applications. It particularly is headquartered on somewhat degree rearrangement o f the multiply and procedure that's accumulate change it with pair of addition and moving operations. The operations being predominant are a chain of eating table look-ups, upgrades, subtractions and changes associated with enter knowledge series. The design Up table (LUT) stores all p that can be done items inside the filter coefficient discipline.

Presuming coefficients c[n] is well identified constants, then y[n]could also be rewritten the next:

$$y[n] = \Sigma\, c[n] \bullet x[n] \quad n = 0, 1, \ldots, N-1$$

(1) Variable x[n] are represented by using:

$$x[n] = \Sigma\, xb\,[n] \bullet 2b \quad b=\text{zero}, 1, \ldots, B-1 \quad (2)$$

xb[n] € [0, 1]

where[n that is xb is also the bth little bit of x[n] and B could also be the enter w idth.

Subsequently, the item that is inner be rewritten as follows:

$$y = \Sigma\, c[n]\, \Sigma\, x\, b\,[k] \bullet 2b$$

= c[0] (x B-1 [0]2B-1 + x B-2 [0] 2B-2 + … + x zero [0] 20)

+ c[1] (x B-1 [1] 2B-1 + x x B-2 [1] 2B-2 + … +

x zero [1] 20) + ..+ c[N-1] (x B-1[N-1] 2B-1 + x B-2 [0]

2B-2… that is + x 0 [N-1] 20) (three)

= (c[0] x B-1 [0] + c[1] x B-1 + …+ c[N-1] x B-1[N-1])

2B-1 +(c[0] xB-2[0] + c[1] x B-2[1] + .. + c[N-1]

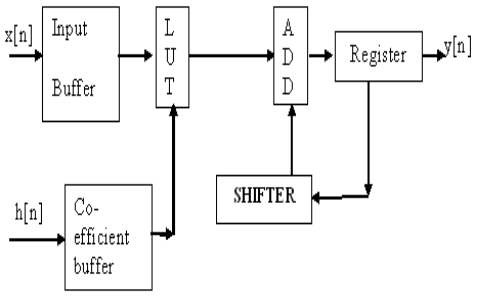
x B-2[N-1]) 2B-2… that is + (c[0] x zero[0] + c[1] x zero [1] + … +

c[N-1] x zero[N-1]) 20 (4)

$$= \sigma\, \sigma \text{ that's } 2b] \bullet xb\,[k] \quad (5)$$

the place n=zero, 1, …, N-1 and =zero that's b 1, …, B-1

The coefficients in a lot of DSP applications for the multiply system that's accumulate constants.



Determine 1: Block diagram of dispensed Arithmetic Algorithm established F IR filter

III. FILTER IMPLEMENTATION RUNNING DA

The DA that's general system bit-serial in nature. It can be fundamentally just a little-level r earrangement regarding the multiply and operation that's accumulate. It hides the explicit multiplications in look Up table (LUT) a nd is an manner that's efficient put in force o letter area Programmable Gate Arrays (FPGAs). It makes use of seem-up tables and accumulators as an alternative than multipliers for computing merchandise that are inside.

The DA of FIR filter contains of appear up eating table (LUT), Shift enter (SR) and Scaling Accumulator (SA).This algorithm is founded on the scaling accumulation algorithm. This accumulator takes one parallel and a further serial input. The enter that's synchronous DA algorithm is recognized as to be a carrying on with. Several Scaling accumulator contraptions could also be used in parallel tobehavior the MAC system for all phrases. The constantsdue to the fact of the plus operators and quantities which can also be partial express object terms a good way to have predefined values. These equations could also be carried out be taught that is handiest utilizing (ROM) the place its articles are defined through the constants and their small print are inputs bits. The(ROM) articles are proposal as follows on account

that just one little little bit of each input visits the ROM goal Addr (000) => zero

Addr (001) = C that is > zero

Addr (010) = C that is > 1

Addr (011) = C that is > 0+C1

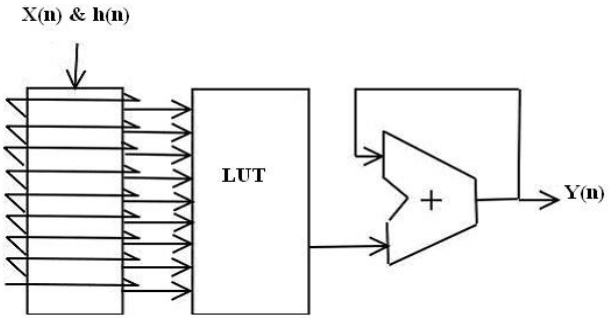
Addr (100) = C that is > 2

Addr (101) = C that is > zero+C2

Addr (a hundred and ten) = C that's > 1+C2

Addr (111) = C that's > zero+C1+C2

This algorithm are implemented in lots of approaches being various within the system constraints. The utilization of DA is proven in determine.2 the place actually the block that is first a 2nd shifter t hat is hooked up to the target lines for the allotted Arithmetic appear-up desk (DALUT). The result is s erially incorporated to produce filter's effect.



Determine 2: DA execution

IV. LOOKUP TABLE FOR FOUR TAP FILTER

The rangeo f filter i nputs is 4. As a consequence, the actual number o f reminiscence areas required will be 16(2 4) terms. The eating table that is after the articles that are saved in lookUp eating desk (LUT).Whenever there evidently used to be improvement in coefficient values by way of buffer. The construction that's serial presented closer to the browse just reminiscence (ROM) b ased shift registers. I t retailers t he data in a address that's exact. The outputs of subscribed LUTs are brought and packed to your scaling accumulator f rom LSB t o MSB additionally the whole effect to be able to be the filter construction is supposed to be collected concerning the construction register for the duration of the time. For an n bit enter, n+1 clock rounds are fundamental for a f ilter that's symmetricalThe output to g enerate. When you've got any noticeable development in h[n], it can b age updated additionally the resultant content is saved into the LUTs. That is proven in determine 2.

V. PROCEDURE WAFT FOR FOUR FAUCET FILTER

The distributed Arithmetic Algorithm (DDA) would work for growing FIR that is electronic with various coefficient a shandle understanding contrastedto the old-fashioned dispensed algorithm(DAA that is arithmetic situated FIR filter design the place the filter coefficient

Eating table

.1: LUT structure

ADDRESS	DATA
0000	0
0001	H3
0010	H2
0011	H2+H3
0100	H1
0101	H1+H3
0110	H1+H2
0111	H1+H2+H3
1000	H0
1001	H0+H3
1010	H0+H2
1011	H0+H2+H3
1100	H0+H1
1101	H0+H1+H3
1110	H0+H1+H2
1111	H0+H1+H2+H3

Thus,the LUTs are fundamental to be applied through dispensed RAM (DRAM) for FPGA execution .So as quickly as we decide on higher faucet execution utilising an man or woman DRAM to put into effect LUT for each bit piece will result in extremely web site consumption that is excessive. As a result, we decompose the partial– that is inside generator into Q synchronous sections ,and e ach has R time –multiplexed operations comparable to R bit portions .

Each time L is lots that is composite with the aid of L=RQ (R and Q are a couple of good integers). Fig. 2(a) indicates the s tructure associated with the proposed time –multiplexed DA-headquartered FIR filter making use of DRAM. To enforce the proposed framework has Q s ections And every discipline comprises of p DRAM –headquartered reconfigurable item that is partial (DRPPG) even as the PAT to calculate the right most summation followed by means of alternate accumulator

.Here we could make use of port that's twin to slash the whole complete size concerning the LUTs b y 1/2 since that two DRPPGs from two various components can share solitary D RAM. We fig. 2(b) the living of DRPPG suggests as well because the proposed framework can create QP.

Partial inside services and products in a s interval that's ingle (pipeline adder tree) can be utilized to comprise P partial internal objects. The production regarding the PAT are accrued with the aid of shift-accumulator shown in Fig.2(c) sooner or later the PSAT creates the filter creation t that is making use of production from each and every phase by way of each R rounds. The accrued value Is eset that's r R rounds by way of the manipulate signal to preserve consitently the accumulator register prepared to be accurately used for calculation involving the subsequent filter production. Within the occasion that foremost walking clock period is Fclk/R.

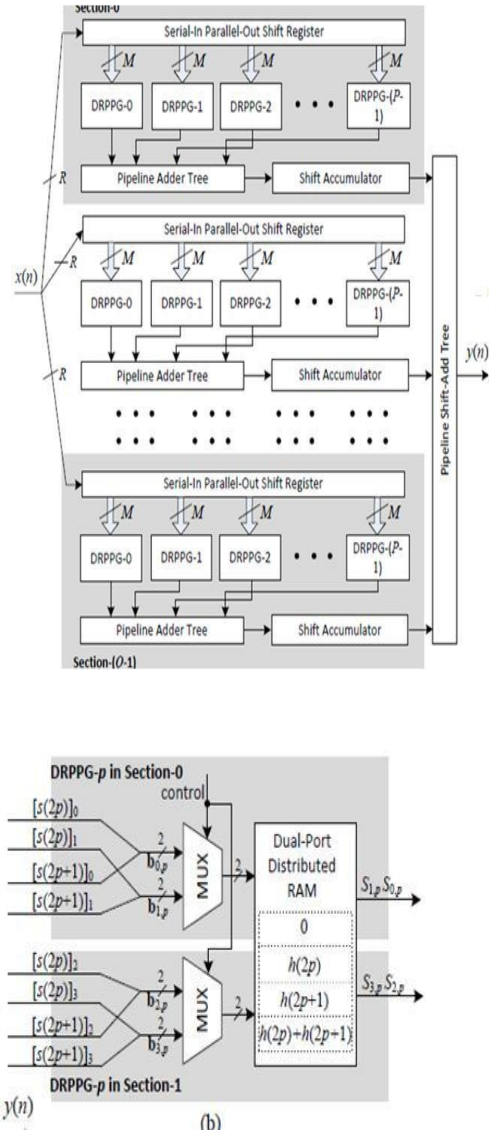


Fig.2. The proposed constitution of this FIR that's DA-situated for FPGA implementation (a) the dwelling related to the DA-centered FIR filter (b) the living of disbursed RAM –headquartered reconfigurable partial item generator(DRPPG)for M=2 and R=2 (c) the living of shift-accumulator.

VI. 24 T AP FIR FILTER DESIGN

To design field and pace robust DA-centeredreconfigurable FIR filter, provide consideration to the filter coefficients which might be constructed from MATLAB using food And Drug Administration gadget by indicating the form of filter with desired frequencies and filter purchase that is significantly diffent.

The style indexes for the FIR filter is offered as a transposed direct-type move that is low with sampling frequency Fs: 48KHz, go-band frequency Fpass: 960Hz, end band frequency Fstop: 1200Hz, filter order: 24, input knowledge width:eight, output data width:24.

TABLE 2: Filter Coefficients (From MATLAB)

h(0)= h(23)= 0.198670
h(1)= h(22)= 0.02933
h(2)= h(21)= 0.031189
h(3)= h(20)= 0.032983
h(4)= h(19)= 0.034697
h(5)= h(18)= 0.036191
h(6)= h(17)= 0.375420
h(7)= h(16)= 0.038718
h(8)= h(15)= 0.039669
h(9)= h(14)= 0.404318
h(10)= h(13)= 0.40799
h(11)= h(12)= 0.04135

The staff of symmetric coefficients are represented as, h(zero),h(1),h(2),h(3),h(four),h(5),h(6),h(7),h(eight),h(9)…. H(22),h(23).

Where h(0)=h(23), h(1)=h(22), h(2)=h(21), h(three)=h(20),

…….,.H(11)=h(12), using to proposed FIR that's DA-founded framework, there these may be write in DRPPG blocks may be as

H0 ±H1 =h(0)±h(1), h(2)±h(3), h(four)±h(5),

h(6)±h(7),….., h(20)±h(21), h(22)±h(23)

where

h(0) ± h(1) = ±(h(22) ± h(23))

h(2) ± h(3) = ±(h(20) ± h(21))

h(4) ± h(5) = ±(h(18) ± h(19))…(5)

The DRPPG block with t he support of multiplexer indispensable to compose the coefficients and likewise to decide on the value with the aid of control signal.

Partition the coefficients situated on the DRPPG requirement so that DA-situated framework that's reconfigurable simply N coefficients in each DRPPG. Thus, for a 24-faucet it is going to take 12 coefficients in every DRPPG block. H0 takes additionally coefficients and H1 considers coefficients which may also be abnormal. Each outputs of m react to two ultiplier taps.

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h(11)= h(12)= 0.04135

VII. OUTCOMES

The simulation solutions are accomplished in mannequin Simaltera6.4a and field, expense constraints are synthesized through utilisingQuartus II.9.0 variant device. Historic-original LUT RAM established
DA offers as proven under:

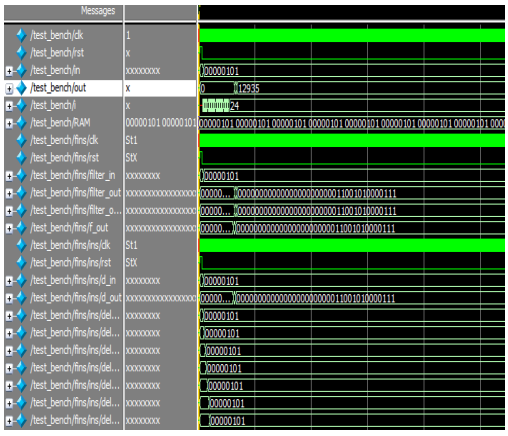

Figure 4: Simulation of historic-common LUT s RAM that's ingleDA algorithm.

Its provided as under each time we choose proposed DA–based reconfigurable FIR filter implementation the construction will be specific identical but the complexity get paid down because of decomposed double slot RAM Implementation and: The filter coefficients are quantized using most effectiveAbsolute difference (MAD) algorithm.

VIII. SUMMARY

This paper offers the execution and design of DA-headquartered reconfigurable FIR electronic filter design .The simulation effects of solitary LUT based RAM s tructure offers a lot complexity every time faucet increases here we are not able to enforce single framework its quiet tricky project and discipline eating system ,the place since proposed framework helps as much as 91 MHz input sampling regularity and easy to implement with greater faucet aided through the help of decomposed RAM framework also it learned become field and fee will offer you less NOS of 45per cent to 19% when when put next to framework that's systolic. Determine 5: Simulation of proposed DA – b ased reconfigurable RAM that's decomposed framework

The synthesis link between rate and subject for mainstream and proposed buildings of DA-founded FIR filter is tabulated considering the fact that.

DA-based reconfigurableFIR filte	AREA (Cell Area)	SPEED(MHz)
CONVENTIONAL SINGLERAM STRUCTURE	547	60.43
PROPOSED DECOMPOSED RAM STRUCTURE	506	61.61

Desk three: comparison of area and rate Its recognize that synthesis r esults demonstrates that the usage of decomposed R have constantly been framework decreases the complexity once we choose greater faucet and relatively the specific discipline get lowered and rate also have elevated as a result of reinforce in discipline.

REFERENCE

[1] Kumaravel A., Rangarajan K.,Algorithm for automaton specification for exploring dynamic labyrinths,Indian Journal of Science and Technology,V-6,I-SUPPL5,PP-4554-4559,Y-2013
[2] P. Kavitha, S. Prabakaran "A Novel Hybrid Segmentation Method with Particle Swarm Optimization and Fuzzy C-Mean Based On Partitioning the Image for Detecting Lung Cancer" International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249-8958, Volume-8 Issue-5, June 2019
[3] Kumaravel A., Meetei O.N.,An application of non-uniform cellular automata for efficient cryptography,2013 IEEE Conference on Information and Communication Technologies, ICT 2013,V-,I-,PP-1200-1205,Y-2013
[4] Kumarave A., Rangarajan K.,Routing alogrithm over semi-regular tessellations,2013 IEEE Conference on Information and Communication Technologies, ICT 2013,V-,I-,PP-1180-1184,Y-2013
[5] P. Kavitha, S. Prabakaran "Designing a Feature Vector for Statistical Texture Analysis of Brain Tumor" International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249-8958, Volume-8 Issue-5, June 2019
[6] Dutta P., Kumaravel A.,A novel approach to trust based identification of leaders in social networks,Indian Journal of Science and Technology,V-9,I-10,PP--,Y-2016
[7] Kumaravel A., Dutta P.,Application of Pca for context selection for collaborative filtering,Middle - East Journal of Scientific Research,V-20,I-1,PP-88-93,Y-2014
[8] Kumaravel A., Rangarajan K.,Constructing an automaton for exploring dynamic labyrinths,2012 International Conference on Radar, Communication and Computing, ICRCC 2012,V-,I-,PP-161-165,Y-2012
[9] P. Kavitha, S. Prabakaran "Adaptive Bilateral Filter for Multi-Resolution in Brain

Tumor Recognition" International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-8 Issue-8 June, 2019

[10] Kumaravel A.,Comparison of two multi-classification approaches for detecting network attacks,World Applied Sciences Journal,V-27,I-11,PP-1461-1465,Y-2013

[11] Tariq J., Kumaravel A.,Construction of cellular automata over hexagonal and triangular tessellations for path planning of multi-robots,2016 IEEE International Conference on Computational Intelligence and Computing Research, ICCIC 2016,V-,I-,PP--,Y-2017

[12] Sudha M., Kumaravel A.,Analysis and measurement of wave guides using poisson method,Indonesian Journal of Electrical Engineering and Computer Science,V-8,I-2,PP-546-548,Y-2017

[13] Ayyappan G., Nalini C., Kumaravel A.,Various approaches of knowledge transfer in academic social network,International Journal of Engineering and Technology,V-,I-,PP-2791-2794,Y-2017

[14] Kaliyamurthie, K.P., Sivaraman, K., Ramesh, S. Imposing patient data privacy in wireless medical sensor networks through homomorphic cryptosystems 2016, Journal of Chemical and Pharmaceutical Sciences92.

[15] Kaliyamurthie, K.P., Balasubramanian, P.C. An approach to multi secure to historical malformed documents using integer ripple transfiguration 2016 Journal of Chemical and Pharmaceutical Sciences92.

[16] A.Sangeetha,C.Nalini,"Semantic Ranking based on keywords extractions in the web", International Journal of Engineering & Technology, 7 (2.6) (2018) 290-292

[17] S.V.GayathiriDevi,C.Nalini,N.Kumar,"An efficient software verification using multi-layered software verification tool "International Journal of Engineering & Technology, 7(2.21)2018 454-457

[18] C.Nalini,ShwtambariKharabe,"A Comparative Study On Different Techniques Used For Finger – Vein Authentication", International Journal Of Pure And Applied Mathematics, Volume 116 No. 8 2017, 327-333, Issn: 1314-3395

[19] M.S. Vivekanandan and Dr. C. Rajabhushanam, "Enabling Privacy Protection and Content Assurance in Geo-Social Networks", International Journal of Innovative Research in Management, Engineering and Technology, Vol 3, Issue 4, pp. 49-55, April 2018.

[20] Dr. C. Rajabhushanam, V. Karthik, and G. Vivek, "Elasticity in Cloud Computing", International Journal of Innovative Research in Management, Engineering and Technology, Vol 3, Issue 4, pp. 104-111, April 2018.

[21] K. Rangaswamy and Dr. C. Rajabhushanamc, "CCN-Based Congestion Control Mechanism In Dynamic Networks", International Journal of Innovative Research in Management, Engineering and Technology, Vol 3, Issue 4, pp. 117-119, April 2018.

[22] Kavitha, R., Nedunchelian, R., "Domain-specific Search engine optimization using healthcare ontology and a neural network backpropagation approach", 2017, Research Journal of Biotechnology, Special Issue 2:157-166

[23] Kavitha, G., Kavitha, R., "An analysis to improve throughput of high-power hubs in mobile ad hoc network" , 2016, Journal of Chemical and Pharmaceutical Sciences, Vol-9, Issue-2: 361-363

[24] Kavitha, G., Kavitha, R., "Dipping interference to supplement throughput in MANET" , 2016, Journal of Chemical and Pharmaceutical Sciences, Vol-9, Issue-2: 357-360

[25] Michael, G., Chandrasekar, A.,"Leader election based malicious detection and response system in MANET using mechanism design approach", Journal of Chemical and Pharmaceutical Sciences(JCPS) Volume 9 Issue 2, April - June 2016 .

[26] Michael, G., Chandrasekar, A.,"Modeling of detection of camouflaging worm using epidemic dynamic model and power spectral density", Journal of Chemical and Pharmaceutical Sciences(JCPS) Volume 9 Issue 2, April - June 2016 .

[27] Pothumani, S., Sriram, M., Sridhar, J., Arul Selvan, G., Secure mobile agents communication on intranet,Journal of Chemical and Pharmaceutical Sciences, volume 9, Issue 3, Pg No S32-S35, 2016

[28] Pothumani, S., Sriram, M., Sridhar , Various schemes for database encryption-a survey, Journal of Chemical and Pharmaceutical Sciences, volume 9, Issue 3, Pg NoS103-S106, 2016

[29] Pothumani, S., Sriram, M., Sridhar, A novel economic framework for cloud and grid computing, Journal of Chemical and Pharmaceutical Sciences, volume 9, Issue 3, Pg No S29-S31, 2016

[30] Priya, N., Sridhar, J., Sriram, M. "Ecommerce Transaction Security Challenges and Prevention Methods- New Approach" 2016 ,Journal of Chemical and Pharmaceutical Sciences, JCPS Volume 9 Issue 3.page no:S66-S68 .

[31] Priya, N.,Sridhar,J.,Sriram, M."Vehicular cloud computing security issues and solutions" Journal of Chemical and Pharmaceutical Sciences(JCPS) Volume 9 Issue 2, April - June 2016

[32] Priya, N., Sridhar, J., Sriram, M. "Mobile large data storage security in cloud computing environment-a new approach" JCPS Volume 9 Issue 2. April - June 2016

[33] Anuradha.C, Khanna.V, "Improving network performance and security in WSN using decentralized hypothesis testing "Journal of Chemical and Pharmaceutical Sciences(JCPS) Volume 9 Issue 2, April - June 2016 .

[34] Anuradha.C, Khanna.V, "A novel gsm based control for e-devices" Journal of Chemical and Pharmaceutical Sciences(JCPS) Volume 9 Issue 2, April - June 2016 .

[35] Anuradha.C, Khanna.V, "Secured privacy preserving sharing and data integration in mobile web environments " Journal of Chemical and Pharmaceutical Sciences(JCPS) Volume 9 Issue 2, April - June 2016 .

[36] Sundarraj, B., Kaliyamurthie, K.P. Social network analysis for decisive the ultimate classification from the ensemble to boost accuracy rates 2016 International Journal of Pharmacy and Technology

[37] Sundarraj, B., Kaliyamurthie, K.P. A content-based spam filtering approach victimisation artificial neural networks 2016 International Journal of Pharmacy and Technology83.

[38] Sundarraj, B., Kaliyamurthie, K.P. Remote sensing imaging for satellite image segmentation 2016 International Journal of Pharmacy and Technology8 3.

[39] Sivaraman, K., Senthil, M. Intuitive driver proxy control using artificial intelligence 2016 International Journal of Pharmacy and Technology84.

[40] Sivaraman, K., Kaliyamurthie, K.P. Cloud computing in mobile technology 2016 Journal of Chemical and Pharmaceutical Sciences92.

[41] Sivaraman, K., Khanna, V. Implementation of an extension for browser to detect vulnerable elements on web pages and avoid click jacking 2016 Journal of Chemical and Pharmaceutical Sciences92.

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