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Automated Error Detection Inreed-Solomon Encoders

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***Abstract:** Ree omon that is d-SolRS) c odes are mostly us e d to get and proper errors in transmission systems and also s torage de vices . The des igner should also just take into account the event of faults into the encoder and s ubs ys temswhe n RS codes are used for reliable systems . The s RS that is elf-checking enc architecture is presente d i n this paper . The RS encoder architecture age exploits some proper ties regarding the operations which can be arithmetic Galois Field (GF(2m)).Thes e properties are rel ate d to the parity of the bi nar y re presentation regarding the elements associated with the Galois Field.In this paper , enables i mplementing c oncurre mistake that is nttection s che me us eful for a wi de range of different decoding algorithms without any inter venti on in the decoder architecture. More over, performances in terms of area and delayoverhe advertisement for the propos e d ci rcuits are presente d.*

***KEYWORDS:** Galois Field, Encoder, Error detection*

I. INTRODUCTION

Reed-Solo mon codes are block-based error correcting codes with an assortment that is wide of in digital communicat ions and storage. [1, 2, 3].Reed -So lo mon codes are us ed to mistakes which can be proper numerous systems .A s which can be typical is shown here:

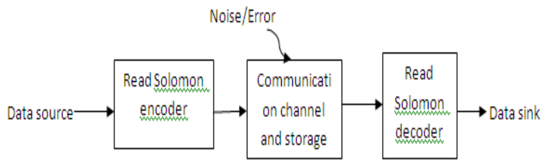

Figure.1:Block diagram of digital co that is l ions system

The Reed-So lo mon encoder takes a block of dig ital information and adds ra that is ext" bits . Mistakes happen during trans mis s ion or s torage for a number of reasons (for age xamplenois disturbance or e, s cratches on a CD, etc). The Reed - Solo mon decoder proces s es each block and tries to correct errors and retrieve the initial information [4,5,6]. The numbe r and sort of mistakes which can be corrected d epends regarding the characteris tics associated with the reed-Solo rule that is mon. Reed-So lo mon codes are block-bas mistake that is eding codes with a broad range of applications in electronic co mmunications and storage space [7,8,9].

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Reed-Solo mon codes are us ed to mistakes which can be proper numerous s ys tems including:
qualities of Ree omon that is d-Sol odesReed Solo mon codes a re a s ubs et of BCH codes a nd are linear block codes . A Reed -So lo code that is mon s pecified as RS(n,k) with s-b it symbols .This ensures that the encoder takes k data s ymbols of s bitseach and adds parity s ymbols in order to make a letter s codeword that is ymbol. There are n-k parity s ymbols of s bits each. A Reed -So lo decoder that is mon correct up to t s ymbols which contain mistakes in a codeword, where 2t = n-k.[10, 11].The diagram that is after s hows a typical Reed -So lo moncodeword (this is understood as a rule that is systematic age the info is kept unchanged while the parity symbols are appended) [12, 13].

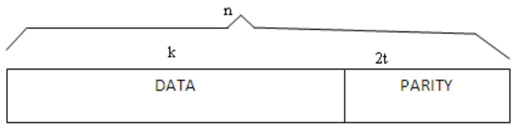

Figure 2: Reed-So lo moncodeword

Example : a Reed-Solo that is popular mon is RS(255,223) with
8-bit s ymbols . Each codeword contains 255 code wordbytes , of which bytes which are 223 information and 32 bytes are parity. With this rule:
letter = 255, k = 223, s = 82t = 32, t = 16

RS Encoder architecture

The parity that is 2t symbols in a systematic Reed -So lo mon code word get by: The following that is shows an architecture for a systematic RS(255,249) encoder: [14, 15].

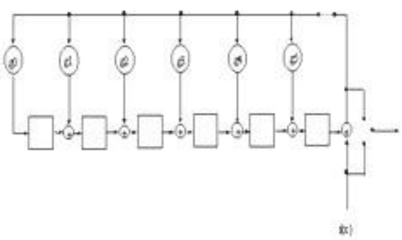

Figure 3: Block diagram of RS Encoder architecture

Each of the 6 registers holds a symbol (8 b its). The arithmetic operatorscarry away itethat is fin ld addition or multiplicat ion on a c omplete symbol.

II PROPOSED SYSTEM IMPLEMENTATION

The blockdiagra m of propos ed BIST-RS ENCODER is s hown above. The purpos which can be primary of BIST-RS ENCODER is whenever encoding the rs encoder it tes t with BIST on -line or off- line [16, 17, 18]. On -line BIST refers to tes ting which occurs during norma procedure that is l f the c ircu it. Examp les with this sort of BIST often h ave to do with practical tes ting s uch as Error Detecting/Error Correcting (ED/ EC) codes or on chip electrica l monitoring. Off-line BIST procedure happens during a s period that is pecified the CUT is idle. Practical tes age that is ting tests bas ed on information of the CUT. It is worried with ensuring that the practical logic regarding the ircuit that is c properly (in other words., ensures an adder circuit adds).this propos ed BIST RS ENC ODER is especially des igned for Xilin x 4000 and Spartan Series FPGAs [19, 20, 21]. Built -In Self-Tes t (BIST) designs that most of this progra logic that is mmable interconnect res ources in the core of Xilin x 4000E,4000XL/ XLA and Spartan Series Fie ldProgrammable Gate Arrays (FPGAs).

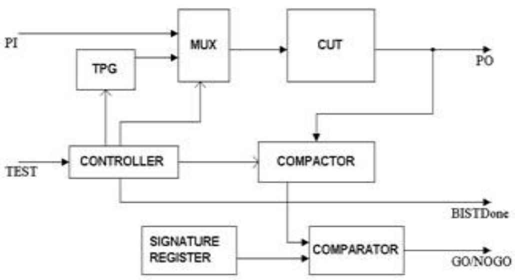

Figure 4: Bloc k diagra m of overall s ys tem des imple mentation that is ign

The propos ed mentation that is imple of overall a rchitecture of most XIlinX4000 and Spartan s eriesFPGAs [22, 23, 24]. FPGAs is identical in that a 2 -dimensional a rray of PLBs is interconnected by a routing system that is programmable. Nevertheless, there are differences between the three ma infamilies we targeted (4000E, 4000XL/XLA, and Spartan) in terms associated with programmable logic that is le inter link res ources [25, 26, 27]. The main advantage of us Xilin that is ing x and Spartan PLB architectures having the less quantity of flip -flops and Look-Up Tables (LUT)The s which are after are used in this paperThe proposed architecture works in 2 cases Whenever Test signal is low When Test signal is high whenever TEST s ignal is minimal (T EST=0) the norma RS that is l Encoding activated. The iple that is mult (MUX) takes the input also it offers to your RS encoder. In this paper the RS encoder is RS (204,188) isused [28, 29]. RS Encoder takes the input as multiple xer s ignal and it age ncodes the s ignal i. that is.e RS encoded output.whenever TEST s ignal is high (TEST =1) the BIST triggered plus it does not takes the input andCUT is triggered.whenever BIST activated the controller s ends a signal to Test Pattern Generation (TPG).

III . RESULTS ANALYSIS

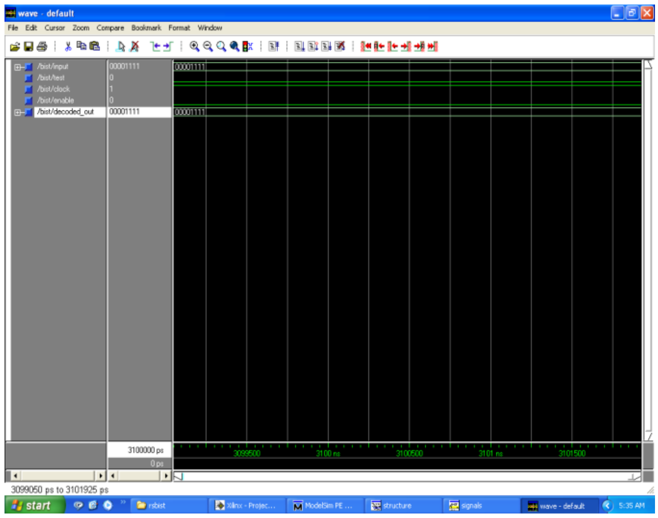

Figure 5: Simulation waveform for RS encoder module

Fig.5 shows the simulation results obtained for the BIST normal mode that is lTes t=0).in this normal mode the input is (7:0).the MUX takes the input plus it offers towards the RS Encoder. the RS Encoder encodes t he input and also the production is provided by it as (7:0).

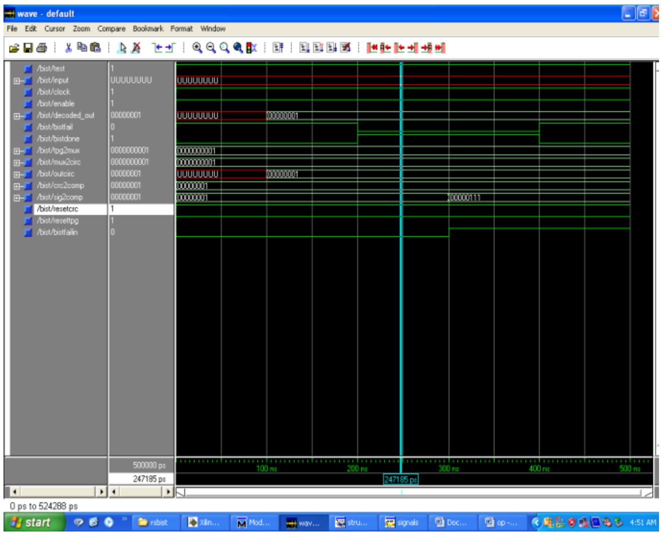

Figure 6: Simulation res ults for imp le mentation of overall s ys tem des module that is ign

Fig.6 s hows the activated BIST done. Meaning the Tes t Signal is high (Tes t=1) and allow is high. When tes help and t is high the controlle r s stops the BIST activated s ignal to your s ys tem. This could be the circuit under tes mode that is tCUT).in this mode CUT is RS Encoder. Whenever BIST is triggered the T PG creates the s ignals . Thes age s ignalsa re inputs to your MUX. The TPG created s ignals are various s ignals (9:0).M UX offers the multip le xed s ignal and it is input towards the CUT(RS Encoder).the input is (9:0) and MUX g ives to your CUT is (1:0).The CUT gives the production as (7:0).This is the normal representation for the b its regarding the polynomia production that is l of CUT. The compactor converts the production that is polynomial to normal representation of bits [30, 31]. This really is fond of the controller to obtain the mistakes out such method is CRC. SIGNATURE REGIST ER module having the Signature gold is understood to be the mean of this coded information is called the s ignature gold [33, 34, 35]. The s ignature gold is 00000001.The co mparator inputs are compactor output (0000000010) and s regis that is ignature value (00000001). The concept regarding the co mparator is co mpares the two inputs a nd provides the s which can be appropriate. The 2 values are s ame in this cas age.s o the comparator provides the BIST DONE signal [36, 37, 38]

Fig 6 s hows theBis t that is triggered fail. The aforementioned procedure is s ame and also by changing the s ignature silver value to s the way the Bis t fail operation.[39, 40]. ThE age comparator co mpares the s ignatureregister co and value mpactor value also it provides the BIST fail signal becaus age the two inputs are very different [41].

IV. CONCLUSIONS

Theis task discounts with concurrent mistake detection in RS encoders . We could attain the erroneous information at encoder s ide and finding the equipment functionality with BIST method by us ing this strategy. The error correcting capability of 8 Symbols (64 b its). The rule us es a s clock that is ingle ssynchronouspurposees . The rule flags the problems and matters the amount of mistakes c orrected and ess that is poss. 64 bits error correcting capability. The quantity of mistakes corrected, s ymbol s codeword and ize size are programmable . The rule also ssupports input that is constant s tream without space between rule obstructs . We are able to inform there are not any mistakes into the RS Encoder by us ing this system. The propos ed mentation that is imple of RS ENCODER overallll arch itecture of a llXilin x 4000 and Spartan s eries FPGAs . FPGAs are identical for the reason that a 2- dimes array that is ional of is interconnected by a programmab le routing network. But, there are differences between the three ma infamilies we targeted (4000E, 4000XL/XLA, and Spartan) in terms of the programmable logic that is le inter link res ources . The benefit of us Xilin that is ing x and Spartan PLB arch tinctureshaving the less quantity of flip -flops and Look-Up Tables (LUT)

REFERENCES

1. Kumarave A., Rangarajan K.,Algorithm for automaton specification for exploring dynamic labyrinths,Indian Journal of Science and Technology,V-6,I-SUPPL5,PP-4554-4559,Y-2013
2. P. Kavitha, S. Prabakaran "A Novel Hybrid Segmentation Method with Particle Swarm Optimization and Fuzzy C-Mean Based On Partitioning the Image for Detecting Lung Cancer" International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249-8958, Volume-8 Issue-5, June 2019
3. Kumaravel A., Meetei O.N.,An application of non-uniform cellular automata for efficient cryptography,2013 IEEE Conference on Information and Communication Technologies, ICT 2013,V-,I-,PP-1200-1205,Y-2013
4. Kumarave A., Rangarajan K.,Routing alogrithm over semi-regular tessellations,2013 IEEE Conference on Information and Communication Technologies, ICT 2013,V-,I-,PP-1180-1184,Y-2013
5. P. Kavitha, S. Prabakaran "Designing a Feature Vector for Statistical Texture Analysis of Brain Tumor" International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249-8958, Volume-8 Issue-5, June 2019
6. Dutta P., Kumaravel A.,A novel approach to trust based identification of leaders in social networks,Indian Journal of Science and Technology,V-9,I-10,PP--,Y-2016
7. Kumaravel A., Dutta P.,Application of Pca for context selection for collaborative filtering,Middle - East Journal of Scientific Research,V-20,I-1,PP-88-93,Y-2014
8. Kumaravel A., Rangarajan K.,Constructing an automaton for exploring dynamic labyrinths,2012 International Conference on Radar, Communication and Computing, ICRCC 2012,V-,I-,PP-161-165,Y-2012
9. P. Kavitha, S. Prabakaran "Adaptive Bilateral Filter for Multi-Resolution in Brain Tumor Recognition" International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-8 Issue-8 June, 2019
10. Kumaravel A.,Comparison of two multi-classification approaches for detecting network attacks,World Applied Sciences Journal,V-27,I-11,PP-1461-1465,Y-2013
11. Tariq J., Kumaravel A.,Construction of cellular automata over hexagonal and triangular tessellations for path planning of multi-robots,2016 IEEE International Conference on Computational Intelligence and Computing Research, ICCIC 2016,V-,I-,PP--,Y-2017
12. Sudha M., Kumaravel A.,Analysis and measurement of wave guides using poisson method,Indonesian Journal of Electrical Engineering and Computer Science,V-8,I-2,PP-546-548,Y-2017
13. Ayyappan G., Nalini C., Kumaravel A.,Various approaches of knowledge transfer in academic social network,International Journal of Engineering and Technology,V-,I-,PP-2791-2794,Y-2017
14. Kaliyamurthie, K.P., Sivaraman, K., Ramesh, S. Imposing patient data privacy in wireless medical sensor networks through homomorphic cryptosystems2016, Journal of Chemical and Pharmaceutical Sciences 9 2.
15. Kaliyamurthie, K.P., Balasubramanian, P.C. An approach to multi secure to historical malformed documents using integer ripple transfiguration 2016 Journal of Chemical and Pharmaceutical Sciences 9 2.
16. A.Sangeetha,C.Nalini,"Semantic Ranking based on keywords extractions in the web", International Journal of Engineering & Technology, 7 (2.6) (2018) 290-292
17. S.V.GayathiriDevi,C.Nalini,N.Kumar,"An efficient software verification using multi-layered software verification tool "International Journal of Engineering & Technology, 7(2.21)2018 454-457
18. C.Nalini,ShwtambariKharabe,"A Comparative Study On Different Techniques Used For Finger – Vein Authentication", International Journal Of Pure And Applied Mathematics, Volume 116 No. 8 2017, 327-333, Issn: 1314-3395
19. M.S. Vivekanandan and Dr. C. Rajabhushanam, "Enabling Privacy Protection and Content Assurance in Geo-Social Networks", International Journal of Innovative Research in Management, Engineering and Technology, Vol 3, Issue 4, pp. 49-55, April 2018.
20. Dr. C. Rajabhushanam, V. Karthik, and G. Vivek, "Elasticity in Cloud Computing", International Journal of Innovative Research in Management, Engineering and Technology, Vol 3, Issue 4, pp. 104-111, April 2018.
21. K. Rangaswamy and Dr. C. Rajabhushanamc, "CCN-Based Congestion Control Mechanism In Dynamic Networks", International Journal of Innovative Research in Management, Engineering and Technology, Vol 3, Issue 4, pp. 117-119, April 2018.
22. Kavitha, R., Nedunchelian, R., "Domain-specific Search engine optimization using healthcare ontology and a neural network backpropagation approach", 2017, Research Journal of Biotechnology, Special Issue 2:157-166
23. Kavitha, G., Kavitha, R., "An analysis to improve throughput of high-power hubs in mobile ad hoc network" , 2016, Journal of Chemical and Pharmaceutical Sciences, Vol-9, Issue-2: 361-363
24. Kavitha, G., Kavitha, R., "Dipping interference to supplement throughput in MANET" , 2016, Journal of Chemical and Pharmaceutical Sciences, Vol-9, Issue-2: 357-360
25. Michael, G., Chandrasekar, A.,"Leader election based malicious detection and response system in

MANET using mechanism design approach”, Journal of Chemical and Pharmaceutical Sciences(JCPS) Volume 9 Issue 2, April - June 2016 .
26. Michael, G., Chandrasekar, A.,”Modeling of detection of camouflaging worm using epidemic dynamic model and power spectral density”, Journal of Chemical and Pharmaceutical Sciences(JCPS) Volume 9 Issue 2, April - June 2016 .
27. Pothumani, S., Sriram, M., Sridhar, J., Arul Selvan, G., Secure mobile agents communication on intranet,Journal of Chemical and Pharmaceutical Sciences, volume 9, Issue 3, Pg No S32-S35, 2016
28. Pothumani, S., Sriram, M., Sridhar , Various schemes for database encryption-a survey, Journal of Chemical and Pharmaceutical Sciences, volume 9, Issue 3, Pg NoS103-S106, 2016
29. Pothumani, S., Sriram, M., Sridhar, A novel economic framework for cloud and grid computing, Journal of Chemical and Pharmaceutical Sciences, volume 9, Issue 3, Pg No S29-S31, 2016
30. Priya, N., Sridhar, J., Sriram, M. “Ecommerce Transaction Security Challenges and Prevention Methods- New Approach” 2016 ,Journal of Chemical and Pharmaceutical Sciences, JCPS Volume 9 Issue 3.page no:S66-S68 .
31. Priya, N.,Sridhar,J.,Sriram, M.“Vehicular cloud computing security issues and solutions” Journal of Chemical and Pharmaceutical Sciences(JCPS) Volume 9 Issue 2, April - June 2016 .
32. Priya, N., Sridhar, J., Sriram, M. “Mobile large data storage security in cloud computing environment-a new approach” JCPS Volume 9 Issue 2. April - June 2016
33. Anuradha.C, Khanna.V, “Improving network performance and security in WSN using decentralized hypothesis testing “Journal of Chemical and Pharmaceutical Sciences(JCPS) Volume 9 Issue 2, April - June 2016 .
34. Anuradha.C, Khanna.V, “A novel gsm based control for e-devices“ Journal of Chemical and Pharmaceutical Sciences(JCPS) Volume 9 Issue 2, April - June 2016 .
35. Anuradha.C, Khanna.V, “Secured privacy preserving sharing and data integration in mobile web environments “ Journal of Chemical and Pharmaceutical Sciences(JCPS) Volume 9 Issue 2, April - June 2016 .
36. Sundarraj, B., Kaliyamurthie, K.P. Social network analysis for decisive the ultimate classification from the ensemble to boost accuracy rates 2016 International Journal of Pharmacy and Technology 8
37. Sundarraj, B., Kaliyamurthie, K.P. A content-based spam filtering approach victimisation artificial neural networks 2016 International Journal of Pharmacy and Technology 8 3.
38. Sundarraj, B., Kaliyamurthie, K.P. Remote sensing imaging for satellite image segmentation 2016 International Journal of Pharmacy and Technology 8 3.
39. Sivaraman, K., Senthil, M. Intuitive driver proxy control using artificial intelligence 2016 International Journal of Pharmacy and Technology 8 4.
40. Sivaraman, K., Kaliyamurthie, K.P. Cloud computing in mobile technology 2016 Journal of Chemical and Pharmaceutical Sciences 9 2.
41. Sivaraman, K., Khanna, V. Implementation of an extension for browser to detect vulnerable elements on web pages and avoid click jacking 2016 Journal of Chemical and Pharmaceutical Sciences 9 2.

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