Automated Error Detection Inreed-Solomon Encoders

S. Pothumanu, Sangeetha. S, N. Priya, B. Sundar Raj

Abstract: Reemon (that is d-SolRS)c codes are mostly us e d to get and proper errors in transmission systems and also s torage de vices . The des igner should also just take into account the event of faults into the encoder and s ubs yt emswhe n RS codes are used for reliable systems . The s RS that is el-checking enc archi tecture is presente d in t his paper. The RS encoder architecture age exploits some proper ties regarding the operations which can be arithmetic Galois Field (GF(2m)).The e properties are relate d to the parity of the binary pre presentation regarding the elements associated with the Galois Field.In this paper , enables i mplementing c once rences which can be typi cally used to mistakes which can be proper numerous systems .A s which can be typical is shown here:

Reed-Solo mon codes are block-based error correcting codes with an assortment that is wide of in digital communicat ions and st orage. [1, 2, 3].Reed -So lo mon codes are us ed to mistakes which can be proper numerous systems .A s which can be typical is shown here:

Example : a Reed-Solo that is popular mon is RS(255,223) with 8-bit s ymbols . Each codeword contains 255 code wordbytes , of which bytes which are 223 information and 32 bytes are parity. With this rule: letter = 255, k = 223, s = 82t = 32, t = 16

RS Encoder architecture

The parity that is 2t symbols in a systematic Reed -Solo mon code word get by: The following that is shows an architecture for a systematic RS(255,249) encoder: [14, 15].

Each of the 6 registers holds a symbol (8 b its ). The arithmetic operators carry away itethat is fin ld ad dition or multiplicat ion on a c omplete symbol.
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II. PROPOSED SYSTEM IMPLEMENTATION

The block diagram of the proposed BIST-RS ENCODER is shown above. The purpose which can be primary of BIST-RS ENCODER is whenever encoding the RS encoder it tests either BIST on-line or off-line [16, 17, 18]. On-line BIST refers to testing which occurs during normal procedure that is if the circuit is in use. Examples with this sort of BIST often have to do with practical testing such as Error Detecting/Error Correcting (ED/EC) codes or on-chip electrical monitoring. Off-line BIST procedure happens during a specified period that is the CUT is idle. Practical testing is worried with ensuring that the practical logic regarding the circuit that is correctly (in other words, ensures an adder circuit adds). This proposed BIST RS ENCODER is especially designed for Xilinx 4000 and Spartan Series FPGAs [19, 20, 21]. Built-In Self-Test (BIST) designs that most of this program logic that is mappable interconnect resources in the core of Xilinx 4000E, 4000XL/XLA and Spartan Series Field Programmable Gate Arrays (FPGAs).

The proposed architecture that is implemented is of overall architecture of most Xilinx 4000 and Spartan Series FPGAs [22, 23, 24]. FPGAs is identical in that a 2-dimensional array of PLBs is interconnected by a routing system that is programmable. Nevertheless, there are differences between the three main families we targeted (4000E, 4000XL/XLA, and Spartan) in terms associated with programmable logic that is interlink resources [25, 26, 27]. The main advantage of us Xilinx that is ing x and Spartan PLB architectures having the less quantity of flip-flops and Look-Up Tables (LUT). The s which are after are used in this paper. The proposed architecture works in 2 cases whenever Test signal is low When Test signal is high whenever TEST signal is minimal (TEST=0) the normal RS that is Encoding activated. Theiple that is mult (MUX) takes the input also it offers to your RS encoder. In this paper the RS encoder is RS (204,188) is used [28, 29]. RS Encoder takes the input as multiple xer signal and it age nodes the signal i. that is e RS encoded output whenever TEST signal is high (TEST =1) the BIST triggered plus it does not takes the input and CUT is triggered whenever BIST activated the controller sends a signal to Test Pattern Generation (TPG).

III. RESULTS ANALYSIS

Figure 5: Simulation waveform for RS encoder module

Fig.5 shows the simulation results obtained for the BIST normal mode that is(TEST=0). in this normal mode the input is (7:0). the MUX takes the input plus it offers towards the RS Encoder. the RS Encoder encodes the input and also the production is provided by it as (7:0).

Figure 6: Simulation results for implementation of overall system design module that is ign

Fig.6 shows the activated BIST done. Meaning the Test signal is high (TEST=1) and allow is high. When test help and test is high the controller r s stops the BIST activated signal to your s ys tem. This could be the circuit under test mode that is CUT). in this mode CUT is RS Encoder. Whenever BIST is triggered the TPG creates

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the signals. The age signal re inputs to your CUT. The TPG created signals are various signals (9:0).MUX offers the multiplexed signal and it is input towards the CUT/RS Encoder).the input is (9:0) and MUX gives to your CUT is (1:0).The CUT gives the production as (7:0).This is the normal representation for the b its regarding the polymedia production that is 1 of CUT. The compactor converts the production that is polynomial to normal representation of bits [30, 31]. This really is fond of the controller to obtain the mistakes out such method is CRC. SIGNATURE REGIST ER module having the Signature gold is understood to be the mean of this coded information is called the signature gold [33, 34, 35]. The signature gold is 00000001. The co mparator inputs are co mpactor output (0000000010) and its regis that is signature value (00000001). The concept regarding the co mparator is co mpares the two inputs a nd provides the s which can be appropriate. The 2 values are same in this case age s the comparator provides the BIST DONE signal [36, 37, 38].

Fig 6 shows theBis t t that is triggered fail. The aforementioned procedure is same also and by changing the s signature silver value to s the way the Bis t fail operation. [39, 40]. The age comparator co mpares the signatureregister co and value impactor also it provides the BIST fail signal because age the two inputs are very different [41].

IV. CONCLUSIONS

Theis task discounts with concurrent mistake detection in RS encoders. We could attain the erroneous information at encoder s ide and finding the equipment functionality with BIST method by us ing this strategy. The error correcting capability of 8 Symbols (64 b its ). The rule us es a s clock that is implemented and ess that is poss. 64 bits error correcting capability. The quantity of mistakes corrected, s symbol s codeword and ize size are programmable. The rule also supports input that is constant s tream without space between rule obstructs. We are able to inform there are not any mistakes into the RS Encoder by us ing this system. The propos ed mentation that is inple of RS ENCODER overall architecture of a ILXin x 4000 and Spartan s sries FP GAs. FPGAs are identical for the reason that a 2- dimers array that is inal of is interconnected by a programmable routing network. But, there are differences between the three ma infamilies we targeted (4000E, 4000XL/XLA, and Spartan) in terms of the programmable logic that is le inter link res ources. The benefit of us ILXin that is in x and Spartan PLB arch tinctureshaving the less quantity of flip -flops and Look-Up Tables (LUT )

REFERENCES


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