Enhanced Scan Segmentation for Low Power DFT

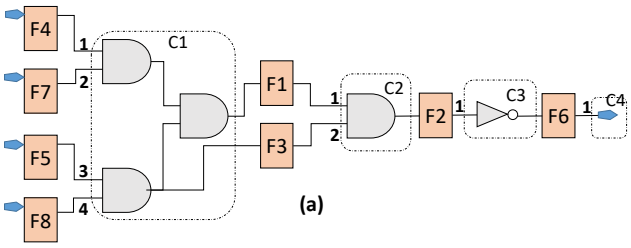
Shalini Pathak, Mausumi Pohit, Anuj Grover

Abstract*— Excessive test power dissipation during scan testing of an SOC may cause reliability and yield concerns for the circuit under test (CUT). We propose an enhanced scan segmentation method using logic cluster controllability (LoCCo) technique for scan chain stitching to reduce test power efficiently. After LoCCo based scan stitching, since the trailing edge of scan chains contain very less switching transitions, we optimize the number of segments needed. This enables segmentation hardware reduction and still achieve lower power scan test compared to conventional method. Test cases prepared from ITC'99 standard circuits and industrial designs in 40nm CMOS and 28FDSOI technology were used for comparison. LoCCo based scan segmentation gave a shift power reduction of up-to 21.7% over conventional scan segmentation. Up-to 8.6%, shift power gain was observed even with 25% reduced segmentation when enhanced scan segmentation technique is used.

Index Terms: Low power DFT, scan stitching, scan segmentation, care bits, DFT.

I. INTRODUCTION

The ever-increasing complexity and size of VLSI designs makes the testing of these circuits a daunting task. Power consumption during test is becoming a major bottleneck in achieving lower test application time as it is practically not possible to test the whole design in parallel due to very high current demands. The switching activity in device test mode is far higher than the functional mode which leads to excessive heat dissipation, voltage IR drops and increased die temperatures. This can deteriorate the device performance during testing leading to erroneous results and hence yield loss. It may also cause instant circuit damage and reduced reliability [1]. A review of various test power reduction techniques has been done in [2]. They can be broadly categorized into software based and hardware based techniques. Hardware-based methods gain on test power by changing the design or scan architecture [3]-[11]. Scan segmentation, multiple scan clocking scheme, extra logic to keep the combinational logic at the outputs of flip flops static, non-overlapping clock usage to control odd and even flip flops of the scan chains with clock gating are few of the existing hardware based methods. These techniques have limitations of increasing circuit area and degrading circuit performance. The software-based methods achieve low power by either generating low power patterns using efficient ATPG algorithms or by reordering the generated test sets. They do not require any hardware overhead and can be easily implemented through algorithms [12]-[15]. X-filling technique is one such commonly used algorithm that reduces the CUT's (circuit under test) power dissipation due to switching transitions by intelligently controlling the filling of don't care bits (X-bits) in test cubes such that the overall switching transitions in consecutive test bits are reduced. Another software based method [16] talks about a novel logic cluster controllability (LoCCo) based scan stitching technique where scan cells are stitched in a way that the flip flops requiring more number of test bit combinations or care bits to test the combinational logic, are positioned towards the beginning of scan chains. This means the end of chains mostly contains don't care or X-bits. These X-bits can be efficiently filled by any X-fill algorithm to generate low power patterns with reduced weighted transition count (WTC). In this paper, we propose an enhanced scan segmentation method using LoCCo. Scan segmentation splits a single long scan chain into segments of smaller chains and during scan shifting each segment is tested one at a time [10]. This reduces the overall WTC of scan chains. LoCCo assisted scan segmentation gives more reduction in shift power as compared to the case where segmentation is applied on conventional scan stitched design because LoCCo chains are already optimized for switching transitions. The presence of don't care bits towards the end makes it possible to segment only the heavy switching portions present in the beginning of chains. This reduces the hardware and routing overhead associated with scan segmentation. Experiments done on ITC'99 circuits and two industrial designs showed an average shift power gain of up-to 21.7% with scan segmentation using LoCCo compared to conventional scan segmentation. We decreased LoCCo segments by 25% and still achieved a power reduction of up-to 8.6% over conventional scan segmentation. Rest of the paper is organized as follows. Section II explains the theoretical background and related work for the proposed technique. Section III discusses the enhanced scan segmentation method. Section IV presents the



Cluster	Controllability
C1	4
C2	2
C3	1
C4	1

(b)

Fig. 1(a) Example topology for showing Logic Clusters and Controllability concept; (b) Controllability numbers for each cluster identified [15]

experimental results on various circuits, and we conclude the paper in section V.

II. BACKGROUND AND RELATED WORK

A. *LoCCo based scan stitching*

LoCCo stitches the scan chains based on cluster identification and their controllability [15]. Fig. 1 shows a simple topology to illustrate the cluster and controllability concept used. Cluster is identified as a group of logic gates bordered by scan flip-flops or ports. The number of input-side scan flip-flops driving the cluster is said to be its controllability. A cluster with higher controllability would need more test combinations for fault testing compared to a cluster with lower controllability number. During ATPG, the test cube generated would have more care bits for testing of higher controllability cluster while the clusters of lower controllability would have don't care bits in most of the patterns. LoCCo sorts the synthesized netlist based on

$$WTM_i = \sum_{j=1}^{N-1}(S_{i,j} \oplus S_{i,j+1}) \text{ X } j \qquad (1)$$

controllability, placing higher controllability clusters to the beginning of chains ensuring care bits concentrate towards the beginning of test vectors. Weighted Transition Metric (WTM) proposed in [16] can be used to estimate the shift-in power caused by transitions in a test vector. where N is the number of scan cells in the scan chain, $S_{i,j}$ represents the logic value of the j^{th} scan cell in i^{th} test vector. As LoCCo sorts the clusters based on controllability, and brings bits with higher care bit probability towards the beginning of chains, it enables lowering of WTM by reducing the transition location number j in each test vector as shown in Fig. 2. A low power X-fill technique can be used to optimally fill the don't care bits. Though the method is generic enough, in our experiments we use MT-filling method to reduce number of shift-in transitions

B. *Scan Segmentation*

Scan segmentation or partitioning is a technique where scan chain is divided into a number of segments and only a single

SI →	F1	F2	F3	F4	F5	F6	F7	F8	→ SO Transitions
P1	1	1	1	1	1	X1	1	1	0
P2	0	0	1	0	1	X1	1	1	9
P3	1	X0	0	1	1	X0	0	1	16
P4	X1	X1	X1	1	0	X1	1	1	9
P5	X1	X1	X1	1	1	X1	1	0	7
								Total Transitions	41

Fig. 2(a) Shift-in transitions for circuit of Fig. 1(a) with scan alphabetically stitched scan chains as done by industrial tools [15]

SI →	F4	F7	F5	F8	F1	F3	F2	F6	→ SO Transitions
P1	1	1	1	1	1	1	1	X1	0
P2	0	1	1	1	0	1	0	X0	16
P3	1	0	1	1	1	0	X0	X0	8
P4	1	1	0	1	X1	X1	X1	X1	5
P5	1	1	1	0	X0	X0	X0	X0	3
								Total Transitions	32

Fig. 2(b) Shift-in transitions for circuit of Fig. 1(a), when scan cells are stitched based on LoCCo achieving a gain of 22%

segment is active while pattern shifting [10]. Other segments are kept in hold mode to retain the scan test data. Fig. 3 shows the segmented scan chain structure. Let us consider that the scan chains are segmented into s number of segments. Each segment is controlled through its $MODE_j$ signal, such that whenever $MODE_j$=1 for a particular segment, that segment gets the test data through *scan_in* port while the other segments are bypassed. The response data from the previous test vector for the selected segment is also simultaneously shifted out through *scan_out* port. The process continues until all the segments are sequentially selected for shifting. Scan segmentation technique is thus an effective way to reduce shift power by decreasing the weighted transitions of scan chains, which is proportional to the number of segments per chain. The generation of $MODE_j$ control signals during scan operation is done by using a s-bit wide shift register which successively shifts 1's from right to left to select different segments. As the test vector is applied to same scan cells' positions as in the original unsegmented scan chain, the method ensures that the test coverage is not impacted. The test application time is also not increased with respect to the original chain

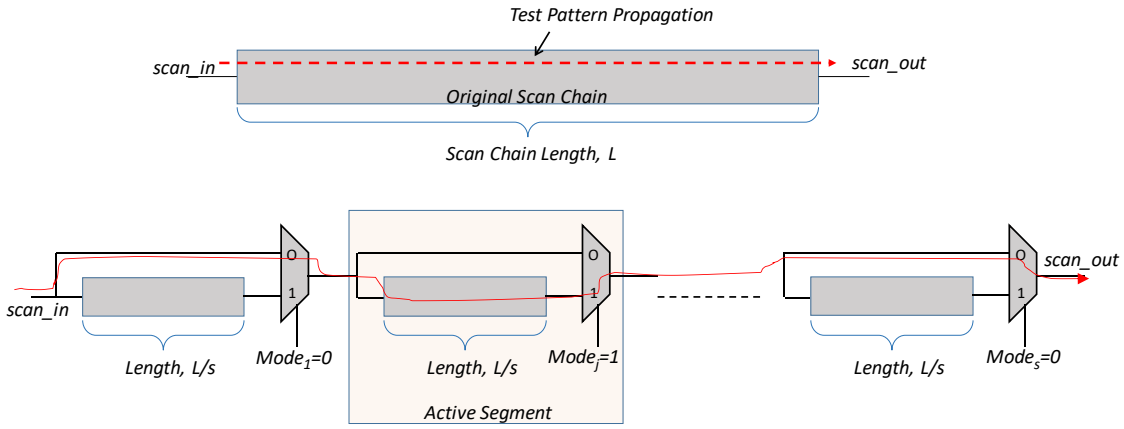


Fig. 3. Scan chain segmentation [10]

III. ENHANCED SCAN SEGMENTATION USING LOCCO

Scan segmentation though is a useful method for shift power reduction, but may suffer from some limitations in large industrial designs due to extra hardware needed to segment the chains and routing overhead to route $MODE_j$ signals to all the segments. The proposed enhanced scan segmentation method utilizes LoCCo stitched scan chains for segmentation to achieve further power reduction and reduce hardware cost of segmentation. LoCCo based scan chains are already optimized for getting low shift power numbers due to its ability to club most of the care bits towards the beginning of scan chains. The high switching transitions required to fill these care bits do not have to traverse through the whole length of chains, thereby giving overall less toggling during shifting. Also the trailing end of chains mostly contain X's which are effectively filled with appropriate values for getting less transitions. Segments can be targeted only in the leading part of the chains to control shift power while later portion of the scan chains which mostly contain don't care bits after applying LoCCo, can be left unsegmented to save the hardware cost.

IV. EXPERIMENTAL RESULTS

For evaluating the performance of LoCCo assisted scan segmentation method, we conducted the experiments on standard ITC'99 benchmark circuits. We combined circuits B1 to B14 to make a single circuit B1_to_B14 to make it large enough for meaningful segmentation and emulate the real SOC behavior. Two industrial IPs were also used for experiments. One is the Built in Self-Test (BIST) block of an Analog-to-Digital converter with 4506 flip-flops synthesized in 40nm technology. The second is a Set-Top Box security features IP with 9450 flip-flops synthesized in 28FDSOI technology. Synopsys Design Compiler was used for design synthesis and conventional scan chains were stitched using DFT compiler. Synopsys Tetramax's MT-fill algorithm was used for generating low power test patterns. To illustrate the usefulness of proposed scan segmentation method we compared the average shift power for conventional scan and LoCCo based scan stitching. The chains were divided in 1 ,4 and 8 segments in different experiments. Table I summarizes the results obtained. On the three circuits experimented, LoCCo based scan-segmentation gave shift power reduction of up-to 21.7% compared to the conventionally stitched and

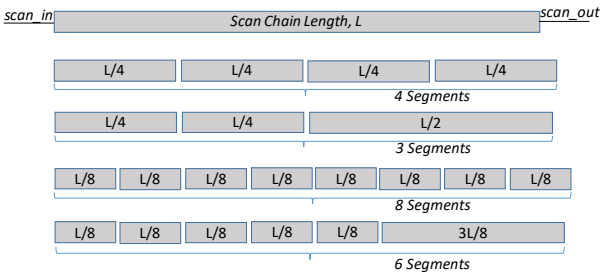


Fig. 4. Scan segments done for the experimental results shown in Table I and II

segmented chains. In order to exploit the fact that LoCCo based scan chains are already optimized for WTM, we did another trial by reducing the number of segments per chain. As the high controllability bits are concentrated towards the leading edge of chain it is better to keep the segment length same as before to minimize the WTM while the trailing edge scan segments were combined. In case of 4 segment experiment, this was done by combining the last two segments, creating 3 segments in total. While for the 8 segment experiment the last three segments were combined resulting in creation of 6 segments, Fig. 4. As LoCCo concentrates bits with lower controllability towards the end of chains, the last segment in the experiment would mostly contain bits with low care bit probability. The shift power in the longer last segment is thus relatively low and does not contribute much in the overall power. The experiments show a shift power gain of up-to 8.6% with reduced segment configuration. Table II shows the results for all three test IPs The method provides a 25% reduction in hardware cost by saving MUXes for segmentation and reduced routing of control signals. [8] proposes a method to further reduce power reduction after scan segmentation. It uses ant colony optimization (ACO)

Table I. Results of Proposed Enhanced Scan Segmentation using LoCCo

Circuit Under Test	#Scan Cells	Conventional Scan Stitching		LoCCo based Scan Stitching		
		# Scan Segments	Average Shift Power	# Scan Segments	Average Shift Power	% Power Gain
ITC'99 B1_to_B14	679	1	71.42	1	60.13	15.8
		4	17.21	4	13.83	19.7
		8	7.57	8	6.31	16.6
BIST IP	4506	1	604.96	1	476.23	21.3
		4	148.22	4	119.06	19.7
		8	65.94	8	53.34	19.1
Security IP	9450	1	1301.34	1	1019.45	21.7
		4	312.32	4	244.67	21.7
		8	141.85	8	112.14	20.9

algorithm to reorder the scan cells within scan segments to minimize transitions. ACO is an iterative approach to solve NP-hard problems. The technique is time consuming and computationally intensive with limitations on how big a circuit it can handle for finding optimum solution. [8] achieved an average power reduction of 3.56% for the circuits experimented. While LoCCo scan chain sorting is quite fast and as the results in table I show, with enhanced scan segmentation, we could achieve an average power reduction of 19.6% for the circuits experimented.

V. CONCLUSIONS

We present an enhanced scan segmentation methodology using LoCCo for low power DFT. Results on ITC'99 standard based circuit and two industrial designs show shift power reduction of up-to 21.7% when scan segmentation was done on LoCCo based scan chains. A shift power reduction of up-to 8.6% was still achieved when number of segments in LoCCo scan chains were reduced by 25%. The proposed method enables a 25% reduction in hardware cost of segmentation with still better shift power saving.

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AUTHORS PROFILE

Shalini Pathak received her M.Sc. Physics in 2000 from IIT Delhi and B.Sc. Physics (Hons.) in 1998 from Delhi University. She started her professional career as FPGA circuit designer at STMicroelectronics, NOIDA in 2000. She is presently working in with Automotive and Discrete Group as Sr. Staff Engineer. Her current research interests include Testability and Test Methods, Low Power DFT, BIST, Low pin count testability and Analog testability.

Dr. Anuj Grover was awarded the Ph.D. from IIT Delhi (2015), MS (ECS) from UCSD (2003) and B.Tech. (EE) from IIT Delhi (2000). He joined STMicroelectronics, India in 2000 in memory design team and is presently working as Assistant Professor with Indraprastha Institute of Information and Technology, Delhi. His research interests include memory design, design redundancy, reliability and testability. He has published more than 20 papers and has 5 patents.

Dr. Mausumi Pohit was awarded the Ph.D. degree in 1996 from Calcutta University. She worked for target recognition based on hybrid optical correlator in the Physics Department of IIT (Delhi) as a project scientist. She is currently a Professor at the Applied Physics Department, Gautam Buddha University, Greater Noida researching on machine vision, digital image correlation and particle swarm optimization.