Design of A Fault Tolerant Razor Flip Flop Sklansky Adder for Delay Reduction in FIR Filter

A.V.S.S. Varma, Kasiprasad Mannapalli

ABSTRACT: ***Basically, to reduce the failure rate in the system, we need to introduce the fault tolerant system. Because of multiple faults occurred in the system, the system will increase the area. To employ the adder architecture, different algorithms are used in digital signal processing. By introducing the fault tolerant system, the reliability of the proposed system will increase. So in this paper we introduced the design of fault tolerant razor flip flop using SKLANSKY adder for delay reduction in FIR filter. The razor flip flop will increase the energy efficiency of proposed system. This flip flop will store the information by latching the circuit. The SKLANSKY adder is the part of arithmetic logic unit. In proposed system, all bits are summed and followed to the fault tolerance system,. This fault tolerance system will detect the error and give efficient output. Hence compared to existed system, the proposed system gives high performance and accuracy in terms of delay.***

KEY WORDS: ***Fault tolerant, sklansky adder, ripple carry adder, VLSI.***

I. INTRODUCTION

The fields like mobile communication and DSP increased quick growth to form complex frameworks into a solitary chip for example system on-Chip (SoC). It is discovered that this single chip framework has great execution, diminished size, and less power utilization than ordinary plan procedure [1]. Here finite impulse response is used for faster operations. Basically, finite impulse response is nothing but a filter where the impulse response remains fine duration. In signal processing, a finite impulse response (FIR) is used. In the same way it settles zero at finite time. This FIR filter is mainly used in digital signal processing applications. Basically, FIR filter is a signal conditioner; it allows the AC components and blocks the DC components. The example of FIR filter is phone line. In the FIR filter all signal frequencies are delayed in the same amount of time. For finite input it all the signals in filter remains stable.

The designing of FIR filter is based on the approximation of ideal filter. By increasing the order of filter, the FIR filter produces perfect characteristics. By using the specifications of FIR filter, the design process starts its process. To implement FIR filter, digital frequency response is used. To get output from FIR filter, adders, multipliers and delay are created in the system design. Here the FIR filter totally, depends on the three types of frequencies; they are stop band, pass band and transition band. Many of researchers are working in different digital signal processing research areas such as speech processing, Image processing, video processing etc. As many people are using handheld devices phones which can process the above said signals and these signals will improve the efficiency as well as the speed in proposed architecture.

Speech processing system is a procedure of naturally perceiving who is talking based on the individual data incorporated into discourse waves. Similarly it is favored that the confirmation strategy in business exchanges or remote individual ID forms did by phone to give security. Speech processing system speaks to a precision and proficient method for confirming an individual's character by breaking down his or her voice. Voice innovation offers large amounts of certainty and insurance. Numerous associations like Banks, establishments, ventures and so on are currently using this technology for providing greater security to their vast databases. Here,it requires efficient and fast DSP systems.

Improvement of the VLSI (Very Large scale integration) has contributed immensely in utilization of signal processing calculations and besides a phenomenal impact in updating the execution of sign handling gadgets [6-10]. Extensive number of mechanical fields has progressed by using VLSI, one of the domains that have experienced an improvement in the earlier years, with the utilization of many signal processing tools. The most normal features are, bringing direction in meantime while interpreting or executing a MAC movement; where effects of vectors are incorporated, for instance, Fast Fourier Transform and structure of automated channels. We make utilization of structure relationship for immaculate VLSI design to create banner planning structure. Vital feature has been given in the recent years being made of various structure models and styles for various testing paces and applications. The execution of system fundamentally depends upon, structure (masterminding) and its parts and besides on the data way containing the data storage functional units [2]. The relationship of helpful units speaks direct to suit the cost and speed restrictions of the general structure. The two guideline commitments of plan combination are to assign the hardware resources and research the distinctive parallel executions. Audio sign in the steady circumstance are normally ruined by various sorts of twisting and basement of system [3].

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II. LITERATURE SURVEY

Today, the fault-tolerant system is exceptional in essential applications, where rapid human movement is ridiculous. The spatial application, the perception of obstruction, the structure of restorative supervision and other safety-related organizations are the situation of these fundamental applications. In the applications of general systems, complexity of circuits is reduced. Forward movement can reduce the range of melted circuits. Because of this transient problems are obtained. The fundamental reason for the proximity of transitory deficiencies in the organized circuit is the electromagnetic clamor, the vast pillars, the interference and confusion of the power supply. Furthermore, the development scale is also the possibility of the proximity of a constant problem [4]. The conservationist structure is useful for reducing concussion, as it will produce the possibility of disappointment of the gears in the propulsive processor. It is surprisingly difficult to perceive these problems in the middle of disconnected tests. Therefore, these problems are the challenges for examiners working in the field of online deficiency tests and recognizable modification procedures.

The main intent of Full adder is to perform the addition operation. Along with addition operation it also performs address check and division operation. Hence these type of full adders are used in the focal point of any system. In many circuits for effective execution full adders are used. The structure of full adder depends on the binary extension system. In this transistor fault is used to check the faults in the system by using multiplier and arithmetic logic units. In this way to structure an error tolerant full adder, a lesser region is incorporated by remarkable significance. Different scientists have been worn out various sorts of weakness tolerant full adders.

The development code of the accumulation number is used to organize the purchaser of complete primary self-control. This adder can perceive the unique defect without delay for a moment. In any case, the limits of the mathematical development codes are irregular circuits and their irregularity obtain from self-control memory structures. After this, countless verification approaches have used address replay to correct the defect, but will extend the deferral of the upward distribution, so to speak. In any case, poor recovery is the ultimate domain of creative abilities in this approach if the problems are long lasting.

The self-control of the complete adder can perceive the insufficiencies with the indication of its unequivocal zone. In this arrangement, Sklansky is used, while it is essential in the plan and in the work. Here the main disadvantage of ripple carry adder is, it takes more time to operate the system. Hence in this case Sklansky adder is used. By using this adder the operation of system performs very fast and it takes less time to perform the operations. Among all adders, the sklansky adder gives effective performance. [5].

Throughout the years, different works from the writing have exhibited various models and VLSI-based usage answers for the Sobel administrator. In any case, in regards to ASIC arrangements, a few works have investigated a quickening agent technique, for example, in which proposes a backend plan for the Sobel administrator. In spite of the fact that the referenced works present various answers for the usage of Sobel administrator, none of them utilize rough adders administrators for the execution of the part. Some of them have lower zone contrasted with other standard circuits however during the difference in state in information flags, the voltage drop is verifiable. In the mean time to assess these circuits upsizing the transistors are required bringing about an expanded power utilization. In any case, these circuits additionally have some zone overhead and don't work appropriately in ultra profound submicron advances.

Ripple Carry Adder is a fundamental adder circuit which contains singular full adder cells and the carry created upon expansion is engendered between the separate adder cells. The calculation of result happens simply after the carry from the past stage to introduce organize. Because of these proliferation delays, the deferral will undoubtedly happen which is a noteworthy burden. Here the number of quantity of bits obtained in the system will progress the ripple carry adder. Generally, ripple carry adder consists of two numbers A and B. Depend upon these two numbers the entire operation is performed. Here carry input is also available in ripple carry adder. The architecture of the RCA is shown in below Fig 1.

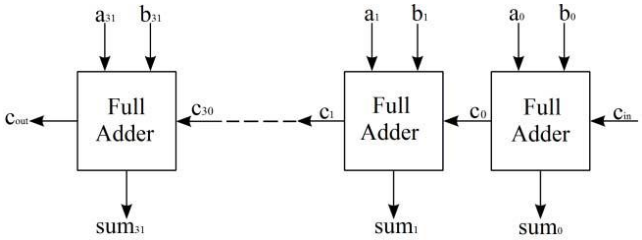

Fig. 1. BLOCK DIAGRAM OF RIPPLE CARRY ADDER

Basically, ripple carry adder is obtained from the general purpose processors and DSP processors. Repetitive additions are performed by using multiplier operand. But By using propagation, the quality, Delay, and area is measured. In ripple carry adder first the carry propagation is overlapped and next addition operation is performed. In spite of the fact that the RCA is made out of a basic structure, which empowers simple execution and it presents poor execution, in light of the fact that the convey is proliferated into every expansion square.

In this the each carry bit is undulated into the following stage. The delay of reverse converters will bind the growth of logarithm in Parallel prefix adder. Basically, in RCA large number of adders will be used. The bit length of this adder is very large. To perform the first part of addition in the system, a desired structure with particular operands is used. Here first full adder is replaced by half adder as shown in fig 2. High power consumption is obtained due to the recursive effect. Recursive effect is obtained while generating and propagating the signals at prefix level.

High fan out characteristic also obtained in the system. So to overcome the problem of delay occurred in the system, a new system is proposed. However, this problem is eliminated by using additional prefix level which is

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discussed in below section. In contrast to the proposed system, it is able to perform a conditional increment depending upon the control signals as shown in Fig 2.

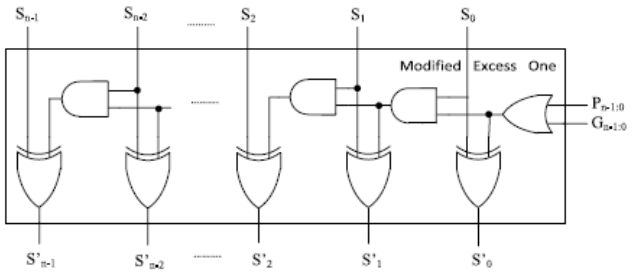

Fig. 2. STRUCTURE OF RIPPLE CARRY ADDER

For power-effective Gaussian and Gradient (Sobel) channels, Canny edge locator calculation is proposed. The work in proposes a surmised engineering for Sobel channel utilizing Copy and the estimated adders. The work likewise recommends a pursuit heuristic to bunch the adders in the design that have comparable sizes in the information operands. For each gathering of adders, k least noteworthy bits is resolved. This is done to mitigate the expansion in the blunder for gathering of adders whose whole outcome may have lower size and to expand estimate for gatherings of adders where the extents are relied upon to be higher.

III. RAZOR FLIP FLOP SKLANSKY ADDER

Addition is a central task for any advanced framework, computerized flag handling or control framework. A quick and precise activity of a computerized framework is incredibly affected by the execution of the inhabitant adders. The execution of an advanced circuit square is checked by dissecting its capacity dissemination, format zone and its working pace. Novel proposed adder is helpful in this day and age of innovation in light of its usage in Very Large Scale Integration (VLSI) chips. Sklansky Adder can be generated by using simple algorithm with minimum depth.

Basically, bi stable multivibrator is known as flip flop. Because flip consists of two logics logic 0 and logic 1. It stores the information in strategic format. Here the flip will change the state of circuit according to the given input or logic. The signs associated with at any rate one control inputs and will have two or three yields. A Razor flip-flop is acquainted that with test the pipeline arrange values with a quick clock and time-getting deferred clock. The key though to check supply voltage by tuning the bit rate accordingly taking out the requirement for voltage edges and misusing the information reliance of circuit delay.

The below fig 3. shows the block diagram of novel proposed adder. In this we use mainly razor flip flop, fault tolerant elements. Novel proposed adder consists of three stages. They are pre-processing stage, prefix generation stage and post processing stage. In pre-processing stage, the generate and propagate signals are carried out. In prefix generation stage prefix graphs are used to define the tree structure. At last in post processing stage, sum and carry is calculated.

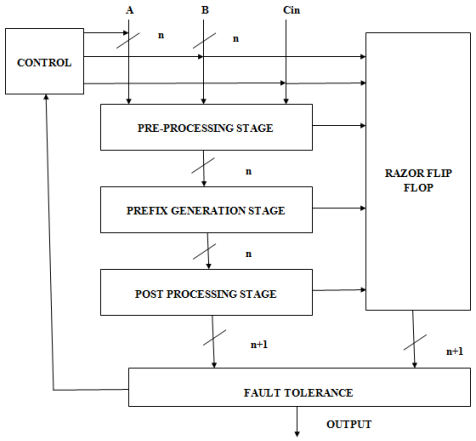

FIG. 3: BLOCK DIAGRAM OF NOVEL PROPOSED ADDER

In the phase of prefix calculation, the conveys are gathered by the adders setup with respect to bring down cost, power, and deferral. As per the adders arrangement, the prefix calculation bunches the two qualities straightforwardly from the contribution with qualities that were registered in the pre-handling stage. The expanded postponement is acquired by the design that has the most elevated basic way like the adders which process multiple data sources. In the post-handling stage, the adders values that form the yield are assembled. They are come to through the last snake setup that is organized by an answer that amends the issue of the right convey spread for each info bit. The last aggregate arrangement is organized by a XOR work that catches the qualities originating from the last stage of carry.

The task of the proposed novel adder relies upon the control signals given independent from anyone else checking full adder. For the situation that the control banner is 0, it shows that there is no shortcoming in the aggregate yield. The full adder cell is obtained from selected inputs which are given. Now if the logic is 1 then the full adder will shows that there is an error in the system. but if the logic shows zero, then the system will shows that there are no faults and the system is error free. Hence the three stages perform the operation in effective way by following the fault tolerance system.

First novel proposed adder architecture is based on the adder architecture is shown in fig 4. In this architecture grey cell and black cell operation is performed to determine the total sum. The parallel-adder computes the entire process and composed of n-bit adder for LSB bits. Carry output obtained at the end of gate.

Here the time should be minimized in computation process. Because of this the speed of the operation is increased. By using recursive equation each bit position is derived. In the same way using a single row of prefix operator the addition operation of carry bit is done in parallel. Here the carry increment stage is utilized for addition operation. Because of this high efficiency is obtained. From this we can observe that carry increment stage is not necessary in this system

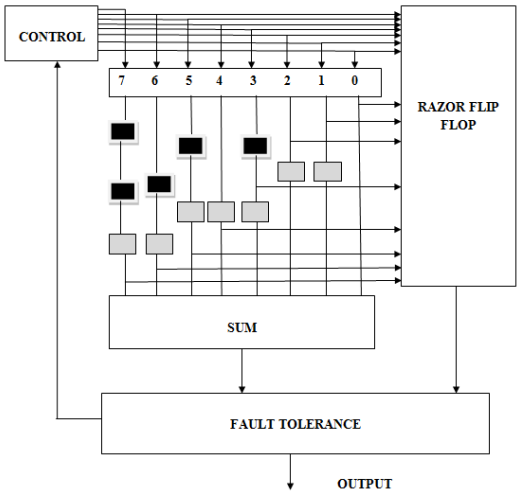

Fig. 4: ARCHITECTURE OF NOVEL PROPOSED ADDER

Based on the inputs given the outcome of operation is performed. As we know that the proposed novel adder performs and executes the operation in parallel. The obtained output will be segmented into smaller pieces. There are different topologies used in proposed novel adder, but the operator is associative. Based on topology the operation is performed. By using the associative binary operations, the algorithms will be generalized. This generalized algorithm performs certain operations and computed with particular efficiency. Basically there are two procedures followed in the system, they are in first pass the prefix sum as are calculated from the processing unit. And in second pass known prefix values are computed from processing unit to get initial value. So along with that the system performs two read operations and one write operation. Here a methodology is employed to design proposed novel adder.

The experimental result mainly, depends on area, delay, and power consumption. The expense of additional area and remarkable will increase the power consumption. Compared with VLSI implementations, the novel proposed adders will produce performance differently. The modern FPGAs employ the fast-carry chain process to get faster results. When compared to the results of existed system, the proposed system gives efficient results. At last it reduces the delay and provides more long wires to route. Less delay is taken to implement the proposed adder and also it has less wiring congestion. The adders are implemented in xilinx14.7 design suite.

IV. RESULTS

Table. 1: Comparison graph

S.NO	LOGIC DELAY	ROUTE DELAY	TOTAL DELAY
CLA	20.473	29.21	49.683
RCA	20.952	26.85	47.84
PROPOSED ADDER	10.789	9.46	20.249

The below fig 5. shows the comparison graph of total delay. From this we can observe that the total delay of proposed system is less compared to RCA and CLA adders.

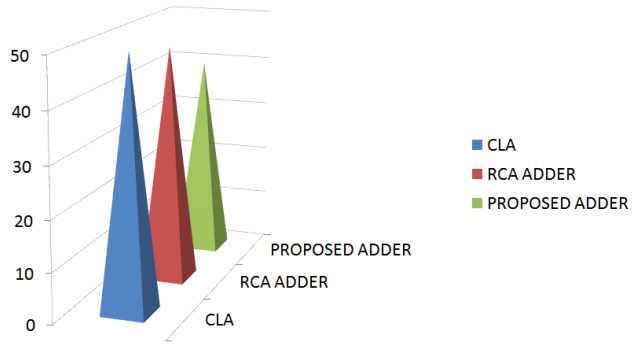

Fig. 5: COMPARISON GRAPH OF TOTAL DELAY

The below fig 6. we can observe the comparison graph of logic delay and route delay. Here the logic delay of proposed system is less than the RCA and CLA adders. In the same way the route delay of proposed adder is less than the RCA and CLA adders. From these results we can observe that the proposed system gives efficient results in terms of delay.

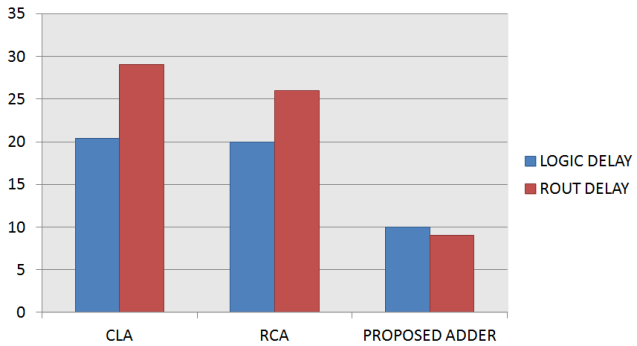

Fig. 6: COMPARISON GRAPH OF LOGIC DELAY AND ROUTE DELAY

V. CONCLUSION

In this paper, we have exhibited flaw tolerant razor flip flop using Sklansky adder structure for delay reduction in FIR filter. This system will increase the robustness by reducing the faults occurred in the system. By using razor flip flop, the proposed system obtained high performance. The framework presents fault tolerant adder configuration accepting deficiency models. For the most part more than one module close to the module influencing some portion of the framework winds up defective. Thus the framework must have the ability to endure various deficiencies. From results we can observe that it produces effective results compared to the existed system.

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