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Fpga Implementation of Active Neighborhood Pattern Sensitive Fault Testing Using Tiling Method

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Abstract*: *Test structure for Active Neighborhood Pattern Sensitive Fault (ANPSF) in memories with high switching speed is modeled in this paper. Algorithm for ANPSF testing is developed using type-1 neighborhood approach. The type-1 neighborhood, also known as tiling method has one victim and four aggressor cells. It is used to identify the ANPSF effect on base cell by the switching of patterns in the corresponding deleted neighborhood cells. The required test pattern can be generated using a Binary counter, Hamiltonian or Gray pattern generator where the two successive values differ in only one binary digit. The BIST architecture allows to incorporate the hardware required by the user to select the victim and corresponding aggressor cells to test the complete memory. It helps in application of test pattern for the memory circuit under test on user's choice. The main objective of this model is to develop the architecture for tiling methodology with test pattern generator to detect the transitions in aggressor cells with edge detection technique. The proposed work enables to verify the response of victim cell which may cause a change in value resulting in an active neighborhood pattern sensitive fault scenario. The complete ANPSF model architecture for memory testing is developed using Verilog hardware descriptive language. The process of simulation and synthesis report is validated using Xilinx 14.2 and implemented on Nexys 4 DDR Artix 7 FPGA board.

Keywords*: *Active Neighborhood Pattern Sensitive Fault (ANPSF), Tiling method, Type-1 neighborhood, Binary counter, Hamiltonian, Gray pattern generator, Xilinx ISE 14.2, Nexys 4 DDR Artix 7 FPGA.

I. INTRODUCTION

Memory testing is of key factor to determine the system reliability. Engineers design a built-in self-test approach to achieve it by reducing the test complexity thereby, decreasing the dependency and cost on external test equipment.

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The BIST approach was first followed by the combinational circuits after which it quickly took a turnover with the testing of regular structures like programmable logic arrays, ROM and RAM [3]. As the complexity of memory circuits became more, the fault models should be considered more in number which are associated with it, to obtain a good quality product. The conventional method of testing memories was limited and indeterministic as there were fault models which made a greater impact with the increase in density of memory circuits. The increase in coupling effect gave rise to k-coupling fault with k, notifying the number of cells being coupled.The pattern sensitive fault model is a type of coupling fault. It has one victim cell in the physical neighborhood of several aggressor cells. Type-1 neighborhood has four aggressor cells and one victim cell. Hayes in 1980 has defined and devised a memory model for NPSF. After which Suk and Reddy has proposed a bipartite method for the memory model. They partitioned the complete memory into two segments to cover all possible victim-aggressor combinations which incorporate the issues regarding longer time complexity. In 2002, other efficient March tests were proposed which involved multiple backgrounds [7] but they couldn't support the complete neighborhood pattern sensitive faults. The proposed methodology reduces the overall timing constraint when compared with the conventional approach and the ANPSF architecture is used to specify the faulty pattern in accordance to the deleted neighborhood cells.

This paper is catalogued as follows. Section II illustrates the tiling methodology and fault models with the classification of NPSF model. Section III describes the block diagram, flow chart, RTL and corresponding pseudo code to the design of ANPSF architecture for the memory using type-1 neighborhood by tiling technique with the description of inner blocks in detail. Section IV illustrates the results obtained by the simulation and synthesis tools with the FPGA implementation on Nexys 4 DDR Artix 7 board. Section V gives the conclusion for ANPSF testing**.**

II. FAULT MODELS AND TILING METHODOLOGY

A deviation from the ascertain to the anticipated memory response causes a faulty behavior. An error is a difference between faulty value and the golden value, which causes a failure when the system response is incorrect. The physical difference between an incorrect and a good system is considered to be a fault and it is denoted as R for a read operation.

A sensitizing operating sequence(S) is an operating sequence which results in the variation between the ascertain and the anticipated memory behavior of the system.

To detect the memory cell faults, such as for stuck at 1 we write 0, and read 0 from it and for stuck at 0 we write 1 and read 1 from it. To detect the rise transition fault, we write 0 then write 1 and read 1 from it. For a fall transition fault we write 1 and then write 0 and read 0 from it. The coupling faults has a victim cell and the aggressor cells [1]. To identify the type of coupling fault such as, inversion coupling where the contents of victim cell are inverted if aggressor cells has a transition. Consider, if we have two cells x and y then, write 0 to x while y makes a transition from 0 to 1 read 0 from x. Similarly, write 0 to x and when y makes a transition from 1 to 0 read 0 from x to locate any of the coupling fault in the memory cell under test.

In idempotent coupling the victim cell is bound to a value of zero or one if there is a rise or fall transition in aggressor cells. Consider two cells x and y, when y makes a transition from 0 to 1 and value of x is 0 then write a 1 into x and read 1 from x, similarly when the content of x is 1 write a 0 into x and read 0 from it which is a vice-versa for a 1 to 0 transition in y.

In state coupling fault, [2] when the coupling cell is in certain stipulation, the coupled cell is bound to a value. Consider two cells x and y where, content of y is 0 and content of x is 0 then write 1 to x, write 0 to y and read 1 from x. In case 2 when content of y is 0 and content of x is 1 then write 0 to x, write 0 to y and read 0 from x. Similarly, when content of y is 1 and content of x is 0 then write 1 to x, write 1 to y and read 1 from x. In case 4 when content of y is 1 and content of x is 1 then write 0 to x, write 1 to y and read 0 from x.

A. Classification of NPSF

If the number of cells involved are more than one it results in multi cell fault. The unrealistic nature of considering all possible patterns of the elementary storage unit can be eliminated with a simplified model called neighborhood pattern sensitive fault. Depending on the cipher of aggressor cells NPSF can be cleft into several types. In our work we consider, the type-1 NPSF with four aggressor cells [5]. Depending on the decorum of fault, the NPSFs are classified into three categories namely:

Passive NPSF:

Due to the perseverance of assured pattern in the aggressor cells, reflect the impossibility of the victim cell to execute a required transition in it causing a passive neighborhood pattern sensitive fault.

Static NPSF:

When the aggressor cells have a specific pattern, the victim cell is forced to a value causing a static neighborhood pattern sensitive fault.

Active NPSF:

Active NPSF occurs when a certain rise or fall changeover in one of the aggressor cells vigor the victim cell to change its state while the other aggressor cells are associated with certain pattern.

B. TILING METHODOLOGY

0	1	2	3	4	0	1	2
2	3	4	0	1	2	3	4
4	0	1	2	3	4	0	1

1	2	3	4	0	1	2	3
3	4	0	1	2	3	4	0
0	1	2	3	4	0	1	2
2	3	4	0	1	2	3	4
4	0	1	2	3	4	0	1

Fig. 1.Tiling Method

The tiling method, ensures that the entire memory is segmented into non-overlapping neighborhoods. Fig.1 depicts the tiling methodology with five-element type-1 neighborhood [4]. Each element has its corresponding neighbors associated with it.When the test pattern is applied to the neighbors of selected base cell notation, they are consequently applied to the neighbors of other base cell in the memory which taper the pattern length and time complexity, when compared with the conventional method of testing.

Table- I: Generation of formal address values using tiling methodology

Case id	Values of (column%5, row%5)				
0	(0,0)	(1,2)	(2,4)	(3,1)	(4,3)
1	(0,3)	(1,0)	(2,2)	(3,4)	(4,1)
2	(0,1)	(1,3)	(2,0)	(3,2)	(4,4)
3	(0,4)	(1,1)	(2,3)	(3,0)	(4,2)
4	(0,2)	(1,4)	(2,1)	(3,3)	(4,0)

III. ANPSF ARCHITECTURE

A. Block Diagram

The Fig.2 depicts the proposed block diagram of ANPSF model. It has a control signal to write/read data into/from memory. Application of row and column address to the tiling methodology segments the memory unit into five test cases as shown in Table I.

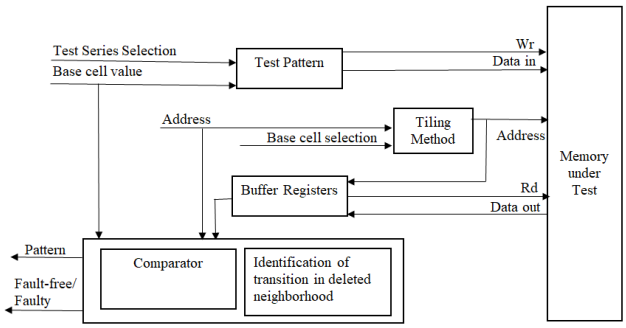

Fig. 2.Block diagram for memory testing

When write control signal is high the test pattern from the selected test series is written into the corresponding aggressor and victim cells which in-turn depends on the base cell selection line. When the status of read control, is active high the value from the memory unit is stored in buffer registers using tiling methodology. The Test Sequence can be generated using one among the test pattern series which are gray, binary or Hamiltonian.

A fault might occur, if there is an inversion of base cell value on identification of any of the transition on the deleted neighborhood cells resulting in a faulty storage unit.

The data read out of comparator block decides whether the memory under test is associated with any of the active neighborhood pattern sensitive faults. An active high indication on fault-free/Faulty determines that the memory unit has a fault associated with it and the pattern from the deleted neighborhood cells is been captured as an output indication.

B. Flow Chart

The Fig.3 depicts the diagrammatical representation of ANPSF pattern detection in presence of a faulty cell.

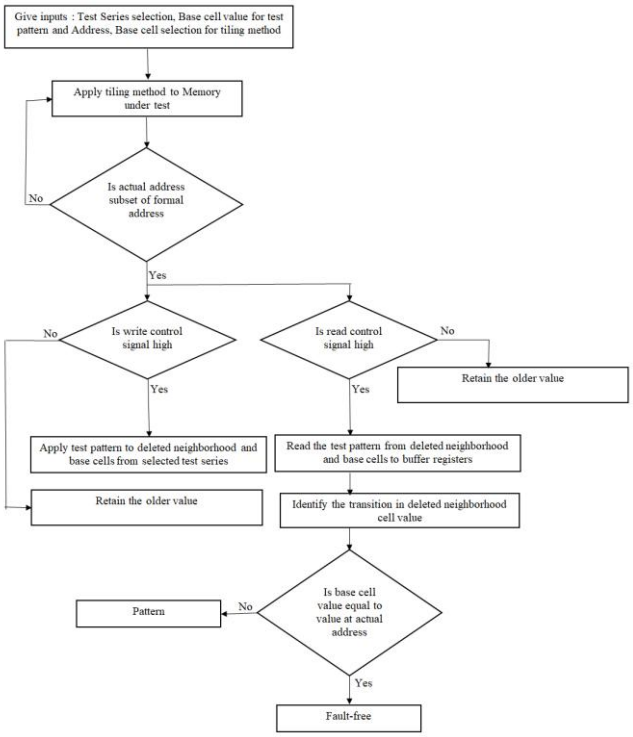

Fig. 3.Flow chart for memory testing

Step I: The inputs for aggressor and victim cells is given through the selected test series and base cell value respectively.

Step II: Application of tiling methodology segments the complete memory elements into five test cases denoted as `0`, `1`, `2`, `3` and `4` as shown in Fig1. The row and column values are provided through the address line. The actual address is now transformed as a subset of formal address as shown in Table I. The aggressor and victim cells are decided depending on the base cell selection value.

Step III: The ANPSF effect of aggressor cells on victim cell can be determined depending on the status of control signals. If write control signal is high the input data is provided to the aggressor and victim cells else the older values of memory are retained. If read control signal is high the output data from the aggressor and victim cells is collected into buffer registers else the older values are retained in the buffers.

Step IV: The transition in aggressor cells is determined using edge detection technique for the deleted neighborhood cell values.

Step V: The base cell value provided as input is compared with the value at actual address of selected base cell. A fault can be detected if a transition in aggressor cells causes a change in value of base cell and the effected pattern is shown as output.

C. Modes of operation

On providing the inputs to the tiling block, it segments the actual address of elementary storage unit and derives a formal address value which may be one among the case id's as specified in Table I. Among the five-case id's, depending on base cell selection criteria the operational mode for the aggressor and victim cells is done in parallel.

The two modes of operation are

i. Write Mode

In write mode the generated test pattern can be applied on selected base cell testing scenario on enabling the write control signal with selection of test series and base cell value.

Fig. 4 depicts the inputs to base cell value. State is a three-bit variable used as a selection pin to the multiplexer. Similarly, the replica of same model is applicable for the selection of deleted neighborhood cells for providing input data to the selected memory cell.

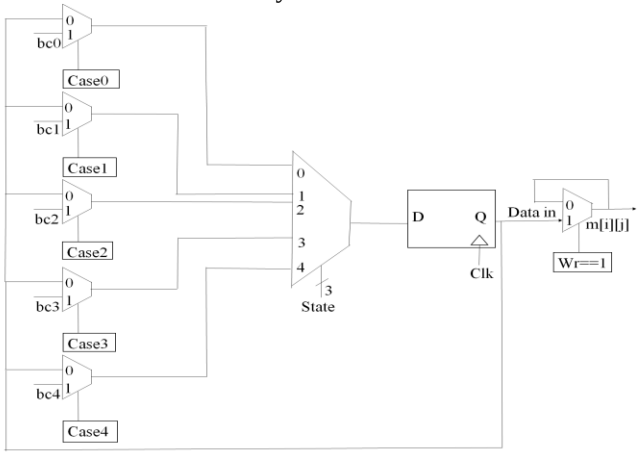

Fig. 4. Input data to selected base cells

In read mode on enabling the read control signal, the output data is read as input to the demultiplexer, depending on the selection line of demultiplexer the output data is placed into corresponding buffer registers. Fig. 5 depicts the behavior of output data being stored into buffer registers.

ii. Read Mode

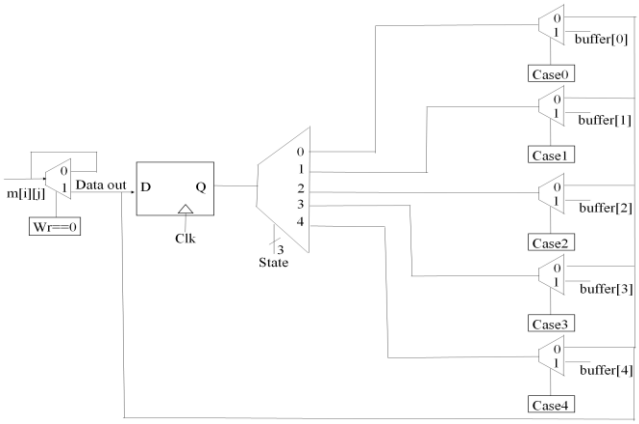

Fig. 5. Output data to buffer registers

In parallel, the process of storing the output data from the deleted neighborhood cells to the east, west, north, south buffers are also performed. The values from the buffer registers are now sent to the edge detector circuitry to specify the transition in deleted neighborhood cells. Fig.6 depicts the occurance of transition in deleted neighborhood cells.

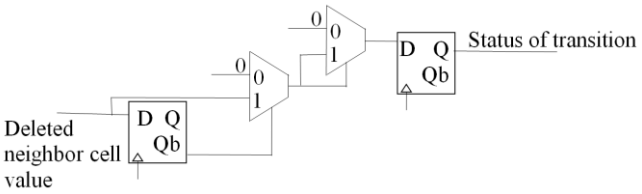

Fig. 6. Neighborhood pattern transition detector

Depending on the status of transition in any of the deleted neighborhood cells causes the comparator to check for the victim cell value in the elementary storage unit resulting in a fault if there is a mismatch in the victim cell value causing a active neighborhood pattern sensitive fault.

D. Pseudo Code

The pseudo code for ANPSF model with case 0 is determined as follows:

```
ANPSF ();
{
Test Sequence ϵ (0,15);
[1:4] dn ϵ values of test series;
m ϵ set of memory elements;
(row, column) ϵ set of actual address;
(i, j) ϵ set of formal address;
(Y1, Y2) ϵ (0→1, 1→0)
t ϵ {0,1,2};
case id ϵ {0,1,2,3,4};
(faulty, faulty read) ϵ {0,1};
for state ϵ selection of base cell criteria;
(deleted neighborhood, base cell) ϵ {N, E, W, S, bc};
    do {
    if(reset) dn←0; m[i][j] ← 0;
    else
    {
    foreach (Test Sequence)
          {
          if (t← 0) dn ← binary series;
          if (t← 1) dn ← gray series;
          if (t← 2) dn ← Hamiltonian series;
          }
    foreach (row, column)
   {
          i←row%5; j←column%5;
    foreach (j, i)
          {
    case (case id)
    {
   0: ((0,0), (1,2), (2,4), (3,1), (4,3)) ϵ (j, i)
   1: if ((0,3), (1,0), (2,2), (3,4), (4,1)) ϵ (j, i)
   2: if ((0,1), (1,3), (2,0), (3,2), (4,4)) ϵ (j, i)
   3: if ((0,4), (1,1), (2,3), (3,0), (4,2)) ϵ (j, i)
   4: if ((0,2), (1,4), (2,1), (3,3), (4,0)) ϵ (j, i)
   }
   for base cell selection if state=0 then,
   for case id=0
    if (wr) m[i][j] ← bc; else if(rd) buffer←m[i][j];
   for case id=1
    if (wr) m[i][j] ← dn[1]; else if(rd) E←m[i][j];
   for case id=2
    if (wr) m[i][j] ← dn[2]; else if(rd) S←m[i][j];
   for case id=3
    if (wr) m[i][j] ← dn[3]; else if(rd) N←m[i][j];
   for case id=4
    if (wr) m[i][j] ← dn[4]; else if(rd) W←m[i][j];
   }
    endcase
       }
       }
foreach element of deleted neighborhood ϵ (Y1, Y2)
if (Y1 or Y2)
    foreach element of selected base cell
    if(buffer==m[i][j])) faulty←0;
    else
    faulty←1;
   pattern ← {E, S, N, W};
}
}
}
```

IV. RESULTS

A. Simulation Results

The simulation results for testing the base cell which satisfies the test case criteria for case 0 with test patterns from binary, gray and Hamiltonian series are shown in Fig.7, Fig.8 and Fig.9 respectively, indicated by the notation B, G and H which displays the output pattern when there is a transition in aggressor cells causing a faulty behavior in victim cell.

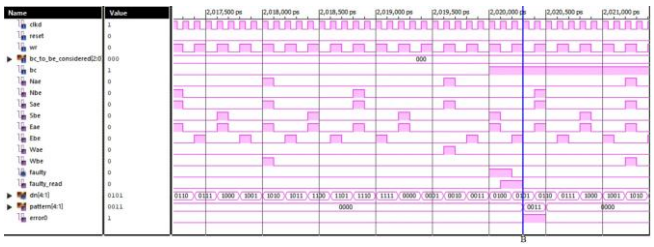

Fig. 7. Simulation result for case 0 with binary test pattern

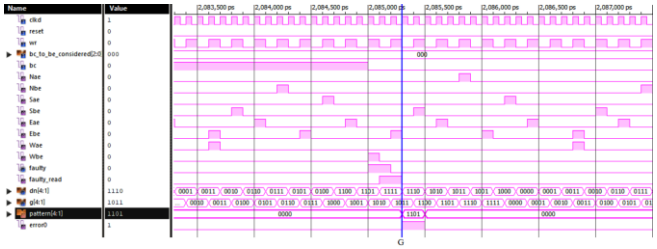

Fig. 8. Simulation result for case 0 with gray test pattern

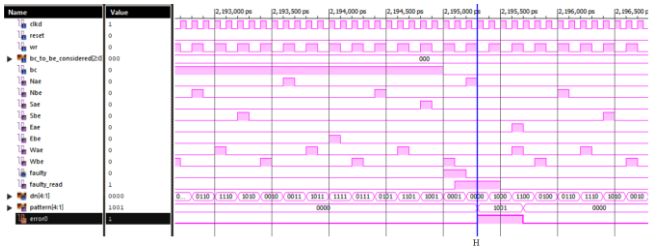

Fig. 9. Simulation result for case0 with hamiltonian test pattern

B. Synthesis Reports

The synthesis of designed logic using Verilog hardware descriptive language is performed using Xilinx ISE tool. It supports to configure the target device with the programming kit facilitating the generated hardware to fit into the available microcells.

Table- II: Device Utilization breviloquent

Slice Logic Usage	Binary Series	Gray Series	Hamiltonian Series
Slice Registers	58	62	58
Flip Flops	58	62	58
Slice LUTs	51	53	50
occupied Slices	22	21	26
LUT Flip Flop pairs	54	56	54
unused Flip Flop	5	5	6
unused LUT	3	3	4
fully used LUT-FF pairs	46	48	44

Table-II describes the different number of registers, flip flops and LUT's used for generating test patterns using binary, gray and Hamiltonian series.

C. FPGA Implementation

The JTAG port is used to transfer the FPGA configuration files in bit file format created from the hardware descriptive language using Xilinx's ISE Web Pack and EDK software.

Nexys 4 DDR Artix 7 FPGA has an internal clock whose frequency is 100MHz [10]. It also has LED outputs and switches which are sixteen in number. The switches are used for giving the inputs and applying test cases. The output LEDs are used to detect the fault scenario. If fault is detected then LED switch will be in ON state otherwise it will be in OFF state.

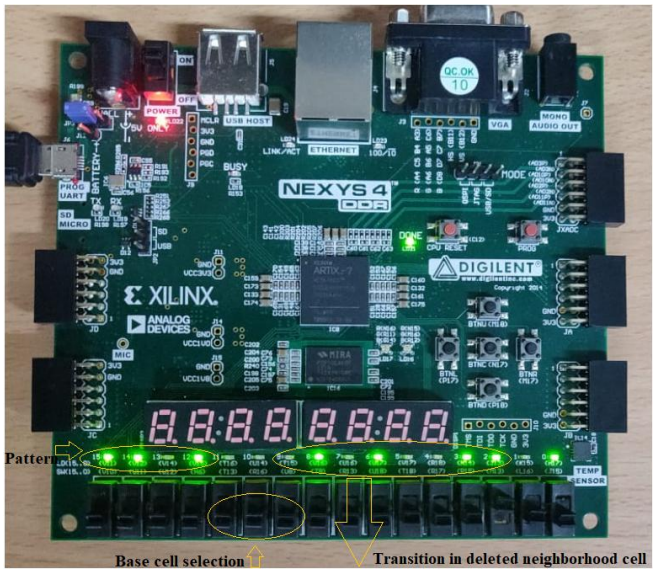

Fig. 10. Fault in memory with active high transition in victim cell for test case 0 on Nexys 4 DDR Artix 7 FPGA

Fig. 11. Fault in memory with active low transition in victim cell for test case 0 on Nexys 4 DDR Artix 7 FPGA

V. CONCLUSION

BIST model for ANPSF in RAM's is synthesized and implemented on Nexys 4 DDR Artix 7 FPGA board using tiling methodology and edge detection technique. In the process of testing, tiling method helps to segregate the aggressor and victim cells. The edge detection technique helps to identify the faulty scenario determining the effect of change in victim cell value due to the corresponding transition in aggressor cells. Thus, dense memory devices which are prone to neighborhood pattern sensitive fault can be tested using this architecture which has reduced time complexity when compared with conventional method of testing.

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