Influence of Self-Heating Effect on I-V Dates of Party Depleted Submicron Silicon-on-Insulator CMOS Transistors at High Ambient Temperatures

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Abstract. ***To solve the problems of high temperature microelectronics the influence of the self heating effect on the I-V dates partially depleted submicron silicon–on-insulator CMOS transistor in the ambient temperature range from 525 K to 650 K is discussed. Approach consists in combination of experimental data and of computational simulating results. For simulation of electrothermal characteristics of SOI CMOS transistor is considered three-layered structure. Temperature distribution is calculated numerically using iterative algorithm in conjunction with software COMSOL Multiphysics. I-V dates of SOI CMOS transistors are calculated by means of two-dimensional models for n-and p-channel transistors of Sentaurus TCAD developed in the system of instrument and technological modelling. TCAD models are calibrated on experimental characteristics for 525 K. It is shown that with growth of ambient temperature the self-heating mechanism contribution consistently decreases. By results of modeling it is established that self-heating contributions at supply voltages 5.5 V to decreases for n-transistor in 2.8 times, p-transistor in 2.2 times. The relative decline of current n-type transistor for reduced from 11.6% to 5.5% and for p-type with 15% to 9%. However, different dynamics of current recession for n-and p-transistors is significant for analog applications that need to be considered at high-temperature circuit design. The proposed methodology allows to critically assess the contribution of the self-heating mechanism on the I-V dates for a wide range of high temperatures and supply voltages. Underestimating this fact leads to unreasonable values for the maximum temperature and limit of thermal stability for the separate SOI CMOS transistor. In total this can be a prerequisite for a significant simplification of the design of not only the chip construction but also the whole electronic Board.***

Keywords high-temperature electronics, the “silicon on insulator” technology, SOI CMOS transistor, self-heating, simulation

I. INTRODUCTION

High-temperature microelectronics is specialized direction of modern electronics products that must operate in temperatures well above commercial range (above 500 K). One of the technological bases high temperature electronics is the SOI (silicon-on-insulator) technology (silicon on insulator), which effectively limits the thermal degradation of key characteristics of silicon CMOS transistor [1, 2]. However, for SOI CMOS transistor thick silicon oxide loaded under thin film channel transistor area is a prerequisite for a clear manifestation of the self-heating mechanism [3].

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It is most highly and dangerously evident in analog applications of the SOI CMOS transistors [4, 5]. In this case, it is the most serious limitation at high values of the gate (Ugs) and drain (Uds) voltages, resulting in a sharp increase in local overheating of the device and, under certain conditions, can lead to the loss of its functional sustainability [6].

In paper for transistors, made on the basis SOI CMOS process with the 0.5 μm topological node, task is to determine the contribution of self-heating effect in their I-V dates in the ambient temperature range above 500 K.

II. TEST TRANSISTOR

For the research capabilities of the technology was developed by test crystal that includes various constructive options of A-tape SOI CMOS transistor which operating in partial depletion regime [7].

Test crystal contains a set transistor structures, provides an opportunity to build SPICE model parameters. The continuity of the basic technology involved the use of SOI structures, SIMOX technology [7]. Their main parameters: the silicon film thickness is 180 nm; the thickness of a insulating oxide layer 150 nm; receptivity p-type substrate 10-20 Ohm×cm.

The gate oxide thickness was estimated by optical measurements on installing APECS 3020 and MOS capacitors and C-V data amounted to 15 nm. Doping profiles of transistor areas is show on fig. 1.

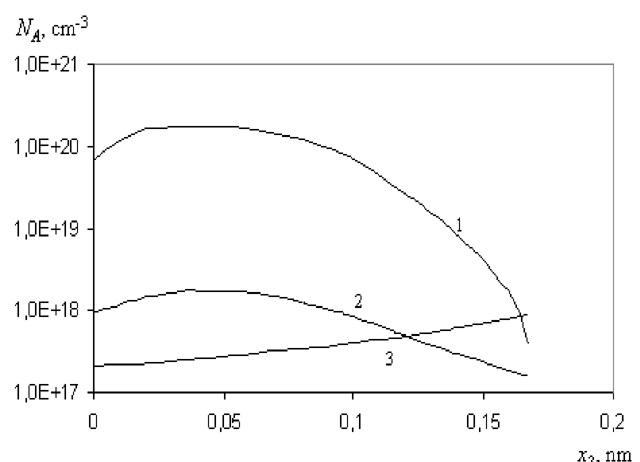


Fig. 1. Doping profiles of transistor areas on depth, where 1 – area a drain/source, 2 – the low-alloyed area, 3 - channel area

Measurement of transistor I-V dates were on the measuring complex Hewlett Packard with probe type device that allows measurements on the plate in the temperature range from 200 up to 600 K. Contribution to self-heating extracted from stock conductivity measurements in pulsed mode [3, 8]. When your test measurements in the temperature range of 425…525 K with step 20 K in each case had to pick up the pulse duration. In this case create a full-scale environmental ambient conditions, including the substrate temperature, the temperature of which above 525 K does not seem technically possible. Therefore, based on experimental data, we numerically investigated influence of self-heating effect on I-V data SOI CMOS transistors in high temperature range.

For simulation of electrothermal characteristics of SOI CMOS transistor is considered three-layered structure (see fig. 2). Each layer is characterized by its own temperature and thermophysical parameters: density, heat capacity, thermal conductivity. The heat source is located on the upper surface of the crystal and takes a hotspot area s_a=*WxL*, где *W*, *L* – width and long of transistor active area.

Considering the fact, that the depth of the position of the working area of the transistor from the top surface of a crystal is considerably less than the thickness of the semi-conductor substrate, it is possible to consider the following approach. Let us assume that the warmth source is located on the top surface of the crystal and occupies the active area of s_a.

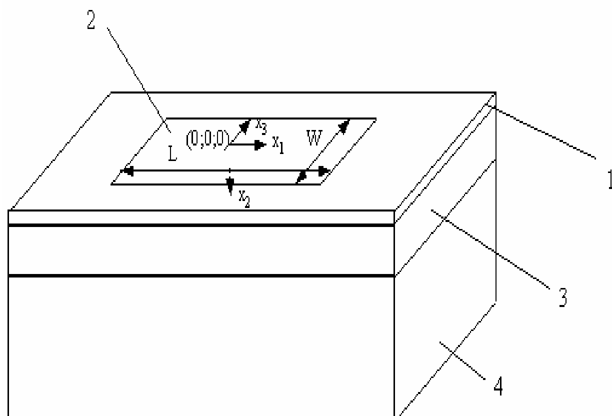


Fig. 2. Block diagram of SOI CMOS transistor, where 1 is a thin silicon film – layer 1, 2-heat source (the active area of the transistor) – layer 1, 3- SiO_2 film – layer 2, 4 - silicon substrate – layer 3

We will also assume that T_a is constant in all of the active area of the transistor and that the power scattered by the transistor depends on the temperature of its active area, that is, $Q_a(T_a)$. The ambient temperature at the distance, many times exceeding the biggest characteristic size of the transistor, we consider as constant and equal to temperature T_0. Taking into account the above assumptions, the warmth distribution in the plate submits to the known stationary equation of heat conductivity [9]:

$$div(\lambda_i(T_i(\bar{x})grad(T_i(\bar{x}))=0\,, \qquad (1)$$

where $\bar{x}\in G_a$ – spatial domains for squared elements $\bar{x}=\{x_1,x_2,x_3\}$.

The boundary conditions on the top surface of the structure

$$\lambda_1(T_1)\frac{\partial T_1(\bar{x})}{\partial n}+\alpha_1 T_1(\bar{x})=\begin{cases}Q_a,\bar{x}\in G_a \\ 0, x\in G_{ts}\end{cases}0, \quad (2)$$

where G_{ts}, G_a – the areas occupied by the top surface of the crystal and the active part, *n* – vector of the external normal to the surfaces, α_1 – coefficient of the convective heat exchange with the environment; *x* – object co-ordinates.

The boundary conditions on the bottom surface

$$\lambda_3(T_3)\frac{\partial T_3(\bar{x})}{\partial n}+\alpha_3 T_3(\bar{x})=0\,, \qquad (3)$$

where $\bar{x}\in G_{bs}$, G_{bs} – area of the bottom surface, λ_3 – coefficient of the thermal conductivity of the heat sink, α_3 – coefficient of the convective heat exchange with the environment.

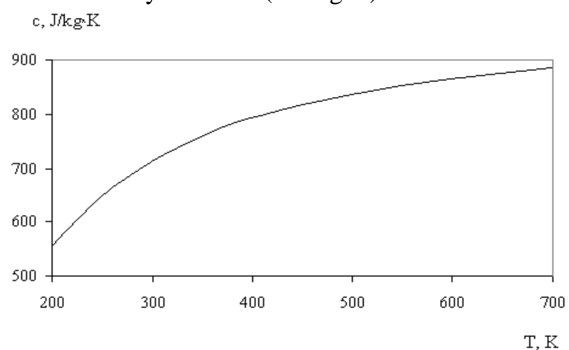
Interface conditions on the borders of contact of the two environments:

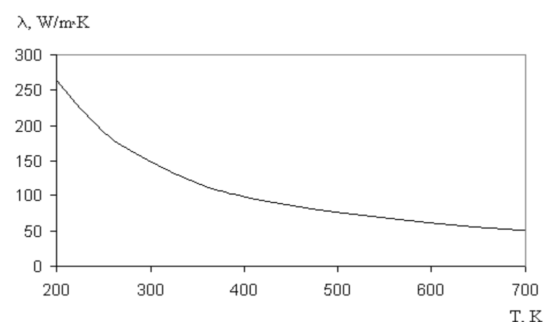
$$\lambda_i(T_i)\frac{\partial T_i(\bar{x})}{\partial n}=\lambda_{i+1}(T_{i+1})\frac{\partial T_{i+1}(\bar{x})}{\partial n}\,, \qquad (4)$$
$$T_i(\bar{x})=T_{i+1}(\bar{x})$$

where G*c (i)* – contact area.

For the purpose of problem simplification, we assume, that the end faces of each layer are heat-insulated, i.e., there is no heat exchange [9]. In fact, the heat exchange from the end faces to the environment is insignificant, because of their small thicknesses, and the end-face heat exchange can be neglected.

Temperature dependences of physical parameters of silicon very much differ [10]. For example, dielectric permittivity at temperature increase practically does not change, its increase can be neglected. However, when heating heat capacity of silicon increases, and heat conductivity and thermal diffusivity decrease (see fig. 3).





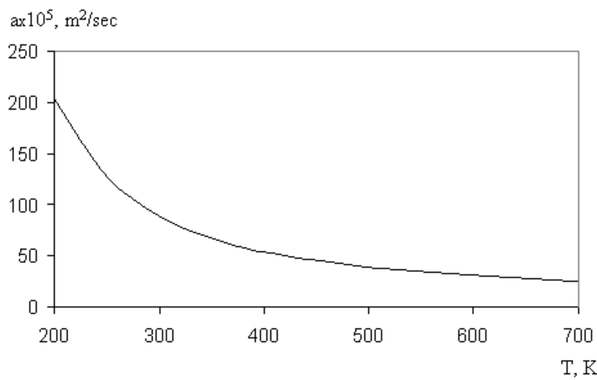


Fig. 3. Temperature dependences capacity (top), heat conductivity (middle), thermal diffusivity (bottom)

At the same time heat capacity increases in the considered temperature range ~ 6%, heat conductivity and thermal diffusivity decrease more than by 30%. Because of such versatile behavior of parameters models become complicated and increase computing resources [11].

The layers have the following geometrical dimensions. Layer 1 $L_{x_1}^{(1)} = L_{x_3}^{(1)}$ =20 µm, $L_{x_2}^{(1)}$ =0,18 µm. Layer 2 $L_{x_1}^{(2)} = L_{x_3}^{(2)}$ =20 µm, $L_{x_2}^{(2)}$ =0,15 µm. Layer 3 $L_{x_1}^{(3)} = L_{x_3}^{(3)}$ =20 µm, $L_{x_2}^{(3)}$ =0,6 mm. Active area *L*=0,5 µm, *W*= 3,1 µm.

I-V dates of SOI CMOS transistors are calculated by means of two-dimensional models for n-and p-channel transistors of Sentaurus TCAD [12] developed in the system of instrument and technological modelling. TCAD models are calibrated on experimental characteristics for 525 K. They are shown in table 1

Tabl. 1. Experimental data n- and p- transistors

Uds,V	**Ids, A n-type**	Uds,V	**Ids, A p-type**
0.0	-7.23E-08	0.0	2.01E-08
0.5	4.32E-04	-0.5	-2.41E-04
1.0	7.62E-04	-1.0	-4.00E-04
1.5	9.00E-04	-1.5	-4.70E-04
2.0	9.54E-04	-2.0	-4.88E-04
2.5	9.46E-04	-2.5	-4.83E-04
3.0	9.52E-04	-3.0	-4.83E-04
3.5	9.54E-04	-3.5	-4.90E-04
4.0	9.53E-04	-4.0	-4.71E-04
4.5	9.36E-04	-4.5	-4.74E-04
5.0	9.38E-04	-5.0	-4.75E-04
5.5	9.38E-04	-5.5	-4.75E-04

The current model for I-V data transistors includes an expanded set of thermal parameters and modified temperature equation, taking into account the temperature dependence of the physical parameters of the silicon [10]. Current model consists of two interrelated components: a strong inversion mode based on temperature-dependent surface distribution capacity [6, 13] and self-heating effect, which in this case is modeled using thermal resistance and thermal capacity values are initially unknown modeling [14, 15]. Therefore, the considered mechanism is the most serious restriction at high values of the gate and the drain voltages. At the low gate voltages the temperature of T_a grows slowly and the influence of the mechanism of self-heating on I-V data of the transistor is insignificant. At high Ugs the parameter of T_a grows very quickly, which causes the self-heating effect in the form of the negative differential conductivity of drain g_{ds}. The value of this conductivity is controlled by the mechanisms of modulation of the length of the channel and the positive thermal feedback [9, 16]. The characteristic frequency of g_{ds} is defined by the thermal time constant $\tau_{th} = R_{th} * C_{th}$. At that, the following interrelation [3] is supported:

$$T_a - T_0 = I_{ds} U_{ds} R_{th} / \sqrt{1 + (\frac{2\pi}{R_{th} C_{th}})^2} \ , \qquad (5)$$

where T_o – ambient temperature.

The dependence of the power density on the temperature of the active area is found from the equation of the electrothermal feedback taking into account the condition of preservation of constancy of the thermal power allocated in the transistor [6, 7]. The equation of the electrothermal feedback looks like the following:

$$Q_a(T_a) = A_{sh} \times$$
$$\times \exp(-\frac{E_g(T_a) - q(U_{gs} + \frac{r}{U_{ds}} Q_a(T_a))}{kT_a}) \ , \qquad (6)$$

where *r* – input resistance of the transistor; $E_g(T_a)$ – temperature dependence of the width of the forbidden zone of silicon [10]; A_{sh} – proportionality coefficient, independent of temperature; q – electron charge; *k* – Boltzmann constant. Temperature field in the three-layer structure is from the solution of equations of heat conduction and electrothermal feedback [14], taking into account the fact that, firstly, the temperature of the active region of the transistor T_a is the same in each point and, secondly, the power transistor power depends on the T_a. The temperature distribution is calculated numerically using an iterative algorithm in conjunction with the COMSOL Multiphysics software [17] environment until the power dissipated by the transistor changes. The resulting temperature distribution with a set value of electrical power is used to calculate the transistor currents. Currents are calculated using two-dimensional TCAD models for n-and p-channel transistors.

III. RESULT AND DISCUSION

On Figure 4 shows the simulation results of core temperature dependence that characterize the self-heating effect on I-V dates of SOI CMOS transistors.

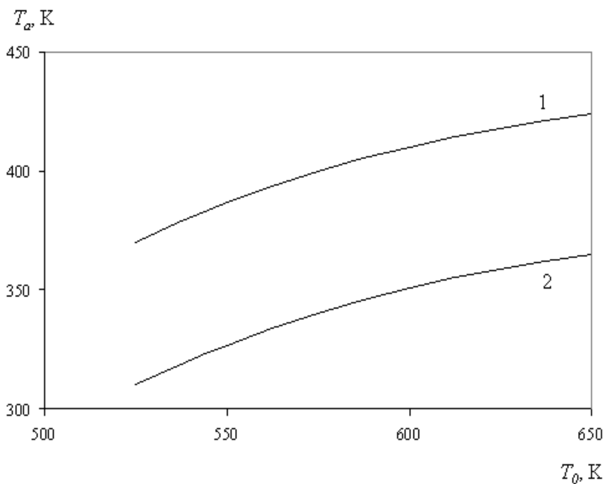


Fig. 4. Dependence Ta (To) at Uds=Ugs=5.5 V, where 1 - transistors of n-type, 2 - the p-type transistor

According to the presented Fig. 4 illustrates the change in temperature of the active area of the transistor n- and p-types with increasing ambient temperature. Note that they have the same slope, and high temperatures parameter $\Delta T = T_a - T_0$ is modest.

I-V dates Ids(Uds) at Ugs = 5.5 V of SOI CMOS transistor n and p-type are show on Fig 5.

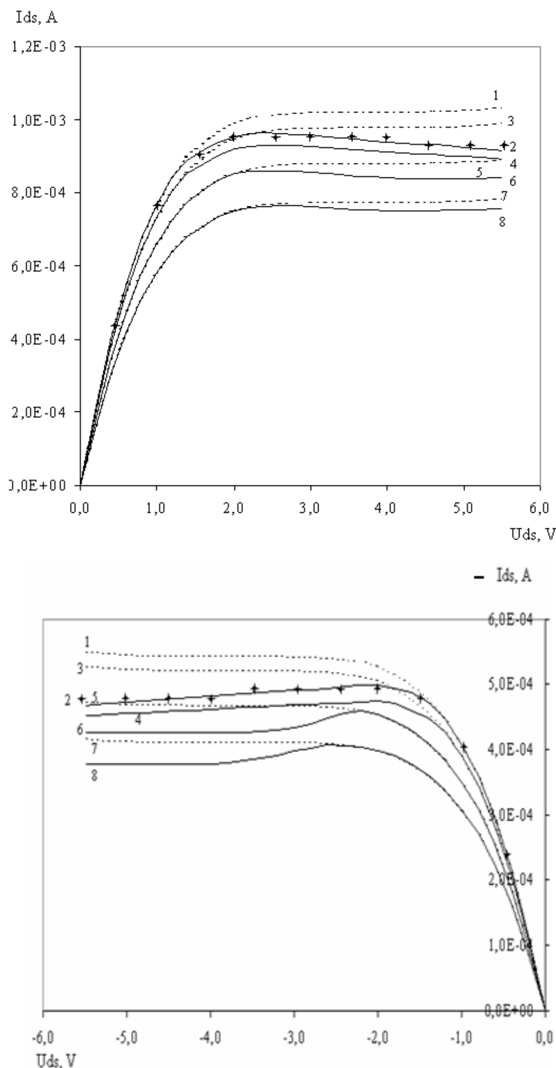


Fig 5. I-V data *Ids(Uds)* SOI CMOS transistor, where top figure – n-type transistor, bottom – p-type.

Here 1,2 - T_0=525 K, 3,4 - T_0=550 K, 5,6 - T_0=600 K, 7,8 - T_0=650 K,
the odd index of curves - without self-heating, even index - taking into account self-heating.
Asterisks showed experimental data.

They allow you to assess the self-heating impact at range high ambient temperature. The results show that calibration of transistor models held at an acceptable level-maximum deviation is less than 3%. The difference in the behavior of I-V dates for n-and p- SOI transistor is directly related to temperature-dependent characteristics of charge transfer [7]. By the results of modeling shows that the self-heating mechanism for SOI CMOS transistors of both types is noticeable, and their I-V dates have a pronounced "negative differential resistance" [3]. With increasing temperature, this contribution is gradually decreasing. In the table 2 for the transistor n-and p-types are transistor currents (Ids) and reduction of transistor current (ΔIds), caused by the action of self-heating at voltages Uds = Ugs = 5.5 V.

Tabl. 2. Temperature characteristics of current transistors.

T_{0}, K	**Ids, A n/p**	**ΔIds, A n/p**
525	$1,03x10^{3}$/ $-5,50x10^{-4}$	$1,21x10^{-4}$/ $-0,83x10^{-4}$
550	$9,89x10^{4}$/ $-5,26x10^{-4}$	$1,02x10^{-4}$/ $-0,75x10^{-4}$
600	$8,95x10^{4}$/ $-4,72x10^{-4}$	$0,58x10^{-4}$/ $-0,47x10^{-4}$
650	$7,88x10^{4}$/ $-4,15x10^{-4}$	$0,43x10^{-4}$/ $-0,38x10^{-4}$

From the simulation results should be that the recession of current transistors with increasing temperature T_o consistently dropping. When this contribution mechanism depends on T_o values. In general, dependency ΔIds(T_o) nonlinear and has its own characteristics for each type of transistor. In the temperature range investigated the contribution of self-heating when Uds = Ugs = 5.5 V to decreases for n-transistor in 2.8 times, p-transistor in 2.2 times. The relative decline of current n-type transistor for reduced from 11.6% to 5.5% and for p-type with 15% to 9%. Differences in the dynamics of the current downturn transistors due to self-heating can be substantial for analog applications [2, 13] that must be considered when designing high-temperature circuits.

It should be noted that the methodology of accounting for the influence of self-heating mechanism developed in the present work, gives equal to experimental data results in most cases analog applications executed on 0.5 micron technology for commercial temperature range [11].

IV. CONCLUSION

On the basis of experimental data has developed a methodology for assessing the impact self-heating effect on current-voltage characteristics of submicron SOI CMOS n- and p-type transistors at high (above 500 K) ambient temperatures and high supply voltages. A detailed account of this process enables you to

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reliably estimate the decrease in the transistor current that nonlinear manner depends on the ambient temperature. According to the simulation in the temperature range from 525 to 650 K self-heating contributions when Uds = Ugs = 5.5 V to decreases for n-transistor in 2.8 times, p-transistor in 2.2 times. The relative decline of current n-type transistor for reduced from 11.6% to 5.5% and for p-type with 15% to 9%. This different current dynamic for n-and p-transistors is meaningful for analog applications that must be considered when designing high-temperature circuits.

The proposed methodology allows you to critically assess the contribution of the self-heating effect. It is extremely relevant and important task for developing and designing chips for analog applications. Underestimating this fact leads to unreasonable values for the maximum temperature and limit of thermal stability for the separate SOI CMOS transistor. In total this can be a prerequisite for a significant simplification of the design of not only the chip construction but also the whole electronic Board.

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