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# Implementation of Audio CODEC with a Novel Design Methodology

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***Abstract*: Currently in the real-time audio applications fixed point CODEC is being used. But the major disadvantage of such CODEC is the speed and accuracy. Because , as the DSP systems cannot be operated with real-time signal 't', but they can be operated with the discrete time 'n' , the real-time analog signal x(t) is to be converted into discrete time signal x(n) by the analog to digital convert (ADC). The most widely used ADC in the signal processing environment is sigma-delta ADC. But, it can operate with the maximum speed of 1MHz. The DSP processor can give several times more speed than sigma-delta ADC. Hence, the speed of DSP system is being limited by sigma-delta ADC, even though the DSP system has the capability to operate with great speed. Similarly, the accuracy is being missed because the floating point samples are converted into fixed point to get the compatibility with fixed point DSP processor. To eliminate these two bottlenecks the novel design methodology has been proposed in which the ADC and DAC have been eliminated and the system is developed by the 16 bit floating point.***

***Keywords: fixed point CODEC, speed and accuracy, DSP systems, ADC, DAC, 16 bit floating point.***

## I. INTRODUCTION

CODEC is the acronym of coder and decoder. CODEC is used in audio signal processing applications. In the real time, all the natural signals are in the form of analogue. For example speech signal, voice signal, Electroencephalogram (EEG) signal, Electrocardiogram (ECG) signal, earthquake or seismic signal etc. In the olden days the analogue signals were used to process through analogue systems, for example analogue radio, analogue camera, analog TV etc are used to process the continuous signals. These analog systems were made with active and passive components. As the technology is being advanced, Digital Signal Processing (DSP) systems have come into the picture. Hence, now a days, almost all the signal processing systems are in digital. The real time analogue signals cannot be processed directly on the digital signal processing systems because the real time analogue signals vary with continuous time 't' but the digital signal processing systems operate with descript time 'n'. Hence, Analog to Digital Converters (ADCs) and Digital to Analog
Converters (DACs) are necessary at the input and output of the DSP system respectively. Hence first we have to convert the real time analogue signal into digital and then need to be processed on DSP system. To convert real time analogue signal to digital signal, there are various analogue to digital converters. They are parallel or flash type ADC, ramp type ADC and successive approximation type ADC. Similarly to convert the processed digital data into an analogue signal, the important DACs which are used in DSP are binary weighted resistor type and R-2R ladder type. The main advantages of DSP systems are utmost easily data can be stored, time sharing, configuration flexibility and cheaper.
In order to convert analogue signal to digital signal we have to use sampler, quantizer and coder. Sampler performs the sampling operation. Sampling is nothing but cutting the analogue signal at some sampling rate (fs). While sampling the analogue signal sampling theorem is to be followed. It can be revealed as- $f_s$ is greater than or equal to $2f_m$, where $f_s$ is equal to sampling rate and $f_m$ is nothing but maximum frequency. If $f_s$ is less than $2f_m$, it is called under sampling due to which aliasing occurs. If $f_s$ is greater than $2f_m$, it is called over sampling due to which signal can be reconstructed well at the output of the receiver without any aliasing. Hence, for all DSP applications over sampling is preferred. There are various limitations in the present CODEC system. The first limitation is- In most of the DSP applications, sigma-delta ADC and DAC are used to convert the analogue signal to digital and digital signal to analogue respectively. The major limitation of sigma-delta ADC is its speed. It can operate with the speed range of 100K hertz to 1 Mega hertz which means that it can give the maximum speed of 1 Mega hertz only. But DSP processor can operate with more than 1 Mega hertz speed. Hence, even though the DSP processor is having the ability to operate with good speed, it is being limited by sigma-delta ADC. It is known fact that after sampling, each and every sample is in float value but they are converted into fixed value because fixed point DSP processor is used to design the conventional (fixed point) CODEC. The second limitation is- the db4 filter co-efficients which are used for audio CODECs are in floating point values.

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But, they are converted into fixed point because fixed point DSP processor is used for the design of conventional CODEC [1]. Hence, due to above two limitations, speed and accuracy are not attained well. To eliminate the above two limitations, a novel design methodology to design novel CODEC (3-stage DWT) with floating point is proposed. Here we have to develop user defined 16 bit floating-point packages to design novel CODEC (3-stage DWT). After designing, to process the analog signal through the novel floating point CODEC, the analog signal equivalent floating point values are extracted through the Matlab tool. Hence, ADC and DAC can be eliminated at the front end and back end of the novel floating point CODEC system. The total design is simulated, synthesized with the compilation of packages on Xilinx ISE 14.7 tool.

## II. DISCRETE WAVELET TRANSFORM DESIGN

If we compare wave and wavelet, wave has infinite length of duration whereas wavelet is having the finite length of duration. For the wave, average value is not zero but for wavelet average value is equal to zero. Wavelets are specially developed to extract the unknown signals of EEG, ECG, and certain audio signals. There are various wavelets like Har wavelet, db4 wavelet, db6 wavelet and Mexican-hat wavelet etc,. Db4 wavelet coefficients are used to process the audio applications [2]. Db6 wavelet coefficients are used to identify certain properties of medical signals like EEG and ECG signals. These db4 and the db6 coefficients had been invented by Ingrid Debauchy, a professor in physics. Hence, to design audio CODEC in real time using floating point, one should use db4 coefficients. There are various types of transforms 1. Fourier transform 2. short time Fourier transform and 3. wavelet transform. The disadvantage of Fourier transform is- it can analyze only frequency resolution but time resolution cannot be analyzed. The disadvantage of short time Fourier transform is the window size is fixed (see figure1). If window size is varied it cannot be applied [3].

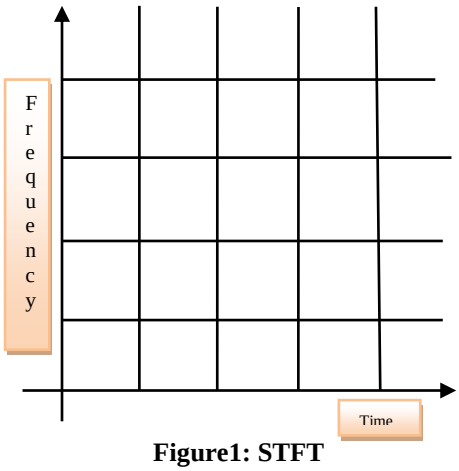


**Figure1: STFT**

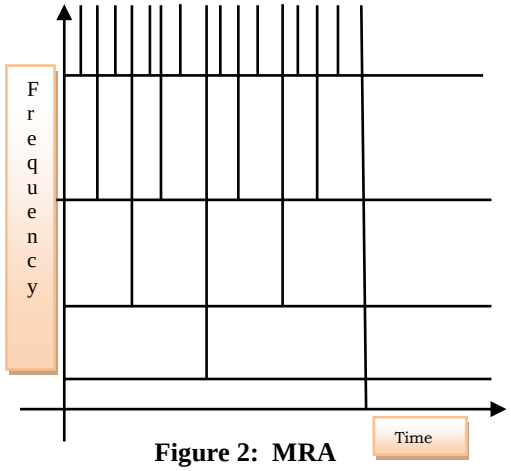


**Figure 2: MRA**

Hence, we need to opt discrete wavelet transform, it is used to carry multirate analysis. In this, time is varied as well as frequency also is varied (see figure2). It can analyze both time and frequency varying signals which means that wavelets are used to analyze non-stationary signals [4].

### A. 3- Stage Floating Point DWT Implementation

**Decomposer**

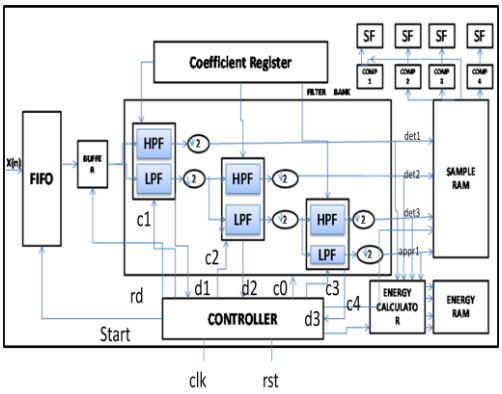


**Figure3:Decomposer**

**Re-constructor**

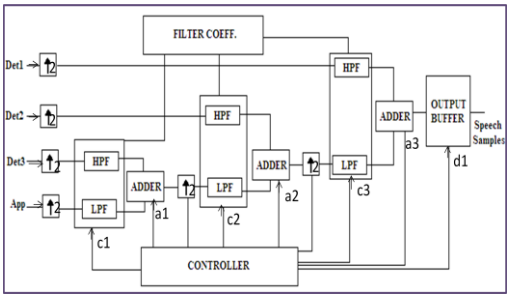


**Figure4: Re-constructor**

Figure 3 and 4 show the 3 stage decomposer and reconstructor respectively. To design three stage DWT, FIR high pass and low pass filters are used [5]. FIR filters are more appropriate than IIR filters to design the three stage DWT because they are stable, they can be designed to linear phase and also limit cycles are not produced because there is no feedback in FIR. FIR filters can be designed with various methods like Fourier series method, frequency sampling method and windowing method. But windowing method is preferred because here db4 window is used to design the three stage DWT.

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**Principle of Operation:**

In this work, we are going to implement the three stage 16 bit floating point DWT or novel floating point CODEC. Why the word length is 16 bit means this much of bit length is sufficient to design audio CODEC because this is a co-processor. If more floating point bit length is taken, the memory will be wasted. The system consists of various sub-blocks like FIFO, buffer, controller, coefficient register, three filter banks and each filter bank consists of one high pass filter and one low pass filter, sample RAM, energy RAM, scale factor and four component registers. The input samples of x(n), which are in the form of 16 bit floating point are applied to the input of FIFO. After it has been filled with complete 16 samples then the first sample will be sent to buffer whenever control signal is sent by the controller. These floating point samples will be applied to first filter bank through the buffer.

These samples are convolved with db4 filter co-efficients come from the coefficient register. The output of the first filter bank will be detail and approximate coefficients. The detail co-efficients are from the output of high pass filter and the approximate co-efficients are from the output of lowpass filter. The detailed co-efficients are stored in the sample RAM and the approximate coefficients are sent to the second FIR filter bank. In second filter bank also the approximate co-efficients come from the first filter bank are convolved with the db4 co-efficients come from the co-efficient register and the outputs from the low pass filter which are approximate co-efficients are given to the third filter bank and the detailed co-efficients will be stored in the sample RAM. In the third filter bank also after convolution, both the detailed and approximate co-efficients are stored in the sample RAM with decimation by 2. The four components which are detailed co-efficients are three and approximate co-efficient is 1 are sent to the receiver after some scaling factor is added. The energy of each co-efficient will be calculated by energy calculator and will be stored in the energy RAM. Like this all 16 samples which are stored in FIFO in the form of floating are decomposed by the three sub bands and after decimation they will be sent to the receiver or synthesis section.

The synthesis section or receiver section is exactly vice-versa to the analysis section or transmitter section. In the analysis section whatever the number of samples are decimated, the same number of samples are interpolated in the synthesis section. Because decimated by 2 in the analysis section is used, in the synthesis section also interpolated by 2 has used. After that they will be passed through the filter banks; each filter bank consists of one high pass filter and one low pass filter. After convolution operation with the db4 filter co-efficients, the output of both low pass filter and high pass filter are added by adder and then the signal is interpolated by 2. Like this the input signal is reconstructed well after the signals have been passed through all the three filter banks at the output of the receiver. Here also the control register will control each and every part of the section by sending control signals. Filter coefficients register will send the db4 filter co-efficients to all the low pass filter and high pass filters.

## III. 16-BIT FLOATING POINT PACKAGES DEVELOPMENT IN VHDL

**Simulation process**

Above figure 5 shows the simulation process. It shows that there are various design units like design unit 1, design unit 2, like this to till design unity n. After VHDL analysis they will be sent to design library. Design library is the area to store the various file systems. Design libraries consist of standard library, IEEE library, book library and working library. IEEE standard library consists of standard_ logic_1164, standard_logic_arith, standard_logic_ unsigned, standard_ logic_ signed and numeric_ standard etc,. Standard and Textio are the packages under the standard library STD.

For current work, the library work is the specific library set by the user. In this work the goal is to implement high speed 16 bit floating point CODEC for audio applications. Since the implementation is in floating point, it takes more memory hence the design is implemented through Discrete Wavelet Transform (DWT). Using discrete wavelet transform the data is compressed and hence memory is saved. Whatever the data is compressed, the same is interpolated and hence the sending data will be recovered at the receiver without any disturbance.

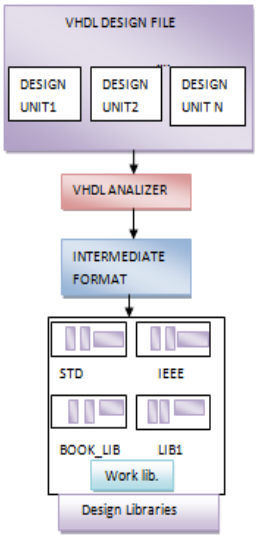


**Figure 5: Simulation Process**

In order to implement MAC by 16-bit floating point adder, shifter and multiplier a library package is developed with user define record type as given below:

*type real_single is*
*record*
*sign : std_logic;*
*exp: std_logic_vector(3 down to 0);*
*mantissa: std_logic_vector(10 down to 0);*
*end record;*

The floating-point notation is realized using 16 bit IEEE-754 standard as shown in Figure 6.

| Sign (1) | Mantissa (11) | Exponent (4) |
|---|---|---|

**Figure 6: IEEE 754 standard for half precision**

## IV. NOVEL DESIGN METHODOLOGY

In the conventional design approach, 16 bit fixed point CODEC was designed but in the novel design approach the CODEC is designed with IEEE 754 16-bit floating point standard library.

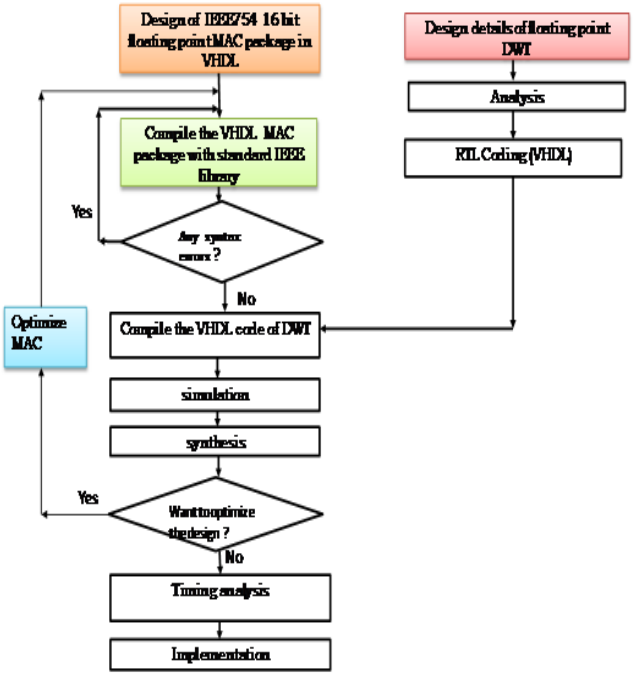


**Figure7: A novel design methodology**

The novel design methodology is shown in above figure7. Initially, by following the IEEE 754 standard, 16-bit floating point adder, multiplier and shifter are designed after that a MAC which is multiplayer accumulator content is designed. These user defined MAC is compiled with IEEE standard library. After confirming there are no syntax errors, compile it with the floating point DWT design code developed earlier. Then simulate and synthesize the design. In simulation results, we can observe the input and output 16-bit floating point values whereas in the synthesis reports we can observe the speed of the overall system.

## V. RESULTS AND DISCUSSIONS

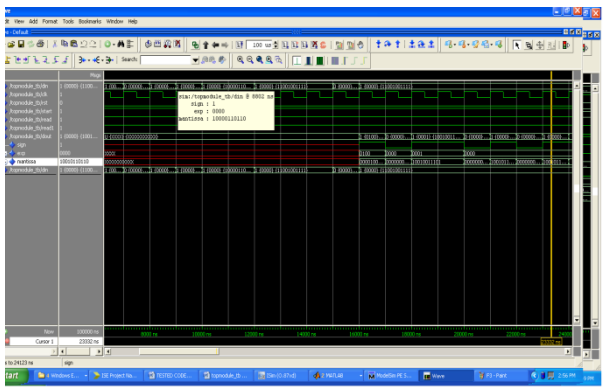

**Figure8 : screen shot with input – output values**

**Table1: binary representation**

| Figure | At Time | Input Value (Binary) | Output Value (Binary) | Error |
|---|---|---|---|---|
| 8 | t1 | 1000010000110110 | 1000010010110110 | Zero |

**Table2: decimal representation**

| Figure | At Time | Input Value (Decimal) | Output Value (Decimal) | Error |
|---|---|---|---|---|
| 8 | t1 | $-7.6444*10^{-06}$ | $-7.6444*10^{-06}$ | Zero |

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**Table3: synthesis report**

| Various parameters | Utilization |
|---|---|
| No.of input-outputs | 106 of 182(57%) |
| N0.of basic elements | 206 of 1728(11.8%) |
| Min. time period | 2.649 nano second |
| Maximum speed | 377.501 Mega Hertz |
| Power utilization | 38.47milli watt |

The above figure 8 shows the screenshot for the input and output of the floating point DWT or novel floating point CODEC at some specific instant of time t1. Its values in floating point binary and floating point decimal are shown in table 1 and table 2. It illustrates that the error is zero between transmitted signal and received signal even though the system has been designed and operated with floating point values. The synthesis report gives delay, speed, power consumption and area in terms of memory elements. If we observe the speed of this novel DWT, it operates with good speed that is 377. 501 MHz which is several folds higher than conventional design of DWT which has only 20 MHz speed. The power consumption is 38.47 mW.

## VI. CONCLUSION

In this work the floating point CODEC has been developed through the multirate analysis concept using discrete wavelet transform. The ADC, DAC have been eliminated with the novel design methodology hence, the speed limitation of the conventional work could overcome. The accuracy also had been improved greatly between transmitted and received signal; the tabular forms 1 and 2 show the clear cut analysis.

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