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Implementation of 5-Stage 32-Bit Microprocessor Based Without Interlocked Pipelining Stages

S. Aruna, K. SrinivasaNaik, D.Madhusudan, V.Venkatesh

Abstract: ***Many processors have evolved in the past century; Out of which, Reduced Instruction set Computing (RISC) processors are well known for their ease of use. The next in line was the Microprocessor without Interlocked pipelining stages (MIPS) RISC based architecture. Less number of instructions, good amount of registers makes these processors a boon to use. Often times, MIPS processors loose the battle against their contenders due to lack of speed. Hence, there is a sheer necessity in designing a more robust system that has all the advantages of MIPS. Over time, there have been designs that could solve the power drawbacks and the area optimizations. However, performance criterion is mostly neglected. This paper emphasizes on the performance metric of pipelined 32-bit MIPS microprocessor. This processor supports RISC architecture and has been designed under Harvard architecture. Pipelining technique is used to solve the problem of low performance and achieve smaller execution times. The processor has four pipes. Pipes are the structures which store data. Pipes can be viewed as register banks. These pipes are generally used to store the intermediate data. The design contains various modules like ALU, Instruction fetch register, Execution unit, Memory, Program counter (PC). Verilog HDL has been used to implement the design. The software used is Xilinx ISE for design and ISIM simulator has been used for simulation purposes. The applications of this MIPS microprocessor are abundant. MIPS microprocessor can be used to carry out the fundamental tasks and an application specific core/IP/processor can be designed and combined with MIPS. This facilitates in meeting the goals of high performance, lower time-to-market and cost- effectiveness. Some application specific uses can be for music systems, PDA, Image processing etc.***

Keywords: ***ISIM simulator, MIPS, Pipeline, , RISC architecture, Verilog HDL..***

I. INTRODUCTION

MIPS processor can be regarded as one of the robust processors which form the basis for design of various advanced microprocessors.

As MIPS are present in the open-source, edits can be made to it by anyone and anywhere. It is categorized under the reduced instruction set computing (RISC) architecture. The said architecture provides the user with less number of instructions and thereby reducing the burden of remembering too many instructions to program it.

The MIPS processor doesn't come with any flags. This can however be seen as a limitation [1-4].

The advantages of flags in the micro-processor world are numerous. However, the MIPS carry some of these tasks with added complexity. The real deal breaker for the processor along with its processing speed is it's time-to- market. Advantages of MIPS include low time-to-market and lower system cost. 32-bit MIPS processor has an ALU capable of processing 32-bit operands at a time, 32- bit dedicated address and data lines. The processor has separate memory for program and instructions, thereby supporting Harvard architecture. Only two instructions can access the memory [5-6]. They are Load and store. The Load instruction loads the instruction from the memory and the store instruction stores the data into the memory. It can be noted that both memory load and store cannot take place at the same time. If such a situation occurs where the load and store are to be taken place simultaneously, it results in hazard.

II. MIPS ARCHITECTURE

The MIPS processor has 5 stages namely: Instruction Fetch stage (IF), Instruction Decode stage (ID), Execution stage (EX), Data memory stage (MEM) and write back stage (WB). The Instruction Fetch stage has Instruction Memory and Program Counter. The Instruction Decode stage consists of Registers and control unit. ALU, ALU control are a part of the Execution stage. The Memory registers are a part of the Data memory stage. The write back stage consists of hardware that writes back data into the memory. The architecture of MIPS processor can be seen in figure 1. It is a well- known fact that MIPS can be used even today for the SoC development. The registers are named rs, rt and rd. rs register corresponds to source register, rt corresponds to target register and rd corresponds to destination register.

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* Correspondence Author
S.Aruna*, Assistant Professor, Department of ECE, College of Engineering (A), Andhra University, Visakhapatnam, India.
K.Srinivasa Naik, Associate Professor, Department of ECE Vignan's Institute of Information Technology (A), Visakhapatnam, India
D.Madhusudan, Assistant Professor, Vignan's Institute of Information Technology (A), Visakhapatnam, India
V.Venkatesh, Student, Andhra University College of Engineering (A), Visakhapatnam, India.

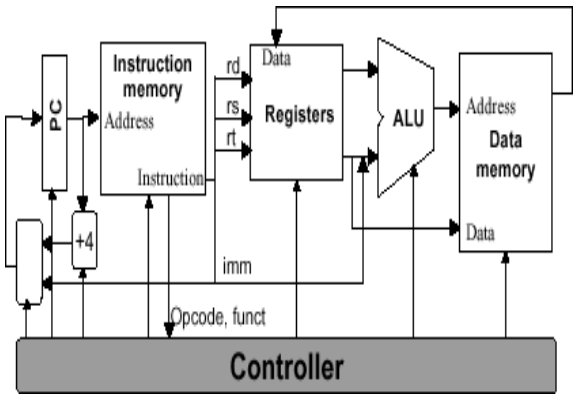

Fig.1: Basic Architecture of non-pipelined MIPS

III. PROPOSEDWORK

Pipelining:

It takes normally one clock cycle to complete one stage. Pipelining is the technique in which multiple stages can take place in just one clock cycle thereby improving performance. For suppose, IF, ID, EX, MEM, WB stages are pipelined. The first instruction takes five clock cycles to complete the execution. In pipelined structures, the second instruction is loaded during the execution of first instruction itself. Similarly, the third, fourth and fifth instructions are loaded one after another in consecutive clock cycles. In non-pipelined structure it would take 25 cycles to completely execute five instructions but in pipeline structure it would only take 9 clock cycles to execute five instructions. Fig.2 illustrates the working of pipelining in a tabular form.

Clock cycle / Instr. No.	1	2	3	4	5	6	7
1	IF	ID	EX	MEM	WB		
2		IF	ID	EX	MEM	WB	
3			IF	ID	EX	MEM	WB
4				IF	ID	EX	MEM
5					IF	ID	EX

Fig.2: Working of pipeline structure

Pipelining is the process of introduction of pipes/registers as intermediate stages to improve the performance. Pipes are basically storage elements. They store the important data necessary to carry out the next stage. Suppose an instruction is executed in the Instruction fetch stage (IF) and has some intermediate data that has to be forwarded to the Instruction Decode stage (ID). To reduce the time in which the next instruction can be loaded, pipelining comes to rescue. A first pipe/register by the name IF/ID register is introduced and the important data that has to be sent to ID stage is now stored in this register. The name IF/ID suggests that this pipe/register is presents between IF and ID stages. Once this data is stored, there is no worry about the loss or corruption of data. Also, once this data is stored in the IF/ID register, the next instruction can be processed by the IF stage.

The ID and EX stages share some data in between them. To speed up the process of data being stored and loaded into the next stage, a second pipe by the name ID/EX register is introduced. The data from the execute stage can be stored in the EX/MEM register. This data can then be used by the MEM stage. The MEM/WB register stores important data of MEM stage and forwards it to the Write-back stage. The ID/EX register is introduced in between Instruction Decode and Execution stages. The EX/MEM register is introduced in between the Execution stage and Data memory stage. Similarly, the MEM/WB register is introduced in between the Data memory stage and the Write back stage. Four pipes will be present in a five stage pipelined structure. This is obvious as each pipe resides between two consecutive stages. MIPS are architecture without interlocked pipeline stages. This means that there is no extra hardware present to check for the hazards encountered. In the proposed work, data hazards have been removed by installing stalls. A total of four pipes/registers were introduced into the architecture of the MIPS processor. These registers help in speeding up the processor. The architecture can be seen in Fig.3.

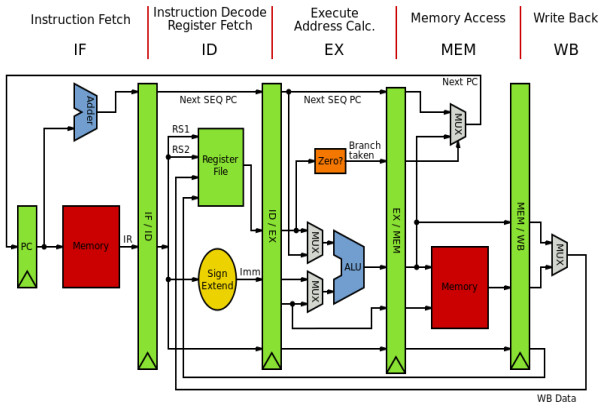

Fig.3: Basic architecture of Pipelined MIPS

IF/ID REGISTER:

The said register is present between instruction fetch and instruction decodes stages. The IF/ID register is designed to be a combination of two registers: IF/ID PC register and IF/ID instruction register. Each of these registers is 32-bit long and are made by combining several 1-bit D flip flops. They have pins write enable, reset, clock. The reset and clock are connected from the top level. The IF/ID PC register retains the Program Counter (PC) value while IF/ID instruction register retains the instructions. The structure of IF/ID can be seen in Fig.4.

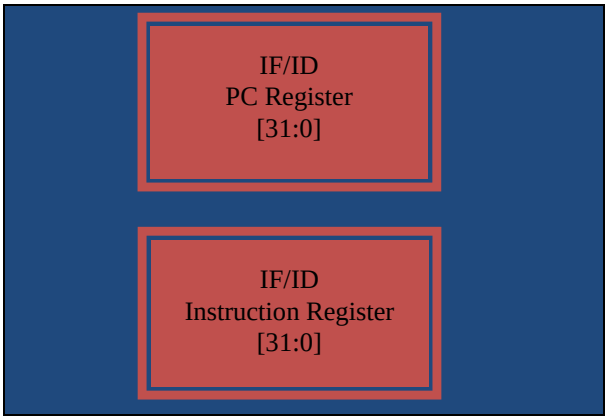

Fig.4: Block diagram IF/ID register

ID/EX REGISTER:

The said register is present between Instruction decode and Execution stages. The ID/EX register is designed to be a combination of 11 registers. These 11 registers are: A pair of Read data registers, rs, rt, rd register, destination register, ALU source register, memory to register, register write, memory read, memory write, ALU operand 1, ALU operand 2. Each register has its own functionality. They basically store data from the Instruction decode stage. Fig.5 depicts the block representation of ID/EX register.

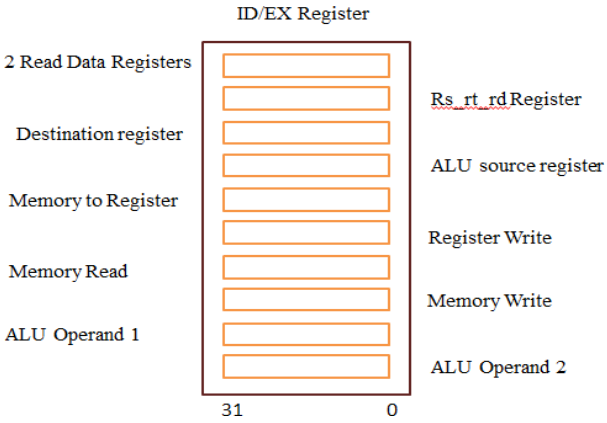

Fig.5: Block representation of ID/EX Register

EX/MEM REGISTER:

EX/MEM register is also a combination of eleven 32-bit registers. They are: ALU result, write data to memory, memory to register, register write, memory read, memory write and five write registers. These registers store the intermediate values. ALU result register stores the result from the ALU. The write data to memory register stores data that has to be saved into the program memory. The memory to register stores data that has to be loaded into the registers. The register write saves data that has to be written into the registers. Memory read stores data read from the memory. The memory writes stores data that must be stored into memory. The five write registers come in handy to store any further values.

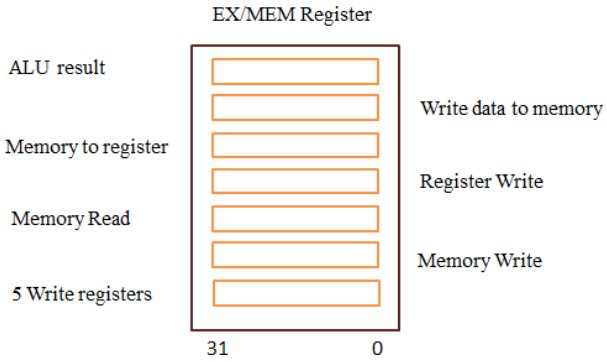

Fig.6: Block diagram of EX/MEM register

MEM/WB REGISTER:

MEM/WB register is designed with nine registers each of 32-bit long. These nine registers are read data of memory, ALU result, memory to register, register write, five write registers. Fig.7 depicts the block representation of MEM/WB register.

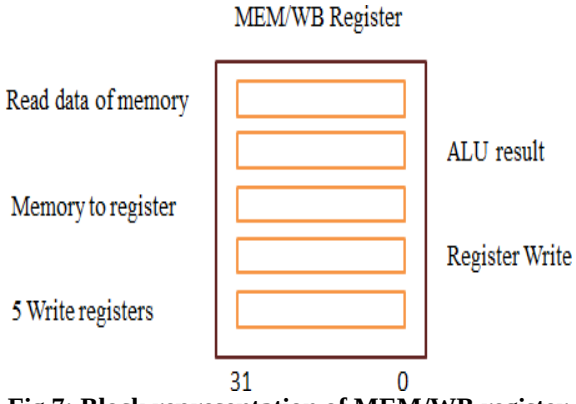

Fig.7: Block representation of MEM/WB register

DATA HAZARDS, FORWARDING AND STALLS:

MIPS non-pipelined structure doesn't come with hardware that could detect or correct hazards. Hence, a data forwarding and stall control block has been introduced in the work. The main purpose of the stall control block is that it stops the execution. This is necessary when a hardware resource is being requested by more than one instruction at a time.

IV. RESULTS

Design of the processor is carried out in Verilog HDL and ISIM simulator has been used for simulations. The time taken to execute an instruction is tabulated. Fig. 8 illustrates the RTL view. Fig. 15 illustrates the simulated results.

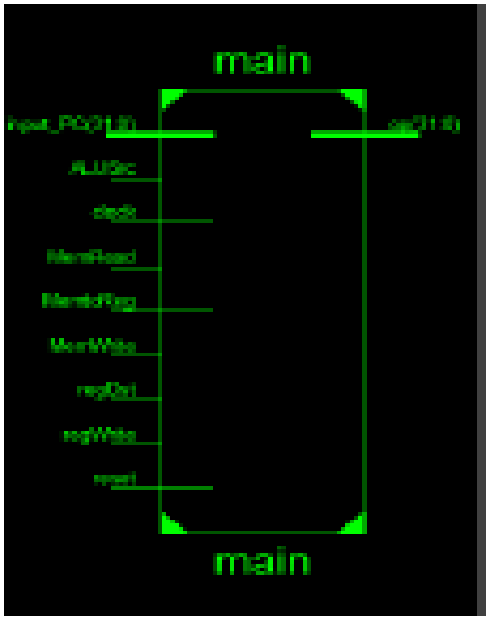

Fig.8: Schematic view of proposed work

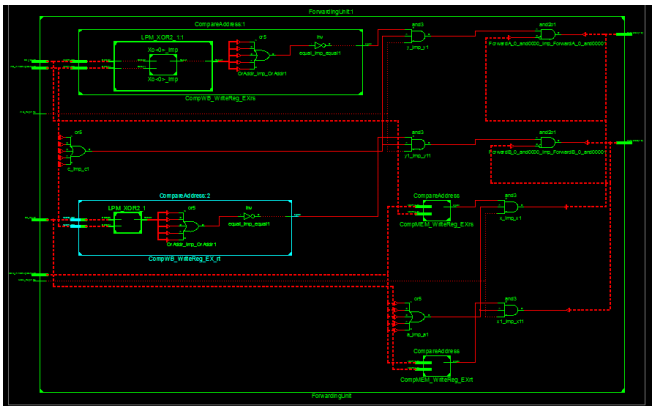

Fig.9: Register Transfer Level view of forwarding unit

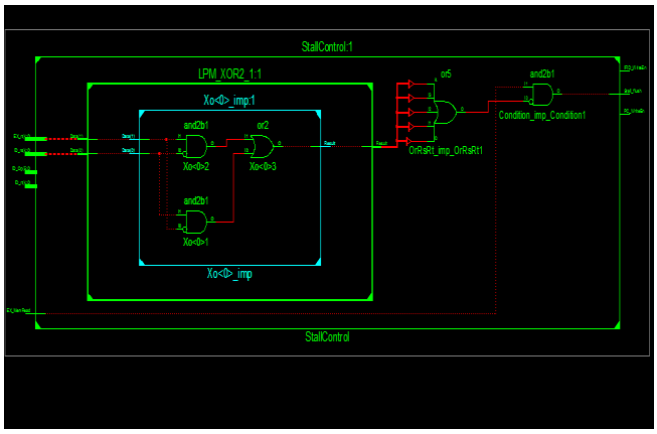

Fig.10: Register Transfer Level view of stall control block

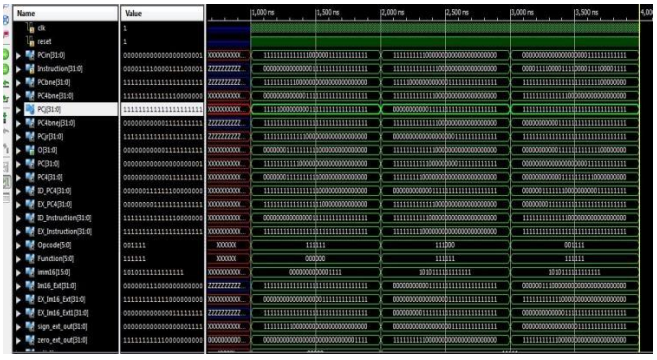

Fig.11: Simulation results of proposed MIPS architecture

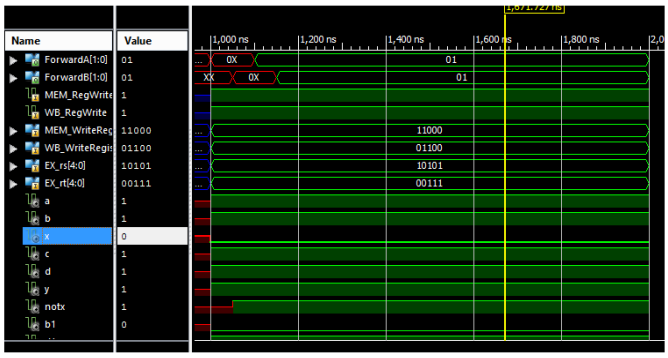

Fig.12 : simulation waveform of Forwarding unit

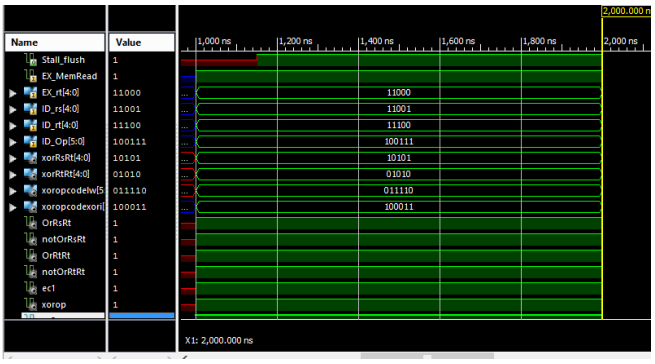

Fig.13: Simulation waveform of Stall control block

Fig.14: Simulation waveform of control unit

Table 1: Comparison of time taken to execute instructions

Instruction	Non-Pipelined Architecture (Existing) (in ns)	Pipelined System Architecture (Proposed) (in ns)
R-Type	2500	1000
J- Type	2500	1000
I-Type	2500	1000

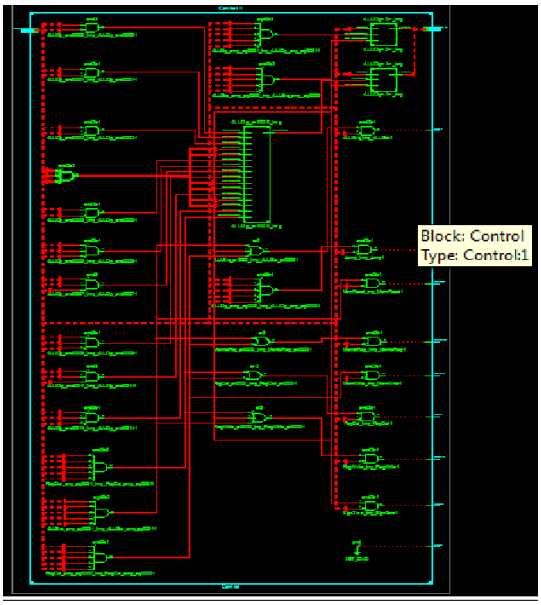

Fig.15: Register Transfer Level view of Control unit

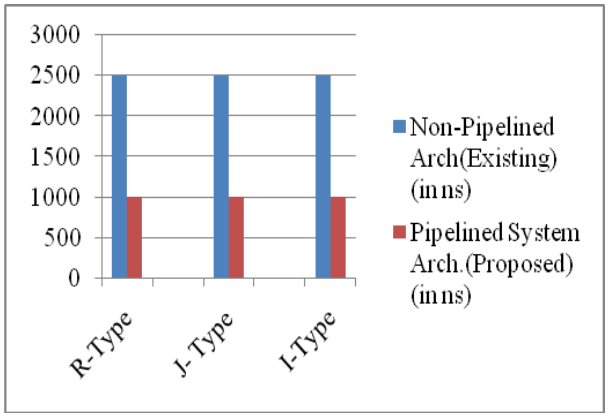

Fig.16: comparison of time taken to execute instruction in existing vs proposed model

V. CONCLUSION

The performance metric of pipelined 32-bit MIPS microprocessor has been designed with Harvard architecture which supports RISC architecture. The proposed work designed by using Verilog HDL with R-type, J-Type, I-Type instructions. Pipelining system is used to solve the problem of low performance and achieve smaller execution times. The instruction execution time in the non-pipelined structure is observed to be 2500ns. With the pipelining architecture, this parameter has been reduced to 1000ns. Thus, a small amount of registers incorporated into the design results in improved performance like high performance, lower time-to-market, cost-effectiveness.

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AUTHORS PROFILE

Dr.S.Aruna received her B.E from SRKR Engineering College, M.Tech from JNTU, Kakinada and Ph.D from Andhra University. She is an Assistant Professor in Andhra University College of Engineering (A), Currently, She is Head of the Department in Andhra University College of Engineering (W) and Published about 40 technical papers in National/ International Journals/ Conference Journals. Her Research interests include Array Antennas, EMI/EMC and Waveguides. She is a Life Member in Instrument Society of India L.M.No.15987 (India).

Dr. K. Srinivasa Naik received Bachelor of engineering in Electronics and Communication Engineering from Sir C.R.R College of engineering, Master of Engineering and PhD from Andhra University. He is working as Associate Professor in the department of Electronics and Communication Engineering, Vignan’s Institute of Information Technology, and he is the DST SERB Young Scientist Awardee. He has presented many technical papers in national and international conferences and published many journal papers in reputed journals. His research interests include Array Antennas, EMI/EMC, Communications, Field Theory and Instrumentation

Madhusudan Donga obtained his B.Tech. Degree from Bonam Venkata Chalamaih Institute of Technology And Science, Batlapalem affiliated to JNTU Kakinada, East Godavari District, Andhra Pradesh, India in the year 2009. M.Tech from Vignan‟s Institute of Information and Technology, Visakhapatnam, affiliated to JNTU Kakinada, India. Presently he is working as an Assistant, Professor in the department of Electronics and Communication Engineering, Vignan's Institute of Information Technology, Visakhapatnam. He has published 8 paper in International Journals and conferences. He is interested in the fields of Antenna, Optimization techniques, wireless communication, signal processing Image and video processing

V.Venkatesh has done his B.Tech in Electronics & Communication Engineering from Gudlavaleeru Engineering College and is now pursuing M.Tech at College of Engineering, Andhra University. His area of interest includes design of high performance microprocessors.