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Multi-Core Eight Bit Ternary Content-Addressable Memory Design Based Image Learning System

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Abstract*: In this research work, the image is learned to find features to make use of during its analysis and a genetic apices based low power Ternary Content-Addressable Memory (TCAM) is designed to implement the proposed image learning system. A technique called Content Matching Search Register is proposed in this work to perform the image learning operations in proposed TCAM architecture. This paper proposes an ImOFF algorithm for image analysis. The focus of this multi-core TCAM (MC-TCAM) is to make fast computations and search based designs. The focus application of this research work is in the design of low power On-board Embedded-VLSI chip to perform image analysis. Proposed multi-core eight bit Ternary TCAM (MCEB-TCAM) is analyzed using IC design tools in 90nm technology, using Verilog hardware description language and usage of Cadence for layout generation and parasitic extraction of the circuit components.

Keywords* : Feature learning, TCAM, Image Analysis, Cadence, pixels.

I. INTRODUCTION

With the increasing complexity in image projection [1] [2] [15] a vast variety of analysis methods and approaches have emerged. Recent advances in image analysis provide high resolution images of the texture structure, so that accurate image illusion model representations can be practically measured. Requires image-based illusion analysis, providing valuable information for projection and representation during image rendering problems, to avoid image benchmarks for both projection - orientation and localization of the image object of interest. A shape reference descriptor, which minimized the coefficient assignment problem, but did not take into account neighborhood points. Under several schemes, a different projection setting was used to solve the matching problem, to detect shapes in the projected images, to improve the corresponding recovery of the projected image. They are used to project image data into a constraint processing, providing an open-ended problems under sequential approximations.

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CAMs [3-5] were designed based on a broad under two categories : first only for search function and second write function with search function. In contrast to these two functions, these days CAMs were predominantly used in parallel processor, to perform various types of parallel data processing with words and addresses. In proposed EB-CAM, this makes an importance to create a compact, highly parallel processing system that requires high levels of performance.

II. PROPOSED METHODOLOGY

A TCAM [7] [8] has three modes of operation, namely : Read, Write and Compare. Since TCAM has a compare operation feature, it performs this feature in two parts : storage and a comparison . By comparing the input data in memory within a single clock cycle predicts the performance and efficiency of a TCAM, resulting in better search time comparatively with the other memory search algorithms. On this contrast, a TCAM which has a feature of high clock levels of performance to achieve high bit or word content searching is proposed in work.

Set of rules to be followed in solving the TCAM design problems are:

a. The size of the design is with 90nm scaling, which reduces the parasitic losses.
b. The parallelism is 8 bit level, to improve the performance of Read Write Cycle Operations.
c. The power is reduced through genetic apices method, extracting the minimum power utilized at each section of design and that power is maintained as a stable power through-out the design.

A. Content Matching Search Register

By giving new data through shift address register Content (In) Search Address Register at each clock cycle, a valid Content (Out) Search Address Register result output for each clock cycle. Each bit location in the shift address register is connected to all the matching cells in the corresponding row wise column distributor as indicated by horizontal lines. Until the Match_Ack goes high, output Content (Out) Search Address Register of the Content Encode Register is not updated.

During a low Clock_Enable operation (shift data in Content Matching Search Register), there should be no shifts in Content (In) Search Address Register and the Search_Enable and Match_Ack should be low.

This will ensure that the outputs of all words are kept inactive.

During a high Clock_Enable operation (match data in Content Matching Search Register), MCEB-TCAM during the first clock of Clock_Enable, bit-by-bit the content data is loaded into Content (In) Search Address Register, during the second clock of Clock_Enable, Search_Enable is enabled to initiate the readwrite technique to search the content for predicting the matched_content or not_matched content, during the third clock of Clock_Enable, Match_Ack goes high then the output of Content (Out) Search Address Register is updated and during the third clock of Clock_Enable, Match_Ack goes high, contents with Content (In) Address Register will be verified for matching with Content Encode Register Address, then the output of Content (Out) Match Address Register will be verified with Match_Lines and Not Match_Lines lines.

And during the successive clocks using readwrite circle (RW_C) circuit the readwrite technique will continue Content to perform faster content searching process.

CMOS based TCAM [9] are having low scaling capacity, performance degradation as data size increases, longer switching times and inefficient in terms of cost or power [10]. With proposed approach of design, TCAM can perform fastest [11] [13] content packet scanning against the sophisticated content patterns.

Now, provide an insight to proposed approach,

a) Highest match result
b) Low power consumption
c) High level of Contentism
d) High Efficiency

B. Operation of Multi Core Eight Bit TCAM architecture

Search_Content() in real time operation contains multiple content, need multi-cycle operation proportional to MCEB-TCAM locations. Compare to conventional TCAMs implementation [12] [14], MCEB-TCAM performs the comparison Content using multiple memory locations, using only one Content Encode Register by increasing the speed of comparison for Match_Valid() for MTrue() and MFalse(). Proposed MCEB-TCAM VLSI Design Architecture Implementation accomplish eight stages of Contentism.

Stage 1: uses single memory location in Content Encode Register to compare each single bit memory block location.

Stage 2: uses a memory Content comparisons, to initiate the MTrue() and MFalse() acknowledgment with an integer match valid S-status of Match_Valid(). In this stage the value of S is 1, corresponding to two Content and results in MCEB-TCAM of Search_Content() two-bit comparisons.

Stage 3: approach will enable the eight-bit content search bus for the MCEB-TCAM memory blocks. Each memory block will be decoded by eight-bit content search status register bits.

Stage 4: uses a eight bit write operation in eight-bit encoder operations, to perform 64 bits read operation. This stage reduces the clock utilizations and improves the clock performance.

Stage 5: performs Content memory comparisons between 64 bit Search_Content() with 64 it MCEB-TCAM address locations simultaneously in eight clock cycles only.

Stage 6: combines 64 bits in Content way with 8 64 bits, combined with the Content Encode Register with the minimum Content search of 512 bit content search in eight clock cycles only

Stage 7: gives an 512X512 Content content search performance increasing the clock performance by utilizing 16 clock cycle only.

Stage 8: performs the logical ORed operation of proposed standard multi-cycle MCEB-TCAM operation implementation.

For eight cycles operation, as shown in figure 1, the process is

Process 1: During the multipleMatch_Operation(), search of MCEB-TCAM for multi-cycle match to an input Search_Content() is performed by simply searching sequentially through all the memory locations i.e., reading the Search_Content(), comparing the Search_Content() and Enable() is performed to Data_Read() a valid MTrue() for mulipleMatch_Operation(). In this operation, MTrue() and Match_Valid() is asserted.

Process 2: If no MTrue() is found, Match_Valid() is not asserted, but Match_Valid() is asserted for all the addresses compared in the search operation. Match_Valid() indicates the read cycle completion.

Process 3: During the multipleMatch_Operation(), considering multiple MCEB-TCAM content locations, the output of Single Bit MCEB-TCAM architecture is indicated by single bit operation MCEB-TCAM, resulting in either 1-bit match or 0-bit match, using one-bit Content encode register at each MCEB-TCAM location. Content Encode Register stores the content of match validation, each Match_Valid() with MTrue() stores a 1-bit eight-bit register and each Match_Valid() with MFalse() stores a 0-bit eight-bit register. The storage single-bit eight-bit register is a distributed register, for multipleMatch_Operation(), all the MTrue() and MFalse() results will be logical ORed to result Search_Content() MCEB-TCAM single-bit operation.

Process 4: Match_Valid() will indicate the assertion of MTrue() and MFalse() to content address matching during search operation and results to status of Match_Operation() and NonMatch_Operation(). When Search_Content() match is found, performs Match_Operation(), resulting into validation Match_Valid(), indicating MTrue() with Match acknowledgement.

A block diagram of Proposed MCEB-TCAM Design is shown in figure 2. Single Cell content and is used to perform the cumulative eight bit comparison of eight bit cells implemented as shown in Proposed MCEB-TCAM Design. MCEB-TCAM consists of 64K word x 288-b memory call array including an address decoder, a Content encoder, registers, I/O buffers, and control circuits for external circuits. A Search_Enable signal is used to use an automatic content search refreshing operation in MCEB-TCAM. A Content Search Register is used to decode the Content Match, Address Match and Match Status signals.

Each of 2048 MCEB-TCAM cells consist of 16 memory cells which to store the content label and match bits. The Search_Content() is applied is compared with every bit stored in the MCEB-TCAM cell, if match bit='1', then MCEB-TCAM will perform the Content_Comparison operation with stored value in MCEB-TCAM cells.

A Match_X is performed by looking at the Bit and select lines of MCEB-TCAM. If the data mis-matches with the contents of MCEB-TCAM cell and the Match_X is pulled low, the stored match bit becomes '1'.

In other conditions, the stored match bit becomes '0' for data matching with the content of MCEB-TCAM cell and by making Match_X is pulled to high.

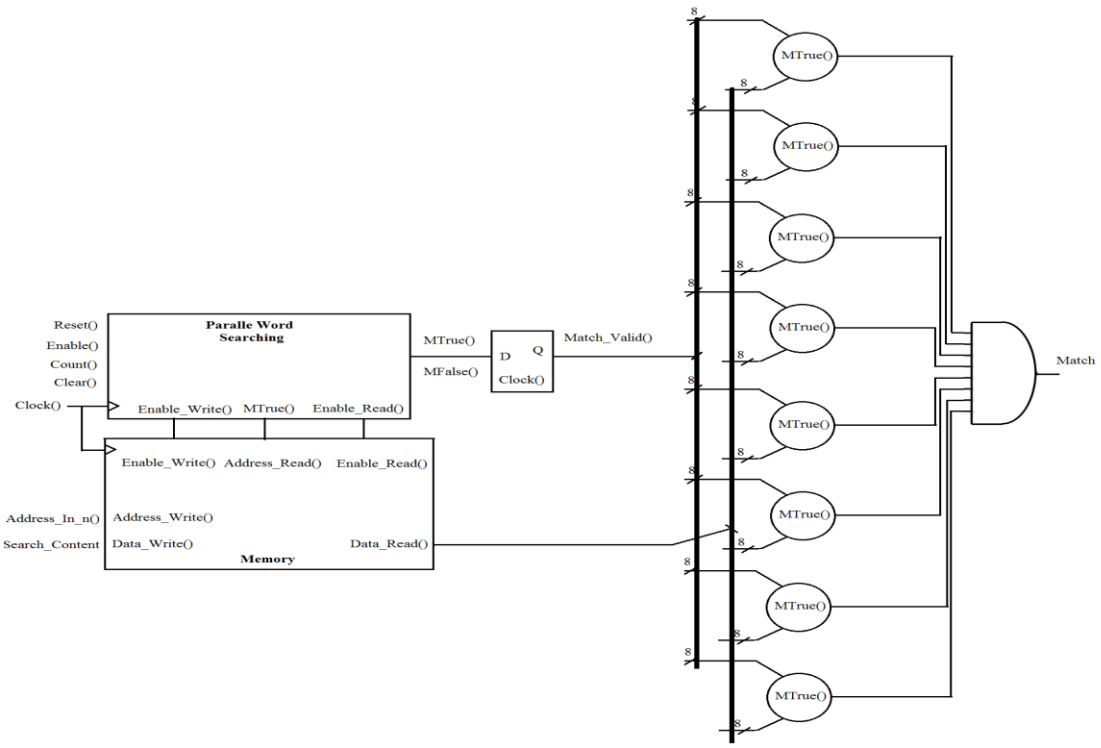

Fig. 1. MC Eight Bit TCAM Architecture

III. RESULTS AND DISCUSSIONS

MCEB-TCAM is designed and simulated using IC design tools in 90nm technology. After designing MCEB-TCAM at the architectural level, behavioral and functional verifications will be done using the Verilog hardware description language, with layout generation and parasitic extraction of the circuit components of all proposed MCEB-TCAM using Cadence are shown in table 1 and 2.

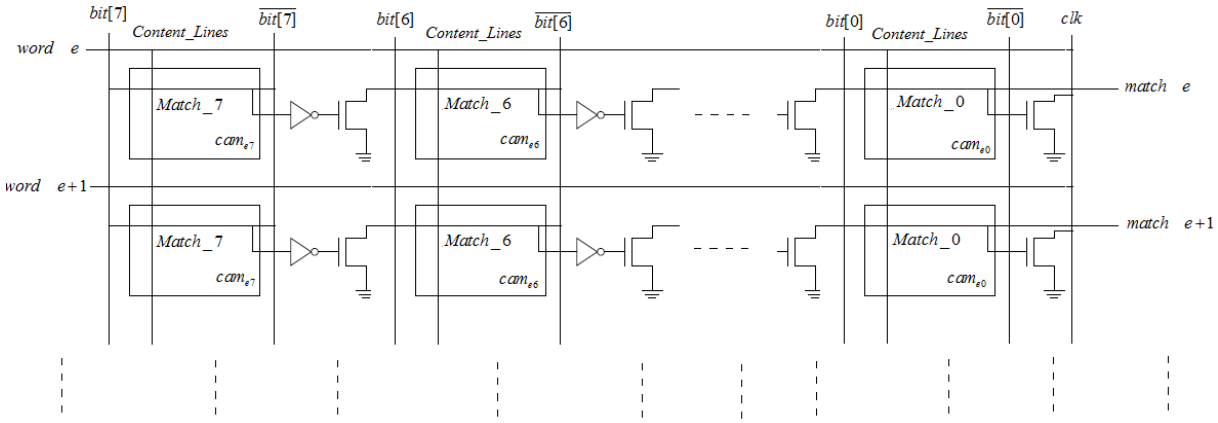

Fig. 2. Proposed MC Eight Bit TCAM design using Dual-TCAM blocks

Table 1: MCEB-TCAM (8192-bit) Performance Statistics

	Design		Implementation	Performance	
	Combinational Modules	Sequential Modules	Device (%)	Max. Frequency (MHz)	Min. Cycle (ns)
512x8 Distributed RAM	2158	2017	50	170	15.5(Write) 16.3(Read)
1024x8 Distributed RAM	5139	4421	98	210	19.9(Write) 817(Read)
2048x8 Distributed RAM	10589	8125	197	291	29.6(Write) 1,150(Read)

Table 2 : MCEB-TCAM (8192-bit) Design Statistics

	Power Consumption (For 2.5 ns search time)								
	V_{bias}	V_{ML}	I_{ML}	Current Source Enabled Time	Voltage difference between ML_H and ML_L	I_{ML} drop-off	%Q (full match & miss match)	% Speed(full match & miss match)	% Energy/ Search
512x8 Distributed RAM	0-0.6V	0.04V	2µA	1.2ns	295 mV	2.3ns	65	51	65
1024x8 Distributed RAM	0-0.6V	0.40V	17.8 µA	2.4 ns	391 mV	18.4 ns	91	81	91
2048x8 Distributed RAM	0-0.6V	0.87 V	77.4 µA	2.8 ns	498 mV	79.8 ns	92	95	93

IV. CONCLUSIONS

In this research work, MCEB-TCAM is designed and simulated using IC design tools in 90nm technology. After designing MCEB-TCAM at the architectural level, behavioural and functional verifications is made using the Verilog hardware description language of proposed MCEB-TCAM using Cadence is made.

In the proposed Search Register method, at the block level all the pixel values of image are analyzed and bit level extraction is performed. At the design level, the image of 8 bits are applied through genetic apices to extract the maximum number of features values to learn the system. At the simulation level, the learned features are tested with the images, to identify the features to be allocated to those tested images. The proposed MCEB-TCAM design allocates a variable bias voltage power for image feature search based on content matching and the number of mismatched bits are analyzed. In content matching, search and TCAM model operations utilizes very less power of total 0.2 bias voltage, for a power reduction to improve the clock speed performance. The suggested MCEB-TCAM design can be implemented in a 256K word x 576-b MCEB-TCAM for a 90nm 1.2-V CMOS logic process, for a 3.5 ns search time on 8Mbit MCEB-TCAM word, the proposed design utilizes minimum 50% less power comparatively with other distributed RAM's

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