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Design of a Linear Voltage to Frequency Converter for Digital Audio Applications

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Abstract*: Voltage to frequency converters are used in various types of analog to digital converters in suitable digital audio applications. One of the applications is the Audio Interface which has been considered. The Voltage to frequency converter (VFC) thus plays a major role in the analog to digital conversion. This paper proposes a low power VFC designed in 0.18 µm technology which in turn is used to design a low cost and a high-resolution analog to digital converter (ADC). The analog signal is given to the V-F converter and the VFC output is given to the frequency counter using a suitable link. This counter gives the digital output. The design is implemented in PSoC and the performance is analysed with the previous technologies. Parameters such as sensitivity, output frequency and power consumption are analysed. This V-F converter and ADC are used in the digital audio interface which is used for audio applications. With the proposed VFC and ADC, the interface produced a good SNR compared to the conventional audio interfaces.

Keywords: low power VFC, frequency counter, PSoC

I.INTRODUCTION

Today's integrated circuit industry provides a wide array of devices which allow the conversion of a quantity from one domain to another. Conversion of voltage to frequency is a technique of data acquisition commonly used in synchrotron radiation and other research applications analog signals to be correctly implemented over well-defined time periods coordinated with photon counting detectors. Conversion between voltage and frequency is a common requirement in areas such as in the remote sensing of a quantity (temperature, pressure, and level), digital voltmeters and most radio frequency (RF) applications. A V-F converter acts as an oscillator circuit. The frequency of this converter is linearly proportionate to its control voltage. In this correspondence, we could consult a unique voltage to frequency converter that could achieve extremely good linearity between both the input voltage and the oscillator frequency. This converter's linearity could be enhanced by altering the op-Amp connected variable resistor [1],[2].

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The two commonly used VFC architectures are: the VFC multivibrator current and the VFC load balanced [3]. The VFC can be made in synchronous or asynchronous forms. Such upgrade was accomplished by introducing a control circuit to standard converters for voltage-to-frequency.

From the experimental data, such converter's linearity was roughly 0.15% at 1 MHz level. In wireless communication networks, high sampling speed (1–3 GS / s) analog to digital converters (ADCs) with medium range (5–10 bits) are used. [4], [5]. It is important to design energy-efficient wideband ADCs, notably from battery-powered portable systems. Flash ADCs have been traditionally used for fast conversion of analog to digital signals. [6–8].

Another issue is the comparator input offset voltage in a flash type ADC, that causes non-linearity mistakes that get worse with higher resolutions. A common method of increasing the input-referred offset is to deal with analog mixer preamplifiers in individual comparators [9]. As an alternative to low power design, there are many offset correction methods to eliminate offset errors in comparators[10]. Interpolating and folding designs have been implemented to overcome most of the flash ADC's key drawbacks, including large power consumption and a wide format area[11]. Furthermore, interpolation benefits from its enhanced linearity due to the error average and distribution[12].Every two-step ADC is equivalent to an ADC sub-range which requires a gain stage to boost the residual voltage before this is applied to the good ADC[13]. The 1.5-bit pipeline phase in each step could greatly ease the comparator offset requirement[14]. Based on the perceptron and manufacturing technology, the SAR ADCs could accomplish a broad series of features as stand-alone ADCs, including ultra-low power[15,16], a TI-ADC would always be lower energy-efficient than any of its sub-ADCs due to the overhead power connected with interweaving[17].

Digital audio systems allow high-resolution analog-to-digital converters (ADCs) and linearity modulation offers an effective signal conversion process for achieving high resolution without the need for high-precision analog building blocks. 18],[19] Nowadays, voice recognition is becoming very common, with apps constantly heeding and waiting for handler commands. In fact, technologies, like the cancelation of ambience noise, need additional than one microphone per unit, increasing the demand for low-power low-cost electronic circuit even more.

Multimedia microphones has some benefits over analog mics (e.g., improved rejection of power supply), and the pattern shows that they could gain attention in the approaching future [20].

A traditional electronic microphone comprises of an analogue microphone attached to an analog to digital (ADC) portable low-power converter. The high audible audio frequency (16-18 kHz) promotes the need for interpolated converters like sigma–delta modulators [21],[22].

For this sort of converter, a standard sampling frequency is in between several hundred kilohertz and a several megahertz, which causes themselves to be fifth and higher [23],[24] even when the quantizer is a single bit. Innovative protocols, like the MIPI SoundWire, are now proposing the need for higher data rate increases to a several hundreds of megahertz, that could allow low-order converters to be used [25].

This paper deals with the mixing up of a synchronous VFC and a frequency counter to function like an ADC. This ADC was made use in a digital audio interface and performance analysis was done with impedance and SNR as the parameters. The performance of the SVFC was also done with sensitivity, linearity as the parameters. The proposed SVFC in turn an ADC was versatile and had high resolution and was very suitable in quantizing audio signals. In section II the design of voltage to frequency is elaborated giving an idea of other VFC architectures as well. Section III deals with the ADC which makes use of a SVFC and a frequency counter. In both these sections the PSoC implementation were done. Section IV describes the use of the proposed SVFC in turn an ADC in a digital audio interface. ADC plays an important role in the function of an audio interface. Section V gives a clear picture on the results and discussions. The outputs of the SVFC and ADC is shown with a comparison to the conventional techniques and found to have a reasonably good performance. The SVFC scheme is simple, low cost and the resolution is high which has an effect on ADC and the audio interface. Section VI summarizes the research work and the future scope is also discussed.

II. VOLTAGE TO FREQUENCY CONVERSION

The various methods of voltage to frequency conversion and its applications were studied in the previous section. The simplest form of a VFC consists of a voltage to current converter, a current integrator and then an oscillator or a control for some applications. It is designed with the basis of charge – balance method. The voltage input is converted in to current first and then altered in to pulses by means of a current integrator and an oscillator or a control circuit. The block diagram of this VFC is shown in Fig 1.

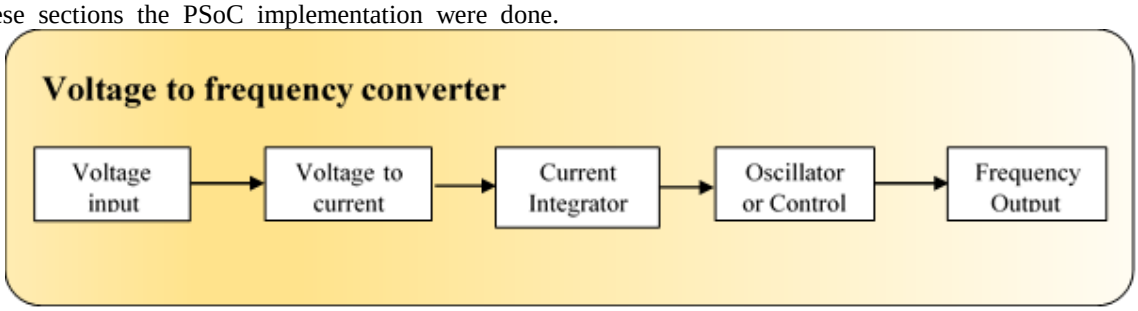

Fig. 1: General block diagram of a VFC

The input voltage is mostly taken from a sensor or a transducer. To convert this sensor input voltage into output current, a voltage to current converter that is built on a wideband PLL that has an adaptive frequency response or a switched – capacitor current source attached with a DDA can be used. To convert the current into frequency, a control or a reduction oscillator is required. This reduction oscillator uses a self-chopped assembly that is analogous to a RC oscillator with comparator offset dissolution. This lessens the channel length modulation consequence owing to the high input common mode difference among the dual input ports.

There are many other types of VFCs namely the comparator-based V-F converter, Integrator based V-F converter, Synchronous VFC, Schmitt trigger based VFC, VFC using CMOS technology and so on. In all these types linearity remains the prime concern. The linearity guaranteed by TC9402 CMOS VFC is 0.25 %.

A. VFC Architectures:

There most frequently used VFC architectures are: the charge-balance VFC and the current- steering multivibrator V-F converter. The charge-balanced V-F converter might be done in synchronous (clocked) or asynchronous or arrangements. The various other variable frequency oscillator (VFO) designs, includes the global 555 timers, nevertheless the significant characteristic of V-F converter is linearity.

Real-world VFCs of the current – steering multivibrator sort have linearity about 14-bits and reasonable stability, though they might be used in analog to digital converters with high resolutions deprived of losing codes. A performance threshold is established by the comparator peak noise, dielectric absorption (DA), highest temperature coefficient, and the steadiness of capacitor, that is normally a discrete module. The voltage/comparator reference construction is an added depiction of the role done preferred to authentic circuit used, that is copious more collective through the switching and congruently tougher towards analyse. This type V-F converter is modest, low powered besides inexpensive, and utmost perform since a widespread variety of source voltages. They remain perfectly suitable for inexpensive and an average accuracy (12 bit) ADC in addition to communication propositions.

The charge balanced V-F converter was little complex, all the more challenging in its supply current and voltage requirements, and more precise. It is proficient enough to have 16-bit to 18-bit linearity. At low frequencies, boundaries on the functionality of this charge balance V-F converter are established by the steadiness of the source of current and the timing of monostable (that relies on the capacitor, among other V-F converters). The temperature steadiness of the integration capacitor in op-amp and the absolute value do not disturb the accurateness, though its seepage in addition to dielectric absorption (DA) affects it.

By higher frequencies, the second-degree effects, like the switching transient along the integrator besides the correctness of monostable although that is retriggered later at the end of a pulse click, with accuracy and linearity.

The stability and momentary behaviour of the precise monostable produce more hitches, nevertheless the problem might be evaded by substituting the monostable multivibrator by a bi-stable multivibrator with a clock. This structure is commonly recognized as synchronous V-F converter or termed as SVFC. The difference compared to the preceding methods is very small, but then again, the pulse of the charge balance is now definite with two sequential peaks of peripheral clock. When the clock has little jitter, then its charge would be precisely distinct. The pulse output would similarly synchronize with the clock. This SVFC form is proficient to an extent of 18-bit linearity and incomparable temperature reliability. The behaviour of this design is appropriate with various applications, because the transfer of synchronous data is always smoother to deal with compared to the asynchronous mode. Nevertheless, the output of a synchronous VFC is an impure tone with added harmonics, but contains some components that are harmonically associated to the clock frequency. The schematic of a synchronous VFC is shown in Fig 2.

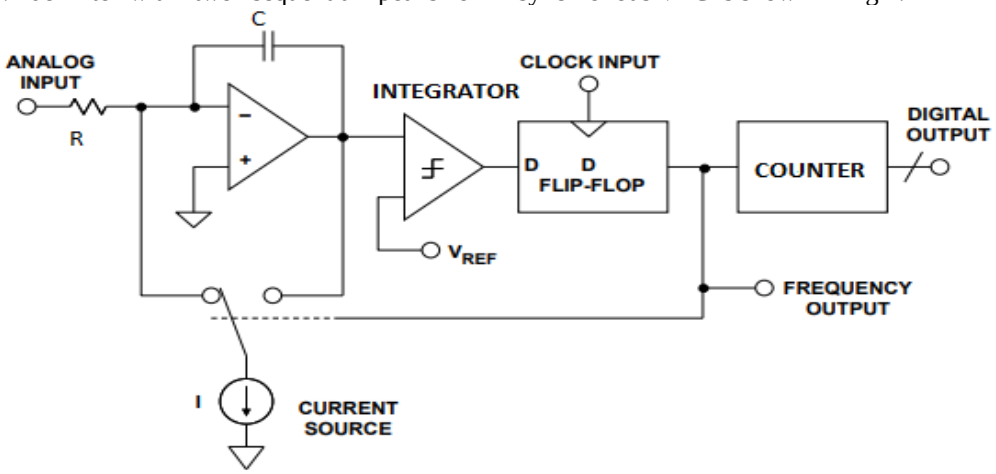

Fig. 2: Synchronous VFC (SVFC)

It is obvious that the Synchronous V-F converter is quantized, while the conventional V-F converters are not quantized. This does not shadow from the effect which the counter – VFC - ADC has more firmness (non-linearities neglected) compared to the counter-SVFC ADC, since the clock in the counter also targets a boundary to the resolution. VFCs have a number of applications than as a module in ADCs. Because of the reason that their output is a pulse train or a square wave, it could be directed on a wider range of communication media (radio, PSN, ultrasonic, IR, optical, etc.) without no trouble. This requirement may not be established by a counter, but with other V-F converter that are organized in place of a frequency to voltage converter (FVC). This stretches an analog output, besides a reasonable VFC-FVC grouping remains a same convenient means of transferring a precise analog signal transversely a separation blockade.

B. PSoC implementation of V-F converter:

PSoC tool belongs to second-generation design environment that is used for design, mend and plug-in the PSoC 5 devices. The design environment is combined with a graphical editor to generate an influential hardware/software design atmosphere. PSoC platform comprises of dual elementary structural slabs. The plug-in which permits the handler to choose, constitute as well as link the prevailing circuits in to the IC and the gears are the correspondent of layers on the microcontroller unit. The PSoC implementation of the SVFC is depicted in Figure 3

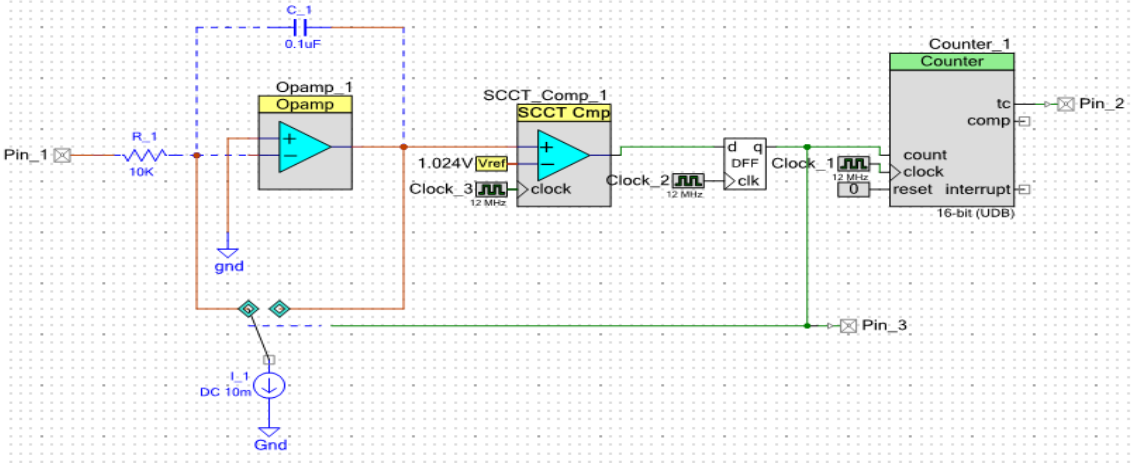

Fig. 3: PSoC implementation of the SVFC

III.ANALOG TO DIGITAL CONVERTER

Analog to digital converter is one that converts an analog signal, such as a sound picked from a microphone into a digital signal. The analog signal is first sampled and converted to a discrete signal and then quantized and encoded to obtain the digital signal. ADC (Analog to digital converter) is used in a number of audio applications like music recording, digital audio workstations, sound processing, audio streaming and so on. Music is often produced on computers using analog recording devices and therefore require an ADC to generate the PCM (pulse-code modulation) data streams that are sent to the compact discs and other digital music storage files. This section deals with the ADC designed based on a synchronous VFC that is suitable for digital audio applications. This ADC scheme has many advantages such as high accuracy, comparatively low power consumption, wide dynamic range, high stability and quicker conversion time when compared with the existing VFC-based techniques. The block of a general ADC is depicted in Figure 4. The importance of ADC is depicted in the figure. The processing of digital signals much easier compared to analog signal processing which was done earlier.

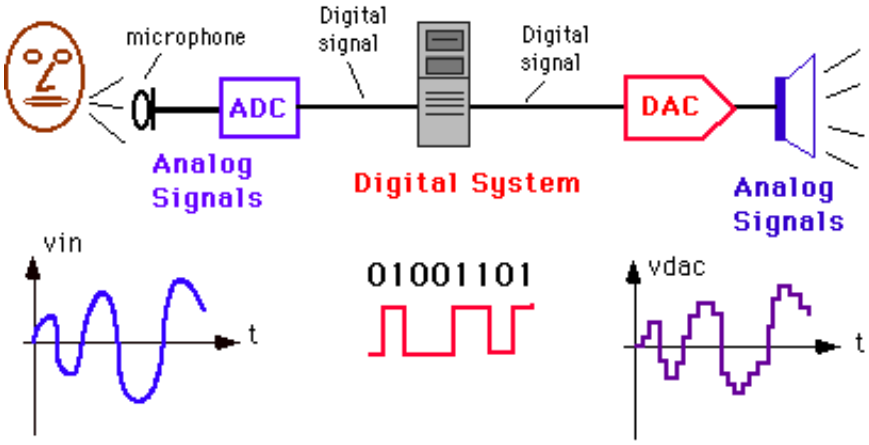

Fig. 4: General block diagram of ADC

A. Synchronous VFC in ADC

Analog audio to Digital audio conversion is comprehended using a modest and low-cost technique grounded on a V-F converter. The output of a V-F converter is a digital pulse or a square wave whose recurrence degree is proportionate to voltage of analog input signal. The digital circuit that follows the V-F converter counts the period of the output signal. A binary counter tallies the pulses of clock having a frequency considerably high than the V-F converter frequency. The time require to translate an analog input signal in to a digital word is correlated to the maximum full-scale frequency of the V-F converter and the required resolution of the measurement. The block diagrm of the ADC using SVFC for an audio application is depicted in Figure 5.

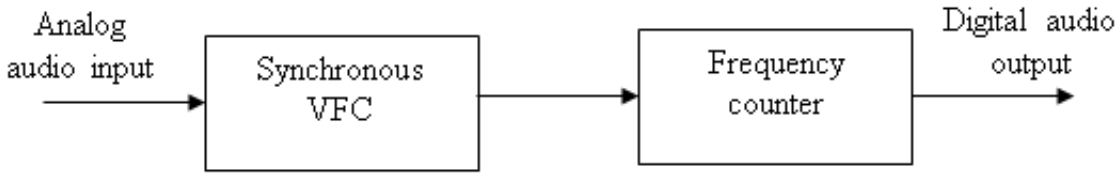

Fig. 5: Block diagram of an ADC using SVFC

The important aspects of an ADC are sampling, quantization and encoding. The quantization plays a major role in digital audio applications especially in a MIDI and audio interface. As seen in the above figure, the ADC makes use of a synchronous voltage to frequency converter. This synchronous VFC is responsible for the quantization part of the proposed ADC. The resolution is very high but there was a little trade-off in linearity. Now, this ADC is versatile, low cost and has a high resolution.

B. PSoC implementation of an ADC

Gears used in the design of SVFC - ADC includes IDAC, PWM, Comparator, Counter, LCD Display and UART in case of interfacing.

The current customed down by the IDAC initially controls the exterior capacitor connected linearly till a brink voltage value stays grasped. The frequency output is reliant upon the worth of capacitance and an altering current. Intended for measurements, a Pulse Width Modulator (PWM) with an immobile phase will permitt a 16-bit counter. This yield by the comparator times the counter. The counter value is received then directed to UART for communicating the signals to the system. The PSoC representation of a SVFC – ADC is represented in Figure 6. The next section deals with the application of ADC in a digital audio interface.

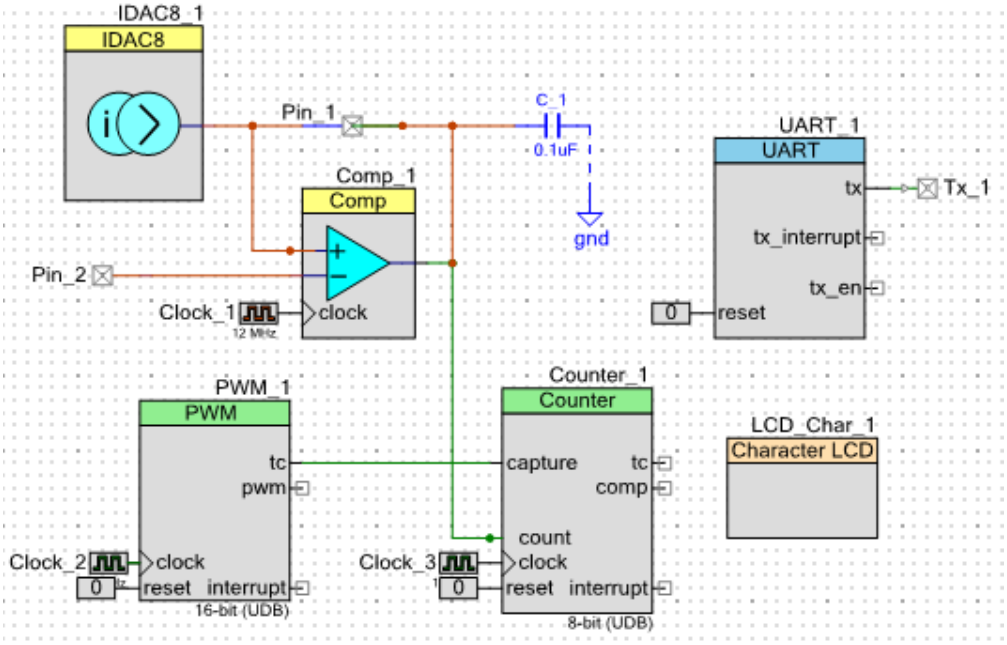

Fig. 6: PSoC implementation of SVFC - ADC

IV.SVFC – ADC IN AUDIO INTERFACE

An audio interface is a hardware equipment that connects the microphones and further audio inputs to the computer or any system. A distinctive audio interface translates analog audio into the digital audio data that the computer could process. It sends the digital audio to the computer through different means of connection (e.g. USB, Thunderbolt, FireWire, or a special PCIe/PCI card). The same audio interface likewise performs the same procedure in inverse, getting digital audio data from the computer and translating it into an analog signal which can be heard through the headphones or studio monitors. Most of the audio interfaces comprise of the line-level analogue inputs and outputs, few microphone mixers or preamplifiers, and might also include digital inputs and digital outputs such as AES and S/PDIF or Alesis digital audio tape (Lightpipe).

It is evident that the important modules of the audio interface are ADC and DAC. The block of an audio interface is depicted in Figure 7. The analog audio input is given to an audio mixer and then amplified if required. The signal from the amplifier is sent to the ADC to get the digital audio. The digital audio is now sent to the signal processing section of the interface where the audio is processed. It is decoded and sent to the DAC to get the analog audio. This analog audio is amplified again and sent to the speaker.

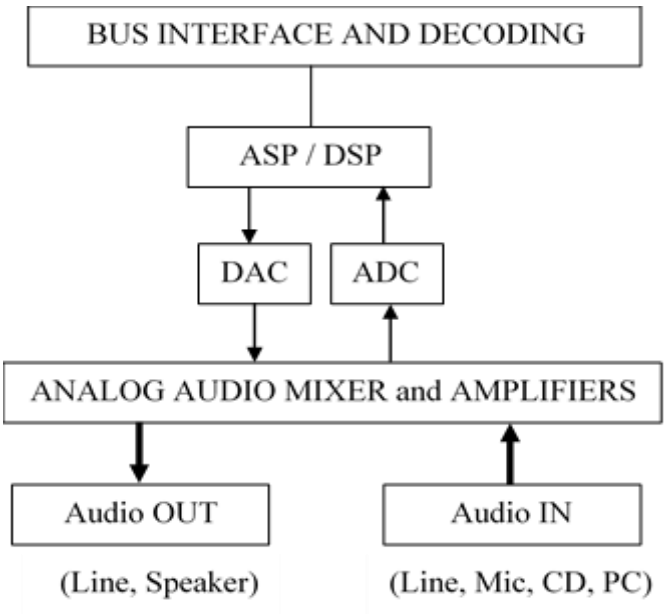

Fig. 7: Block diagram of an Audio Interface Module

V. RESULTS AND DISCUSSIONS

A. Synchronous VFC

The frequency measurements are the count of the increasing edges which arise in a period of one second. This paper makes use of a Pulse Width Modulator to produce the time space window. The analog signal for which the frequency has to be estimated is directed as the input to the counter. Thus the counts in the binary counter limited to a time space window provides the equivalent count to the frequency of the input analog signal. The intended frequency stands exhibited on the display to the computer through an interface. The transfer characteristics of volts vs counts is depicted in Figure 8. The figure shows that it had a linear characteristic throughout its period.

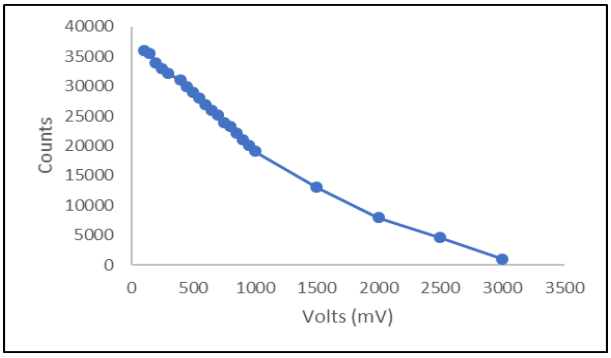

Fig 8: Transfer Characteristics of Volts vs Count

B. SVFC – ADC

In this technique, the voltage as on the editable voltage source was directed as input of an op-amp comparator. As the output of the op-amp comparator goes high, the IDAC output was linked to the pin. Whereas, as the op-amp output indicated low, the pin was shorted to ground. The current source to the circuit was configured through IDAC. IDAC charged the capacitor connected externally. As the capacitor voltage moves beyond the input voltage Vin, the output of the op-amp becomes low which consequently discharged the capacitor. When the capacitor voltage marked zero, output of the op-amp indicated high, thus IDAC charged the external capacitor again. This cycle lingers. The oscillator frequency, which is inversely proportional to input voltage was obtained. The time duration of the output waveform was directly proportionate with the analog input. The output frequency was initiated through the relation: $F = \frac{1}{\frac{C-V}{I} + t_d}$

Where: F- Output Frequency
C- Capacitor
V-Input voltage
I-IDAC current
t_d – Period of the Comparator's Synch clock

Figure 9 and Figure 10 shows the readings of the analog to digital converter for two different voltage ranges. The first one is a 0-3.3 V DAC range and the next is a 0 – 1.2 V DAC range. Linearity is obtained in both the cases because of the presence of a synchronous V-F converter.

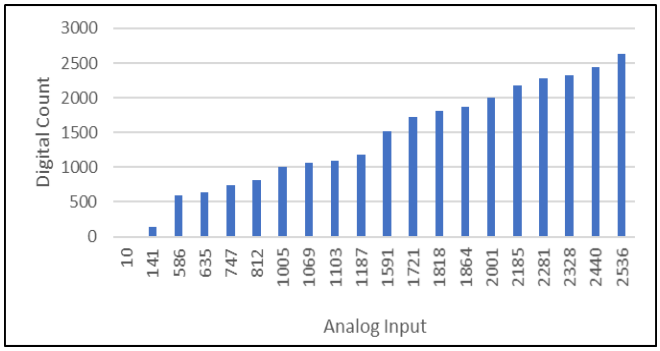

Fig 9: ADC Output readings for 0 – 3.3V DAC range

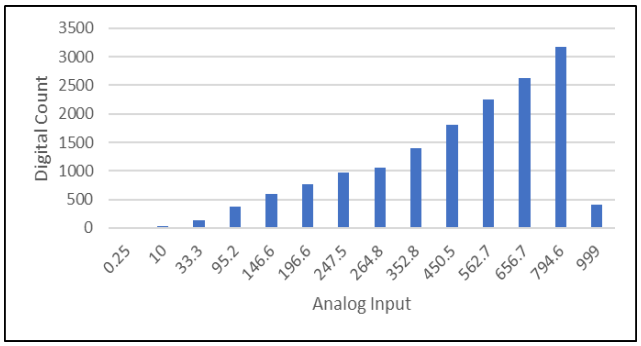

Fig 10: ADC Output readings for 0 – 1.2V DAC range

C. SVFC – ADC IN an AUDIO INTERFACE

The characteristics of the synchronous V-F converter and the SVFC-ADC was used in the design of an audio interface where ADC played a major role. The linearity in the designed V-F converter created a great impact in the quality of the audio coming out as output. This design was validated through subjective evaluation by audio experts from the commercial audio engineers and the audio researchers. Parameters like the gain, latency and the overall clarity of the audio were checked. The table 1 given below shows the results of the subjective evaluation for the proposed design. This design was compared with the conventional audio interfaces. The SNR was calculated for the proposed design and found to be 52 dB which was much better compared with the conventional audio interfaces.

Table 1: Subjective evaluation results

Parameters	User 1	User 2	User 3
Gain	High	High	Low
Latency	Low	Low	Low
Clarity	High	High	High

VI. CONCLUSION

This paper dealt with the design of a synchronous V-F converter and in turn an VFC-ADC which was used in the audio interface. Linearity was a major factor used and the proposed audio interface showed good results compared to the conventional interfaces. The outputs of the V-F converter and the SVFC-ADC were also depicted individually. The future scope of this research could be the design of a digital to analog converter using the SVFC-ADC so that the entire interface can be designed with good linearity.

REFERENCES

1. Y. H. Leow, H. Tang, Z. C. Sun, and L. Siek, "A 1 V 103 dB 3rd-orderaudio continuous-time ADC with enhanced noise shaping in 65 nmCMOS,"IEEE J. Solid-State Circuits, vol. 51, no. 11, pp. 2625–2638,Nov. 2016.
2. K.Taniguchi, "A design of the voltage-to-frequency converter," Trans. Inst. Elect. Commun. Eng. (Japan), vol. 57, pp. 597-599, Oct.1974.
3. John L. Lindesmith, "Voltage-to-Digital Measuring Circuit," U.S. Patent 2,835,868, filed September 16, 1952, issued May 20, 1958. (Voltage-to-frequency ADC).
4. Chung, Y.-H.;Wu, J.-T. A 16-mW 8-Bit 1-GS/s digital-subranging ADC in 55-nm CMOS. IEEE Trans. Very Large Scale Integr. Syst. **2015**, 23, 557–566. [CrossRef]
5. Ku, I.-N.; Xu, Z.; Kuan, Y.-C.; Wang, Y.-H.; Chang, M.-C.F. A 40-mW 7-bit 2.2-GS/s time-interleaved subranging CMOS ADC for low-power gigabit wireless communications. IEEE J. Solid-State Circuits **2012**, 47, 1854–1865. [CrossRef]
6. Pernillo, J.; Flynn, M.P. A 1.5-GS/s flash ADC with 57.7-dB SFDR and 6.4-bit ENOB in 90 nm digital CMOS. IEEE Trans. Circuits Syst. II Express Briefs **2011**, 58, 837–841. [CrossRef]
7. Chahardori, M.; Sharifkhani, M.; Sadughi, S. A 4-Bit, 1.6 GS/s low power flash ADC, based on offset calibration and segmentation. IEEE Trans. Circuits Syst. I Regul. Pap. **2013**, 60, 2285–2297.
8. Park, C.-J.; Onabajo, M.; Geddada, H.M.; Karsilayan, A.I.; Silva-Martinez, J. Efficient broadband current-mode adder-quantizer design for continuous-time sigma-delta modulators. IEEE Trans. Very Large Scale Integr. Syst.**2015**, 23, 1920–1930. [CrossRef]
9. Razavi, B. Principles of Data Conversion System Design; IEEE Press: Piscataway, NJ, USA, 1995
10. Nuzzo, P.; Nani, C.; Armiento, C.; Sangiovanni-Vincentelli, A.; Craninckx, J.; van der Plas, G. A 6-Bit 50-MS/s threshold configuring SAR ADC in 90-nm digital CMOS. IEEE Trans. Circuits Syst. I Regul. Pap. **2012**, 59, 80–92. [CrossRef]
11. Van de Grift, R.; Rutten, I.W.J.M.; van der Veen, M. An 8-bit video ADC incorporating folding and interpolation techniques. IEEE J. Solid-State Circuits **1987**, 22, 944–953. [CrossRef].
12. Kimura, H.; Matsuzawa, A.; Nakamura, T.; Sawada, S. A 10-b 300-MHz interpolated-parallel A/D converter, IEEE J. Solid-State Circuits **1993**, 28, 438–446. [CrossRef]
13. Doernberg, J.; Gray, P.R.; Hodges, D.A. A 10-bit 5-Msample/s CMOS two-step flash ADC. IEEE J. Solid-State Circuits **1989**, 24, 241–249. [CrossRef]
14. Zahrai, S.A.; Azhari, S.J. A 12b 100MS/s Highly Power Efficient Pipelined ADC for Communication Applications. Cyber J. J. Sel. Areas Microelectron. **2011**, 2, 1–7.
15. Zhang, D.; Bhide, A.; Alvandpour, A. A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13um CMOS for medical implant devices. IEEE J. Solid-State Circuits **2012**, 47, 1585–1593. [CrossRef]
16. Zhu, Z.; Liang, Y. A 0.6-V 38-nW 9.4-ENOB 20-kS/s SAR ADC in 0.18-_m CMOS for Medical Implant Devices. IEEE Trans. Circuits Syst. I Regul. Pap. **2015**, 62, 2167–2176. [CrossRef]
17. Stepanovic, D.; Nikolic, B. A 2.8 GS/s 44.6 mW time-interleaved ADC achieving 50.9 dB SNDR and 3 dB effective resolution bandwidth of 1.5 GHz in 65 nm CMOS. IEEE J. Solid-State Circuits **2013**, 48, 971–982.
18. Goette J, Jacomet M, Hager M. Using dither to improve the performance of lossy sigma–delta modulators. The Third IEEE International Workshop on Electronic Design, Test and Applications, 2006: 11
19. Yu J, Maloberti F. A low-power multi-bit. • modulator in 90-nm digital CMOS without DEM. IEEE J Solid-State Circuits, 2005, 40(12): 2428
20. E. Bachet al., "A 1.8 V true-differential 140 dB SPL full-scale standardCMOS MEMS digital microphone exhibiting 67 dB SNR," inIEEEInt. Solid-State Circuits Con
(ISSCC) Dig. Tech. Papers, Feb. 2017,pp. 166–167.
21. A. Sukumaran and S. Pavan, "Low power design techniques forsingle-bit audio continuous-time delta sigma ADCs using FIR feed-back,"IEEE J. Solid-State Circuits, vol. 49, no. 11, pp. 2515–2525,Nov. 2014.
22. C. D. Berti, P. Malcovati, L. Crespi, and A. Baschirotto, "A 106 dBa-weighted DR low-power continuous-time modulator forMEMS microphones,"IEEE J. Solid-State Circuits, vol. 51, no. 7,pp. 1607–1618, Jul. 2016.
23. C. D. Berti, P. Malcovati, L. Crespi, and A. Baschirotto, "A 106 dBa-weighted DR low-power continuous-time modulator forMEMS microphones,"IEEE J. Solid-State Circuits, vol. 51, no. 7,pp. 1607–1618, Jul. 2016.
24. Y. H. Leow, H. Tang, Z. C. Sun, and L. Siek, "A 1 V 103 dB 3rd-orderaudio continuous-time ADC with enhanced noise shaping in 65 nmCMOS,"IEEE J. Solid-State Circuits, vol. 51, no. 11, pp. 2625–2638,Nov. 2016.
25. T.C.Wang,Y.H.Lin,andC.C.Liu,"A0.022mm298.5 dB SNDRhybrid audio modulator with digital ELD compensation in 28 nmCMOS,"IEEE J. Solid-State Circuits, vol. 50, no. 11, pp. 2655–2664,Nov. 2015

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