Research on Power Efficient Clock Distribution Schemes for Switching Converters

S. Karunakaran, R RaniHemamalini

Abstract—Trends in VLSI technology represents bottleneck for the future high performance computing architectures as the ratio of the power pins to the total package pins keeps on increasing. A viable solution to this is bottleneck is to have final power consumption on-chip. Switched Capacitor DC-DC Converters are the most preferred for on-chip power conversion. However, as the number of power conversion modules increases and they get distributed across the chip area, clock distribution for the switched capacitor converters becomes a non-trivial task and the increased interconnect lengths cause clock degradation and power dissipation. This paper presents a power efficient signaling topology for driving the clocks to higher interconnect lengths.

Keywords—VLSI, switched capacitor converters, interconnects

I. INTRODUCTION

International Technology Roadmap for Semiconductors (ITRS, 2011) [1]mentions that more than half of the total package pins in high performance processors are utilized as power pins. This leaves less than half of the pins for signal interconnections. ITRS also predicts that the supply voltage for devices will decrease, however the supply current will increase. As the maximum current carried by each package pin is specified, the increased current will lead to increasing number of power pins.

A viable solution to decrease the number of power supply pins is implementing on-chip dc-dc converters. By implementation of the dc-dc converters in silicon, the input voltage will increase causing a decrease in the supply current and hence the number of package pins for the same power specification.On chip power conversion may furthermore be enabler for power distribution in multi-core processors with voltage regulation at individual cores.

However, with voltage regulation achieved at individual modules in case of complex integrated circuits, signal routing for the dc-dc converters becomes a critical task. Switched capacitor converters need clock signals for the switching of the MOSFETs. The clock distribution interconnect wires present an ever increasing energy budget along with their associated circuitries.[2-3] The power efficient schemes for clock signals for switched capacitor dc-dc converters. In continuation to the same, this paper presents two more schemes and compares the performance of all the four schemes. [4]

Differential signaling, extra reference voltages, multiple thresholds, multiple wire interconnects are the techniques reported in literature for tackling the interconnect effects [4], [5], [6]. Reduced voltage swing results in insufficient drive strength for larger loads. Literature reports use of using bootstrapping capacitors to improve the drive strength [7].For long interconnects the signaling schemes are differentiated based on the direction of swing reduction in the signal [4], [8]. Design topologies that do not require extra power nor does it need multiple threshold voltages is presented in [9]. But the design suffers from low drive strength and sensitivity to variations in supply voltage, process parameters and loading conditions [10].

II. TEST ARCHITECTURE

The test structure used in this article is shown in Fig 1. Every one of the circuits are broke down under indistinguishable stacking conditions, control supply and entryway source voltage. The test conditions are recorded in Table I.

The two circuits are mimicked with a yield load capacitance of 25fF. Interconnects are executed in M3 (metal-3) layer and are demonstrated by a π3 dispersed RC model (Rw=300ω/mm and Cw=230fF/mm) as appeared in Fig. 2.To model the fan-out, an extra capacitive heap of 250fF/mm length of wire is included as dispersed burden along the interconnect length.

TABLE I. CONDITIONS

Description	Notation	Range
Power Supply	V_{ddh}	1.0V
Gate Source Voltage	V_{gs}	0.54V
Loading Condition	C_L	250fF/mm
	C_{Lout}	250Ff

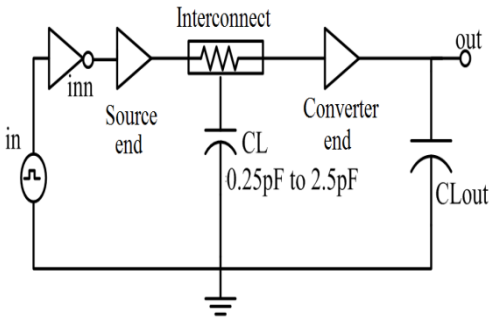

Fig. 1. Test architecture

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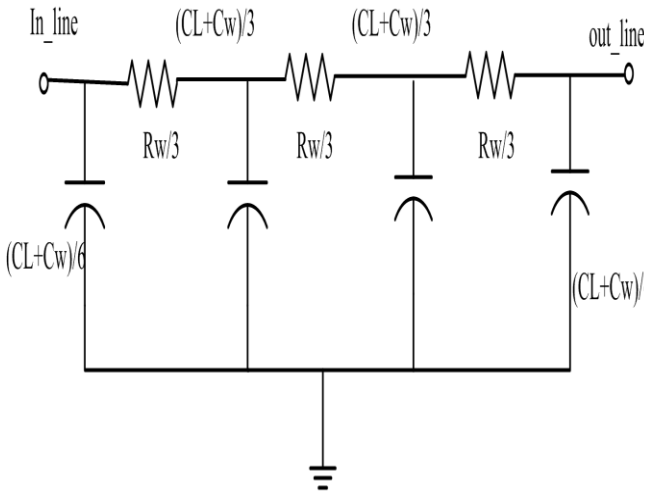

Fig. 2. Interconnect Model

III. DESIGN TOPOLOGIES

Karunakaran et al presented power efficient schemes for clock signals for switched capacitor dc-dc converters. In continuation to the same, this paper presents two more schemes and compares the performance of all the four schemes.

A. Scheme-I

The design topology is shown in Fig. 4. The voltage swing V_s is limited as shown in Equation 1. The reference voltage is avoided by using this limitation.

$$\sim V_{tn} \le V_s \le \left(V_{dd} - \left|\sim V_{tp}\right|\right) \quad (1)$$

The equation 2 describes the energy saving ratio

$$\frac{E_{low}}{E_{tot}} = \frac{V_s}{V_{dd}} \cong \frac{V_{dd} - \left|\sim V_{tp}\right| - V_{tn}}{V_{dd}} \quad (2)$$

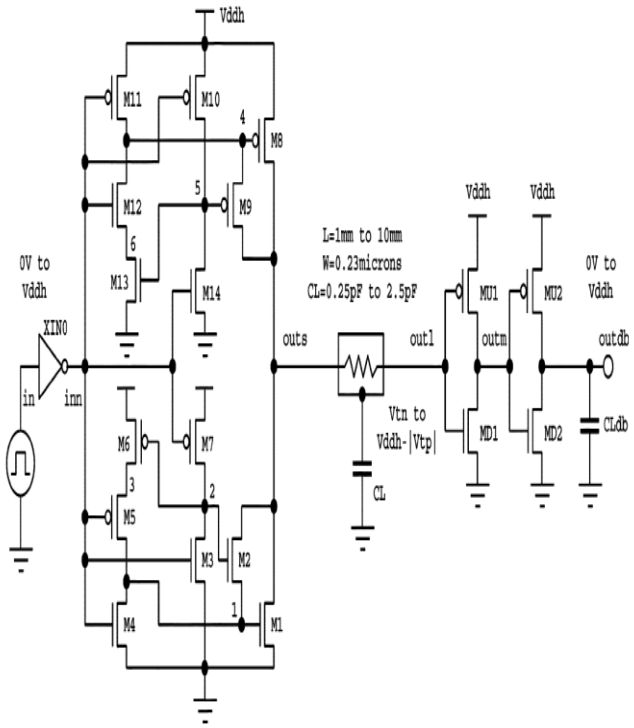

Fig. 3. Circuit Schematic for Scheme-I

B. Scheme-II

The second design topology is shown in Fig. 5.

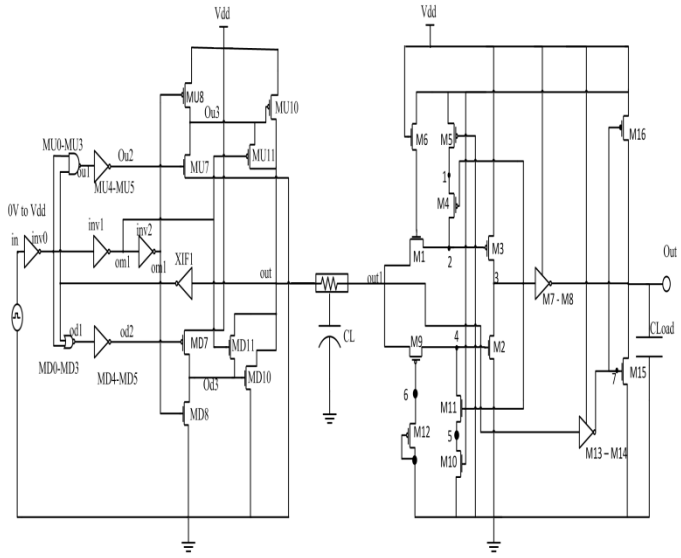

Fig. 4. Circuit Schematic for Scheme-II

C. Scheme-III

Scheme III is presented in Fig. 6. The source end and the converter end circuits are presented in Fig 7 & 8 respectively.

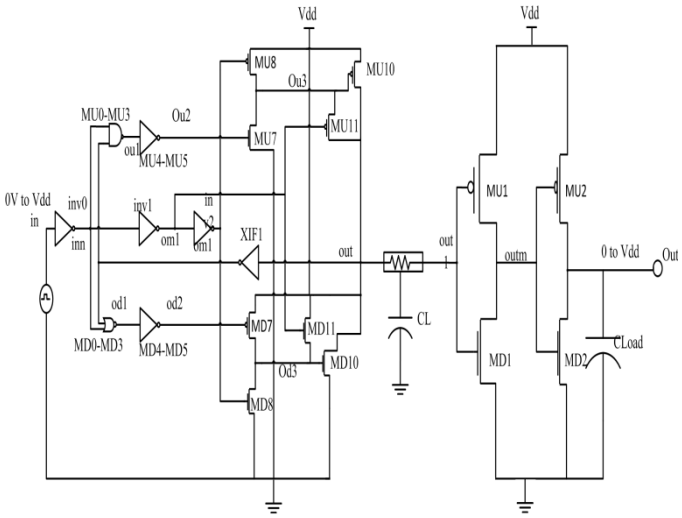

Fig. 5. Circuit Schematic for Scheme-III

The schematic can be isolated into two segments, source end and the converter end as appeared in Fig. 7&8. At the point when the yield in Figure 8 LOW, MU7, MU10 and MU11 are OFF and MU8 is ON. The yield is passed through the diode associated pair MD10 and MD11. At the point when the yield experiences LOW-HIGH change, the postponement in the criticism way causes MU7 and MU10 to turn ON, which destroys the yield hub to HIGH, to energize the heap. In the end, the input circle causes MU7 to mood killer and the entryway drive to MU10 is incapacitated. MU11 anyway is still ON. This keeps up the yield voltage at ≈ (Vdd-Vtp) through the diode associated arrangement pair MD10-MD11. At the point when the yield is HIGH, MD7, MD10 and MD11 are OFF and MD8 is ON. The yield is

headed to HIGH through diode associated pair MU10-MU11. HIGH-LOW progress at the information causes MD7 and MD11 to turn ON because of the postponement in criticism circle. This destroys the yield hub to LOW, releasing the heap. The criticism circle inevitably turns MD7 OFF impairing the door drive to MD10. MD11 stays ON giving a diode associated design pair MD10-MD11 to keep up yield voltage at ≈ Vtn.

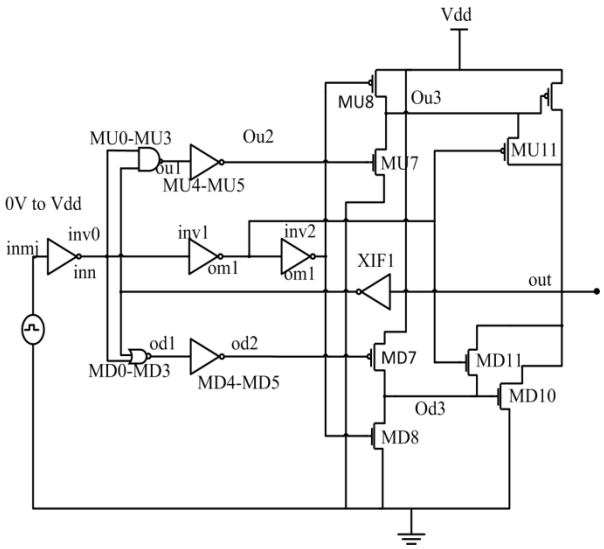

Fig. 6. Scheme-III: Source end Circuit Schematic

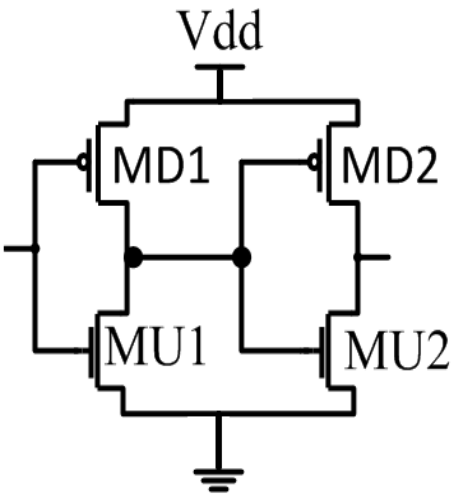

Fig. 7. Scheme-III: Converter end Circuit Schematic

On the other end of the transmission line (dc-dc converter module end), a simple inverter with enable signal is used as in Fig. 8.

D. Scheme-IV

The circuit schematic for Scheme-IV is presented in Fig. 9. For the schematic on the source side, when the input *in* is HIGH, the outputs of INV0 and INV1 are LOW and HIGH respectively. This forces MU1 to be ON and MU2 to be OFF. Hence the output is driven towards HIGH up to V_{dd}-V_{tn}. When the input is LOW the inverters toggle their outputs and force the transistors MU1 to be OFF and MU2 to be ON. Hence, the output is driven to GND. Thus, the interconnect line on the source side can swing from GND to V_{dd}-V_{tn}. On the converter side of the interconnect line, a matching level restorer circuit is used. The feedback keeper is realized by series transistors M4 and M5 reducing the capacitive load on node 3. M5 is sized larger than M4 reducing the loading on M2 and M3. This reduces the power consumption as M2 and M3 can be sized smaller now. M1 and M2 devices are low V_{th} devices.

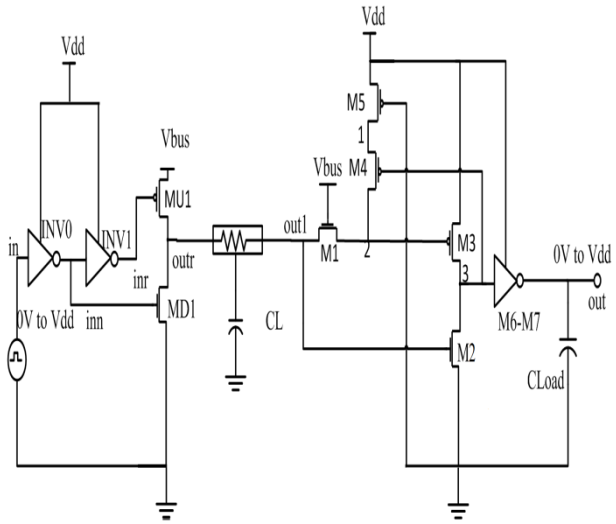

Fig. 8. Circuit Schematic for Scheme-IV

IV. PERFORMANCE EVALUATION AND RESULTS

This section presents and discusses the results obtained from the simulations for Schemes-I to IV. A comparative analysis ispresented for the four schemes. The performance of these schemes is discussed for three performance parameters; delay, power consumption and power-delay product.

A. Results

Fig. 10-15 present various outcomes for Schemes-III and IV for deferral, power and power-postpone item execution as opposed to shifting interconnects length from 1mm to 10mm.

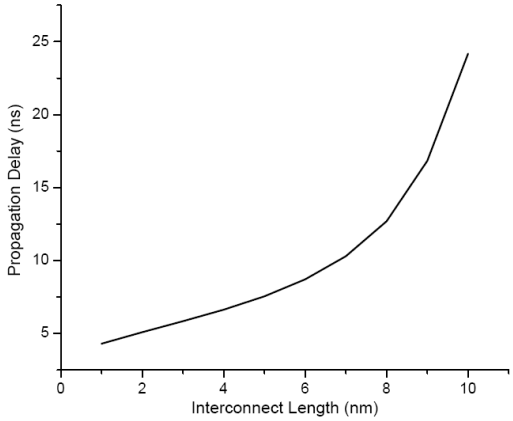

Fig. 9. Scheme-III: Propagation delay vst length

Fig. 16-18 shows the results for the three parameters compiled for all four schemes.

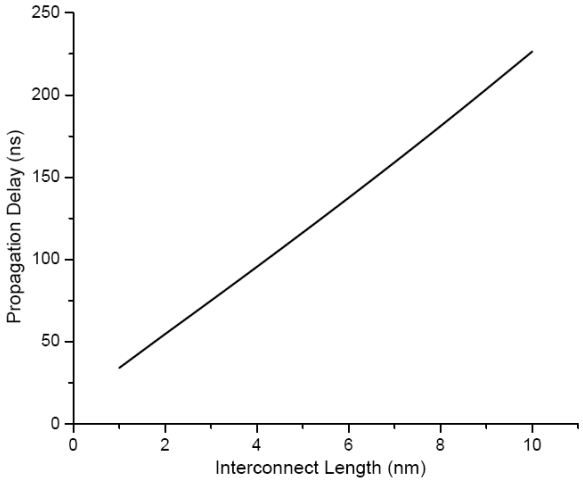

Fig. 10. Scheme-IV: PropagatioVs length

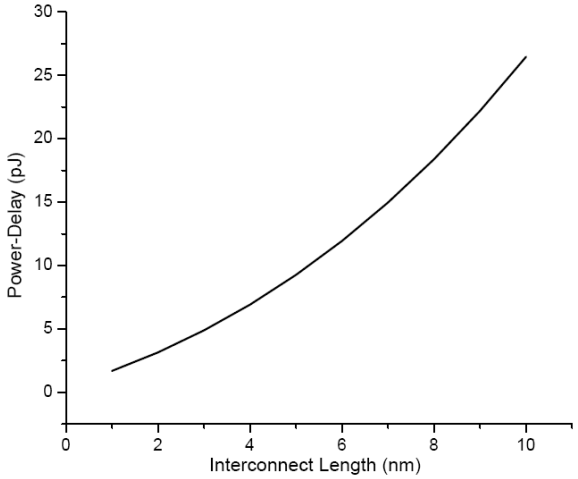

Fig. 13. Scheme-III: Power-delay product vs length

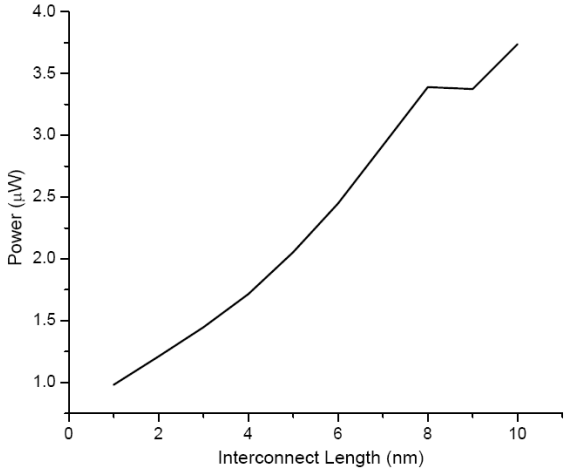

Fig. 11. Scheme-III: Energy consumption Vs length

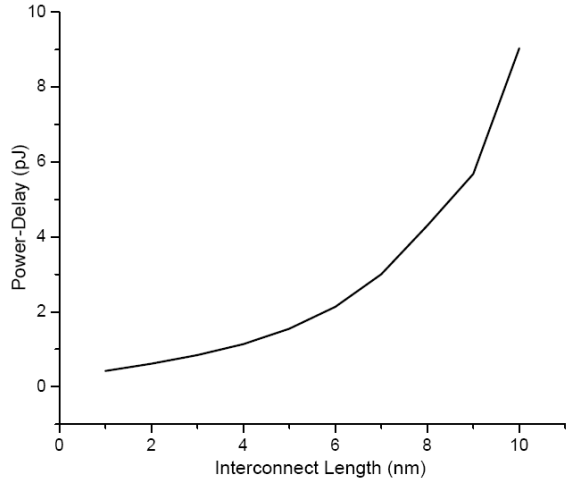

Fig. 14. Scheme-IV: Power-delay product vs length

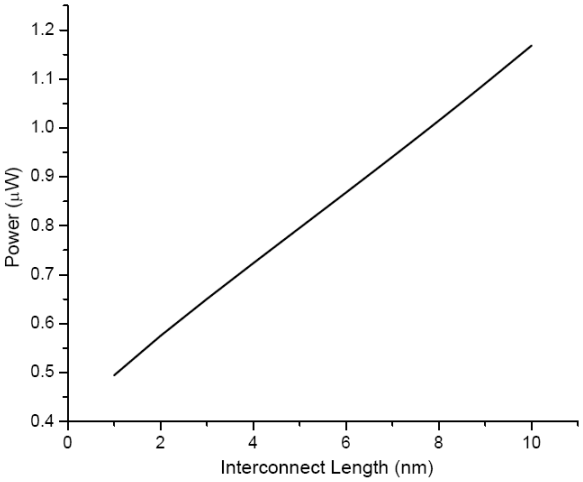

Fig. 12. Scheme-IV: Power consumption versus interconnect length

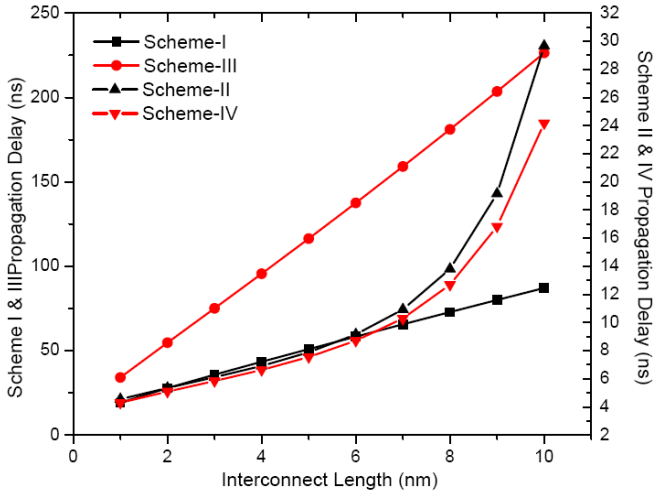

Fig. 15. Propagation delay vs length

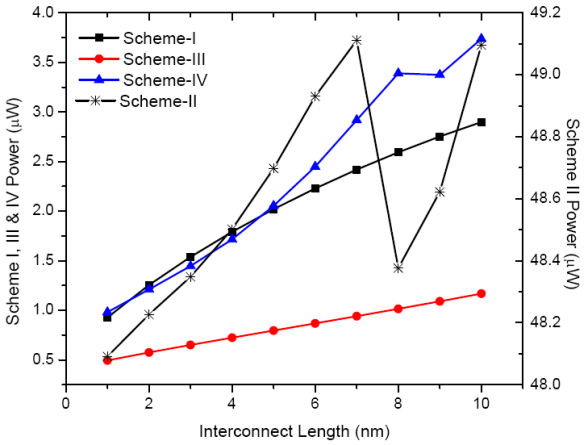

Fig. 16. Power consumption vs length

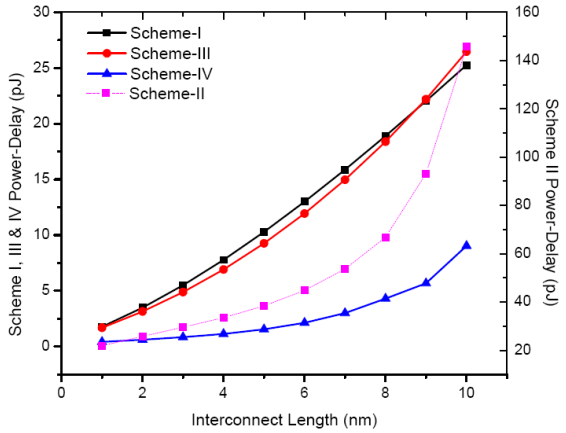

Fig. 17. Power-delay product vs length

B. Discussion

As shown in Fig. 16, scheme I & III have very high propagation delay as compared to scheme II & IV. For schemes I & III the delay varies linearly with interconnect length whereas, for schemes II & IV it varies as quadratic with interconnect length.

Fig. 17 shows that scheme-II demands higher power consumption as compared to all other schemes. While schemes I & IV have comparable power consumption for lower interconnect length, power consumption for scheme-IV increases for higher interconnect lengths. Scheme-III has the minimum power consumption among all the schemes.

Power-delay product for scheme-II rises exponentially for higher interconnects lengths. Power-delay product for scheme I & III is almost comparable for all interconnect lengths, while that for scheme-IV it is the minimum.

When the criterion for selection is purely power consumption then scheme-III is the best choice but as power-delay product gives a measure of the energy, scheme-IV is the preferred choice because of its lowest power-delay product value.

V. CONCLUSION

This two new plans for circulating the timekeepers for exchanged capacitor converters in superior processors. Performance of these two plans is contrasted and other two plans proposed by the Karunakaran et al as far as three execution paradigm; delay, control utilization and power-defer item. It is reasoned that the Scheme-IV shows better execution as far as engendering delay, while Scheme-III is better regarding force consumption. However, conspire IV is the best as far as the power-postpone item. Thus, it very well may be presumed that Scheme-IV is the favored decision.

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