

Simulation and Design of Low Noise Amplifier

N. NazeeyaAnjum, M.Akshaiya, G.Alagulakshmi

Abstract—A low-noise amplifier is an electronic amplifier that amplifies a very poor signal (in terms of its power) without significantly degrading its SNR. An amplifier increases the power of both the signal and the noise present at its input. A good LNA has a low Noise Figure as well as enough gain to boost the signal thereby does the work required of it. This paper proposes a LNA designed with ATF-21170 to operate in 2.4 GHz with a maximum gain of 18.453 dB and minimum NF 1.346

Keywords : LNA, 2.4GHz, ATF-21170, low Noise Figure, Maximum gain, ADS

I. INTRODUCTION

A low-noise amplifier (LNA) is an electronic amplifier that amplifies a very low-power signal without significantly degrading its SNR. A good LNA has a low Noise Figure, enough gain to boost the signal and a large enough inter-modulation and compression point to do the work required of it. The four important parameters in LNA design are: gain, noise figure, reflection co-efficient and impedance matching.

An amplifier is a network that increases the amplitude of weak signals. Receiver amplification is distributed between RF and IF a stage throughout the system and an ideal amplifier increases the desired signal amplitude without adding distortion or noise. But practically amplifiers are known to add noise and distortion to the desired signal. In a receiver chain, the amplifier located after the receiving antenna contributes most to the system noise. Adding gain in front of a noisy network reduces the noise contribution from that network. So low noise amplifier (LNA) is required to obtain a better gain.

LNA designs differ in their gain, Noise Figure, stability and power consumption. To compare such amplifier designs, typically all the amplifier specifications are mapped into a single scalar called figure of merit and if Figure of merit is large it indicates a more effective design. In the proposed work, a LNA at 2.4 GHz with matching network and its improved stability performance was designed and the performance analysis was simulated by using ADS.

II. PROPOSED WORK

The below mentioned steps were followed in designing the LNA

Revised Manuscript Received on October 15, 2019.

N. NazeeyaAnjum, Assistant Professor- Grade I, Department of Electronics and Communication Engineering, Sri Sairam Engineering College, Chennai, Tamilnadu, India. (Email: nazeeyaanjum.ece@sairam.edu.in)

M.Akshaiya, Student, Department of Electronics and Communication Engineering, Sri Sairam Engineering College, Chennai, Tamilnadu, India. (Email: akshaiyamohan@gmail.com)

G.Alagulakshmi, Student, Department of Electronics and Communication Engineering, Sri Sairam Engineering College, Chennai, Tamilnadu, India. (Email: alagulakshmigomu@gmail.com)

- A. Selection of a transistor.
- B. Stability factor estimation.
- C. Stabilization techniques.
- D. Evaluation of Gain, NF, Output and Input Reflection co-efficient.

A. Selection of the transistor plays a vital role in LNA design. Each transistor has its maximum available gain (MAG) and a minimum noise figure (NFmin) at a particular frequency. So a LNA which gives more gain than maximum available gain and a Noise figure less than minimum NF cannot be designed. ATF-21170 transistor was selected for LNA design as its specifications were matching as per our targeted values. Transistor biasing is done in order to maintain proper zero signal collector current and maintenance of proper collector- emitter voltage when signals are applied. The circuit which facilitates this is known as a bias circuit. The LNA and its biasing was designed in the workplace of the ADS in the standard ADS layers by placing the lumped components from the component palette present in the left side of the ADS workspace.

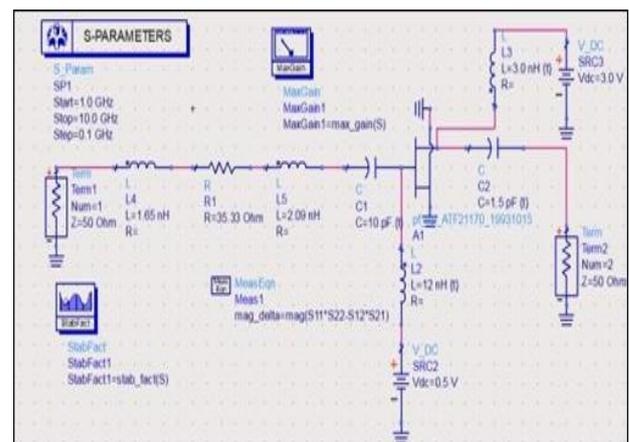


Fig. 1 Circuit Diagram of Low Noise Amplifier

B. Stability Analysis is very important consideration in design of not only LNA but any RF circuit design. Stability can be determined by S- parameters. Delta (Δ) is intermittent quantity and K is the Rollett stability factor.

If $K > 1$, then the circuit is said to be unconditionally stable which means its stable for any combination of given source and load. For $K < 1$ and $\Delta < 1$, system is said to be

potentially stable. Thus, the K factor provides quick check for stability at a given frequency and bias condition. The formulas to estimate K and Δ are as follows,

$$K = (1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2) / (2 |S_{21}| |S_{12}|)$$

$$\Delta = S_{11} S_{22} - S_{12} S_{21}$$

Where,

- S_{11} = Input return loss or Input reflection coefficient
- S_{22} = Output return loss or Output reflection coefficient
- S_{21} = System gain
- S_{12} = Reverse voltage gain

Depending on the values of S-Parameter, the values of $K = 0.719$ obtained using ADS software and $\Delta = 0.537$. This shows that the value of $K < 1$ and $\Delta < 1$, this results reflect a potential unstable transistor. Hence the transistor had to be stabilized.

C. Stabilizing Technique incorporated here was to reduce the impedance mismatch at the input port. An impedance matching network was implemented using the Z-Y plot available in the ADS. The inductance and resistor combination provided the impedance matching at the input port. Thus, the effect of impedance mismatch was overcome using this RL filter. Thus, the stability of the LNA was achieved by introducing matching network at the input port. The impedance matching and stability can also be achieved by using other techniques as well. The K factor and Δ were again simulated after adding impedance matching network. $K = 1.894$ and $\Delta = 0.274$ after adding input matching network thus resulting in an unconditionally stable transistor circuit.

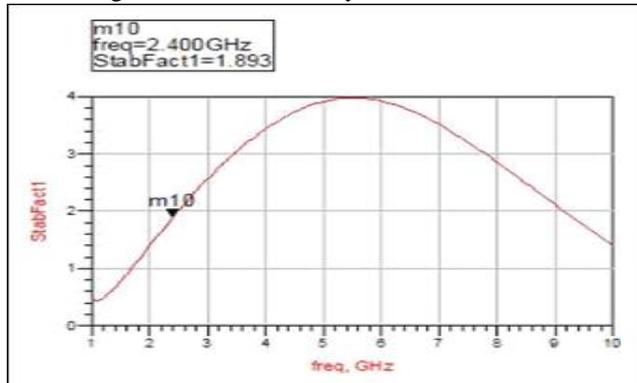


Fig.2(a) Stability Factor Plot

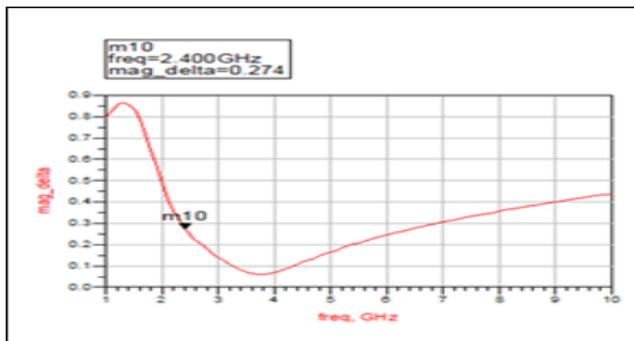


Fig. 2(b) Rowlett Factor Plot

D. Estimation of Gain, NF, Input and Output reflection coefficient. The various S- parameters were simulated and Gain, NF, Input and Output reflection coefficient were analyzed from the plots obtained from simulation, the results were found to be satisfactory.

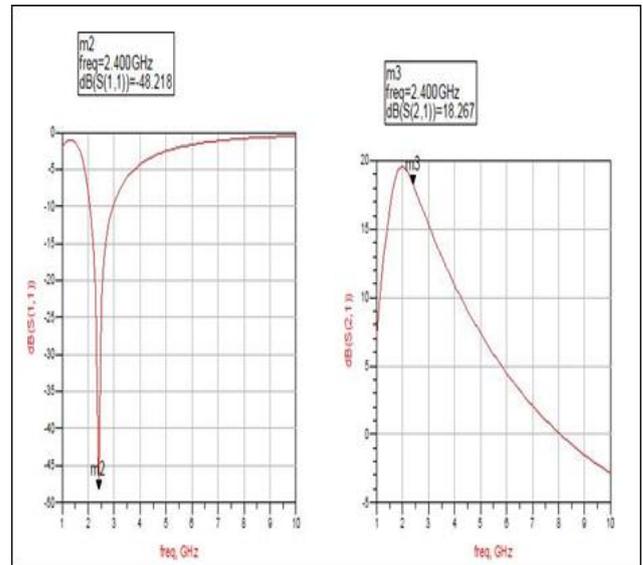


Fig. 3(a) S11 and S21 plots

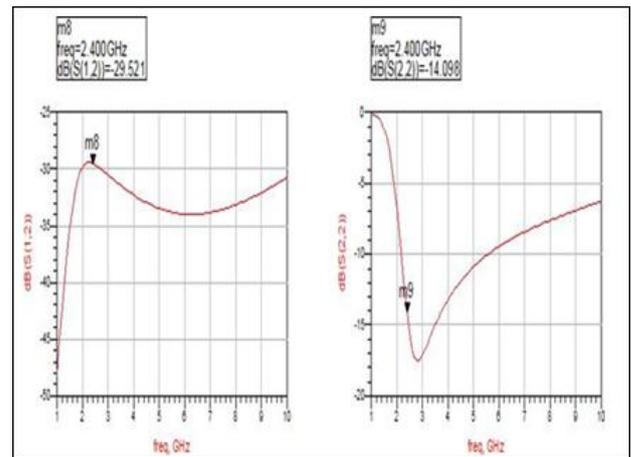


Fig. 3(b) S12 and S22 plots

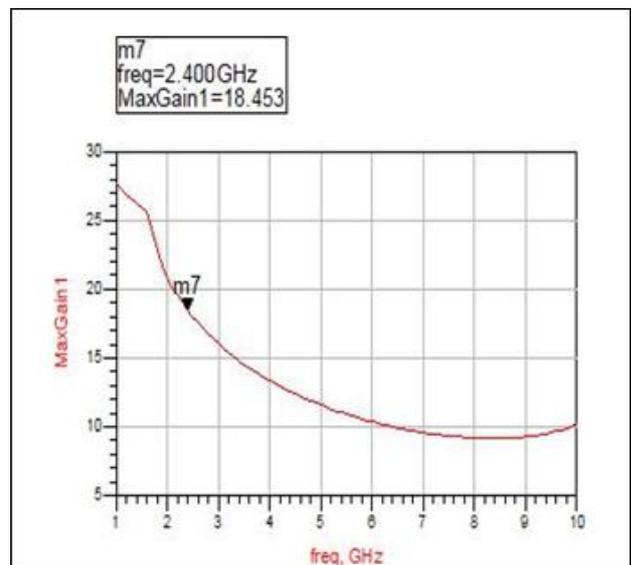


Fig. 3(c) Maximum Gain plot

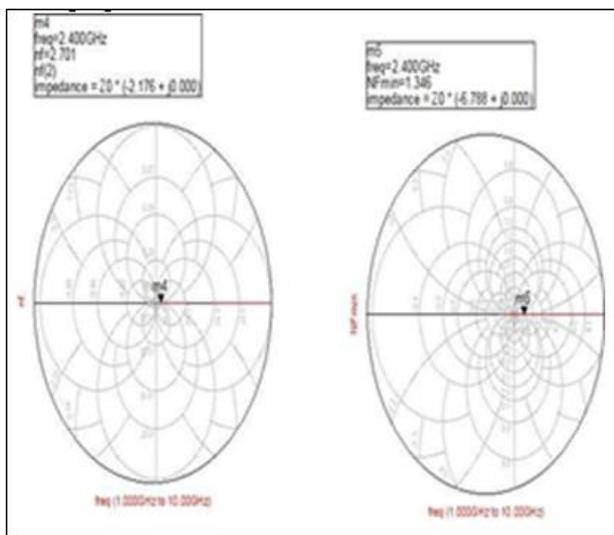


Fig. 3(d) NF and Minimum NF plot

III. RESULTS

The various LNA parameters obtained as result of simulation work have been tabulated below.

Table 1. Simulation Results

S.No	LNA Parameters	Values in dB
1.	Input Voltage Reflection Coefficient, S_{11}	-48.218
2.	Forward Voltage Gain, S_{21}	18.267
3.	Reverse Voltage Gain, S_{12}	-29.521
4.	Output Voltage Reflection Coefficient, S_{22}	-14.098
5.	Maximum Gain	18.453
6.	Noise Figure	2.701
7.	Minimum Noise Figure, NFmin	1.346

IV. CONCLUSION

The responses were found to be satisfactory; even then we have scopes to improve the performance. The circuits can be optimized with more effective matching techniques which would result in good response. In future, various types of band pass filters such as elliptical, Chebyshev with different orders can be incorporated with LNA to provide more selectivity and improved system performance in terms of gain and NF. New prototypes can be made with components which were used in the simulation; it may produce better response of LNA than the one designed with lumped components. The knowledge acquired from this work will certainly help to design the whole RF receiver system in the ISM band. Inductor design techniques are specified in literature. [7] inductor based LNA design requires less silicone but it adds more noise and consumes more power compared to passive inductor design. The NF and power consumption of active inductor based LNA can be reduced by using noise cancelling networks and low power LNA design. RF front end have three main

analogblocks LNA, Mixer and Local oscillator. The work can be expanded by the design of mixer and local oscillator [7] for multi standard universal receiver and integrate proposed LNA design with mixer and local oscillator to make complete RF frontend.

REFERENCES

1. Reena K. Panchal, Harsha Gupta, Design and Simulation of Low Noise Amplifier at 2.3 GHz Frequency for 4G Technology, International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 4, Issue 6, June 2015.
2. V. M. García-Chocano, Low Noise Amplifier Basics, 24-Oct-2017.
3. S.Vimal, Dr.M.Maheshwari, Design and performance improvement of a low noise amplifier with different matching techniques and stability network, National Conference on Information, Communication, VLSI and Embedded systems, 16 - 17 March 2016.
4. Arun Sharma, Jaikaran Singh, MukeshTiwari, Design And Simulation of 0.18 mm CMOS LNA for UWB System, 17 January 2016.
5. <https://www.keysight.com/en/pc-1297113/advanced-design-system-ads?cc=IN&lc=eng>
6. <https://www.digikey.in/>
7. http://shodhganga.inflibnet.ac.in/bitstream/10603/149765/9/17_chapter7.pdf

AUTHORS PROFILE



NazeeyaAnjum .N, aged 40 is a Assistant professor in Department of Electronics and Communication Engineering department at Sri Sairam Engineering College. She completed her Masters of Engineering at Anna University, Chennai with First Class Distinction in 2006 and has a total of 18 years of teaching experience added to her credit. Her special interest are towards Antenna design, Electromagnetic Interference & Compatibility, Communication Engineering and Embedded systems. She has actively participated in many workshops, National and International conferences and has presented and published papers in few of them. She has so far guided 10 undergraduate and 2 post graduate projects in her tenure.