

Gigabit Ethernet Switch Characterization over VPX Backplane

Vinayak Kumbhar, Lalita Admuthe, Vinod Kumbhar

Abstract: Complexity & Criticality have made the latest state of the art Military/Aerospace systems more and more I/O and data intensive. Demand for huge chunk of signal information drives the innovation in the technology to make the systems capable of transforming the data at higher and higher speeds. So, computers and communication devices use VPX technology to communicate with other devices because, VPX support multi Gigabit communication and it is very rugged, compact and portable. So switching systems used for communication in military and aerospace should also support VPX connectivity. Characterizing switch, which gives connectivity on VPX and which communicate through VPX switched fabric backplane with other devices on same backplane is difficult and tedious task. In switch there are many stress points, which may cause switch goes down in network. To characterize these stress points, we designed VPX based test card and characterize data plane performance of switch by measuring some parameters and analyzing transmitted and received frames. Also by preparing setup for environmental characterization we can test performance for different environmental conditions. Also using environmental chambers, we characterize for environmental parameters at different ruggedized levels.

Keywords: VPX, VME, EMI, EMC, Backplane, DUT, OpenVPX.

I. INTRODUCTION

Communication Devices And Interfaces Used In Military And Aerospace Industry Must Be Highly Ruggedized, Must Sustain High Temperature, Extreme Humidity Conditions And Harsh Working Environments. Considering The Requirements In Present Day Embedded Computing And Communications, Various Technologies Like Serial Rapidio, Infiniband, PCI Express (Peripheral Component Interconnect) And Gigabit Ethernet Evolved, Out Of Which Ethernet Interface Is Of Very High Importance In Present Day Systems. Even In Harsh Environments Like Military And Aerospace Ethernet Works Seamlessly. In Military And Aerospace, There Are Several Standards Used For Communication. Out Of Such Standards, Backplane Communication Standards Play A Crucial Role. There Are Backplane Communication Standards Like VME (VERSA Module Eurocard), VPX (Virtual Path Cross-Connect), VXS (Vmebus Switched Serial) Which Are Used Extensively In

Revised Manuscript Received on November 06, 2019.

Vinayak Kumbhar, Assistant Professor in Electronics Department, DKTES Textile and Engineering Institute, Ichalkaranji

Second Author Name, Professor and head of Electronics Department, DKTES Textile and Engineering Institute, Ichalkaranji

Vinod Kumbhar, Assistant Professor in Electronics Department, DKTES Textile and Engineering Institute, Ichalkaranji

The field. The focus in military and aerospace is concentrated around network-centric warfare, increasing usage of video, digital signal processing, graphics, processing, and sensor data acquisition and generally more compute intensive applications. In Radar processing, for example, requires huge bandwidth. With increasing application demands (speed, power, increased bandwidth, operational conditions, and increased functionality) the existing VMEbus specification may not be sufficient. With the identifiable challenges, a later version of backplane standard called VPX superseded. VITA (VMEbus International Trade Association) developed VPX. The main advantage is that VPX also uses the general sizes 6U and 3U card of VME.

VPX standard offers proper rough capabilities, counting conveyance resistance and cooling to vibration and shock. At the like instance, it gives superior power budgets, extra signal density and an extreme faster serial backplane, which fulfils most of requirements of industry, military and aerospace. These are some of the reasons why VPX has become so popular in short time. Examples of present days computing devices which utilize VPX standard are Single Board computers (SBC), different I/O boards, routers, switches, graphics cards etc. The design of such computing devices is a far more challenging part then the standard. Designers all over the world are utilizing their skills to come up with devices compatible with the latest backplane standards. Apart from designing these devices, designer has to characterize their design for functional and environmental parameters before mass production.

Ethernet switch is a part and parcel of the modern-day communication systems. After design, bring up and Characterization of VPX based gigabit Ethernet switch is done using various VPX backplanes. VPX backplanes can be committed and uncommitted. For testing Ethernet switch over VPX backplane, we use various test equipment and test data is generated using available tools like Spirent Test Centre (STC). Environmental testing is done using environmental chambers.

II. LITERATURE REVIEW

IEEE in 1983 standardized the Ethernet and Ethernet has turn into the world's largely extensively used networking technology.

Gigabit Ethernet Switch Characterization over VPX Backplane

In day to day life 95% world's data runs over Ethernet and 85% local area networks are Ethernet based. Still, Ethernet's market requirement increases and it turning into wireless networks, WAN, First Mile, MAN, and so on. Thus, the opinion in opposition to using switched Ethernet in the backplane have not been logical, but alternative have been technical, complaints such that Ethernet has very large latency, suffers from packet processing inefficiency in relation to other proposed standards and lacks advanced congestion control [1].

While alternative interconnect standards are competitor for property market share, Ethernet has been doing what it's continually done best for the requirements of a brand new application by adapting and scaling. Ethernet's speedy advancement into new areas could be direct results of the actual fact that it's therefore omnipresent. Its success has become in a very possible way a self-sufficient development. Ethernet's current use has junction rectifier to widespread understanding and technical power, that successively has junction rectifier to the creation of an energetic system of engineers, makers, and users with the will and means that of regularly extending the practicality of primarily Ethernet based communications.

Demand for huge chunk of signal information drives the innovation in the technology to make the systems capable of transforming the data at higher and higher speeds. So computers and communication devices used in military and aerospace are developed to communicate over VPX because, VPX support Multi Gigabit data rates, very rugged, compact and portable [2].

So, network switches used for communication in military and aerospace should also support VPX connectivity. But, if VPX committed backplane is not used then to connect devices to switch require cables. This makes difficulty to handle devices, reduces speed, and increases chances of disturbance and damage of cables which may affect communication. So now days we use VPX backplane which provides facility to devices (connected to same backplane) to communicate with switching device through VPX backplane [3].

We know now the popularity of Gigabit and 10 Gigabit Ethernet in communication systems and networks. Even Military and Aerospace domain use Ethernet technology for communication. And we know that in military and aerospace VPX backplane is used for the Ethernet switches for communication. Many industry efforts are done in earlier years to bring Ethernet to backplane, like PCIMG 3.1 standard, 802.3ar and 802.3ap initiatives which are taking out the tech roadblocks to Ethernet implementation and to make preferable choice for interconnects these days. [4][5].

The standard mentions however network instrumentality manufacturers will transmit Gigabit local area network and ten Gigabit local area network up to 1 meter on backplanes of standard, chassis-based platforms employed in enterprise networks and knowledge centres. With standardization, we can accept that the coming of a best results in lesser prices and

improved products for users. As the communication among the devices directed by standards, we are not sealed in to an only vendor for entirely the parts. Obviously, the Ethernet Medium Access Control (MAC) and the min and max frame sizes previously quantified by the IEEE will be adhered to [6]. The standard conjointly offers for auto-negotiation among the modules, because of this module can spontaneously configure themselves to the maximum link speed conceivable. The Ethernet Association media announces the criterion's accomplishment speaks that 802.3ap Could also be employed by the PICMG, which earlier leveraged 802.3z and 802.3ae [5][7].

To implement these standards over VPX backplane OpenVPX group developed some standards [2]. The VPX standard, known formally as ANSI/VITA 46, and as the OpenVPX standard ANSI/VITA 65, was designed to extend the mechanical concepts of VME systems with multiple high-speed serial point-to-point communications buses. Ethernet has been considered a primary communications bus within the VPX standard, being used exclusively for the Control Plane bus, and as one of many options for the higher-speed Data Plane bus [1].

Where the ANSI/VITA 46 VPX standard allows an extremely large number of bus, protocol and speed options, the OpenVPX standard has attempted to narrow the selection to a smaller number of popular interface choices [8].

A. Control Plane Ethernet

OpenVPX defines a single Control Plane across all modules. In OpenVPX terminology, the Control Plane is electrically connected for either Thin-Pipe (TP) or Ultra-Thin Pipe (UTP) connections using central switch architecture. Thin-Pipe profiles mandate the use of 1000Base-T Ethernet connections. Complying with the IEEE 802.3-2008 standard, the 1000Base-T interface provides auto-negotiation services which ensure backwards compatibility with 10Base-T (10Mbps) and 100Base-TX (100Mbps) interfaces [2].

Ultra-Thin Pipe profiles mandate the use of 1000Base-BX Ethernet connections, but can also support 1000Base-KX connections, both of which have similar electrical specifications. Using half the number of signal pins as the Thin-Pipe interface, the Base-X interface uses 2-pairs of signal wires at signal speeds of 1.25Gbps [2].

B. Data Plane Ethernet

The Data Plane, the OpenVPX standard approved by ANSI in 2010 and updated in 2012, has defined only the 10GBase-BX4 and 10GBase-KX4 Ethernet interface standards. And this standard also defines other Data Plane fabrics, such as PCI Express (PCIe) and Serial RapidIO (SRIO) [2].

C. Ethernet Switch

An Ethernet Switch operates at the data link layer of the OSI reference model. A switch is primarily same as a bridge, but generally carries a more number of linked LAN segments and has a better-off management ability. Recent LANs have progressively changed the shared media with a switched media, by Ethernet switches and bridges installation in place of repeaters and hubs. These logically divides the payload to move only on the network pieces on the path among the source and the destination. It causes decrease in wastage of bandwidth which further results from transmitting the packet to piece of the network which do not need to receive the data [9]. Also Benefits from enhanced security, best management and to bound the effect of network problems, and the capability to work few links in full duplex [10].

Advances in 10 Gbps Ethernet switch chip design and manufacture, which reduced total device latency to 200ns, a tenfold improvement over early-generation Ethernet data fabrics. TCP offload Engines (ToE) developed hardware-based protocol processors that improved all TCP processes and offload them from the system processor, has only a few microseconds lowered endpoint latency.

Moving former protocols over an Ethernet switch and backplane is reasonably forthright and efficient in that a source packet can be positioned inside an Ethernet packet without changing the original header or parsing the payload.

D. Board bring up and debugging

After you design the electronics, manufacture the board and assemble it, you need to "bring it up". Bring up includes power supply check, debug, programming and make it bootable. Before proceeding to the next level of the project, these steps need to check for consistency over a queue of boards.

The definition of debugging is to identify and remove errors from (software or hardware). Locating and fixing bugs (errors) in computer code or in designed hardware. Intent of hardware performance check is to confirm that the underlying design is capable to perform desired tasks. To understand and verify design bottleneck and limitations hardware testing will help. Design and verification team will get complete picture of optimized and max capacity performance by stress testing. To confirm that the hardware is capable to retain hop with the loads of the industry these metrics will nourish into future capacity plans and strategies.

Designing a price inexpensive electronics system needs cautious concern of the thermal domain and electrical area. Overheating and system breakdown may be problems for under designing system. Designing an optimum solution needs a decent understanding of how to forecast the working temperatures of the system's power devices and how they get heated by surrounding components, such as capacitors and semiconductor devices.

In general, we do not want on board electronics of any aircraft to fail. This is just one example of safety critical

systems where high level of reliability is a must. Breakdown of electronics systems in around 55% of all cases was due to thermal problems this is observed by the US Air Force Avionics Integrity Program which is carried about two decades ago. A typical failure mechanism which leads to thermal problems is when the thermal interface materials degrade.

Performance of equipment may get decrease or may cause breakdown due to electromagnetic disturbance is nothing but electromagnetic interference (EMI).

Electromagnetic compatibility (EMC) is a almost perfect state in which a receptor works desirably in general electromagnetic surroundings. To explain it other way, the system must be work deprived of introducing Unbearable electromagnetic trouble to any other equipment's, devices in that surroundings.

Categorization of EMI/EMC:

- Radiated emission
- Radiation Susceptibility
- Conducted emission
- Conduction Susceptibility

Power consumption testing: Power consumption is a critical criterion for any system. For any device integrated into an existing system and importantly the power requirements are achieved by it in which case interoperability will be smooth. For this, a newly designed system must be throttled to maximum load and corresponding power consumption must be calculated. The same power consumption can be declared in the unit datasheets and user manuals.

E. Ethernet for OpenVPX Systems

The VPX standard, known formally as ANSI/VITA 46, and as the OpenVPX standard ANSI/VITA 65, was designed to extend the mechanical concepts of VME systems with multiple high-speed serial point-to-point communications buses. Ethernet has been considered a primary communications bus within the VPX standard, being used exclusively for the Control Plane bus, and as one of many options for the higher-speed Data Plane bus.

Where the ANSI/VITA 46 VPX standard allows an extremely large number of bus, protocol and speed options, the OpenVPX standard has attempted to narrow the selection to a smaller number of popular interface choices.

F. Control Plane Ethernet

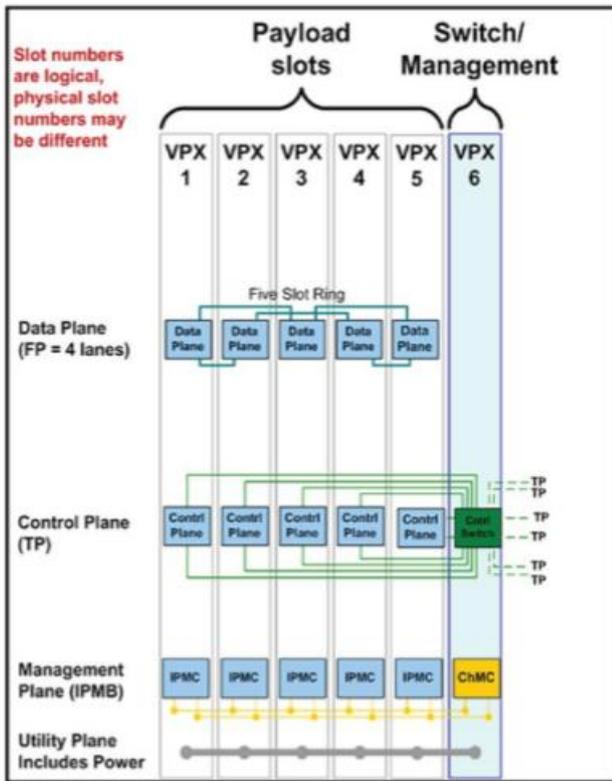
OpenVPX defines a single Control Plane across all modules. In OpenVPX terminology, the Control Plane is wired for either Thin-Pipe (TP) or Ultra-Thin Pipe (UTP) connections using central switch architecture. Thin-Pipes for 1000Base-T Thin-Pipe profiles mandate the use of 1000Base-T Ethernet connections. Complying with the IEEE 802.3-2008 standard, the 1000Base-T interface provides auto-negotiation services which ensure backwards compatibility with 10Base-T (10Mbps) and 100Base-TX (100Mbps) interfaces. This



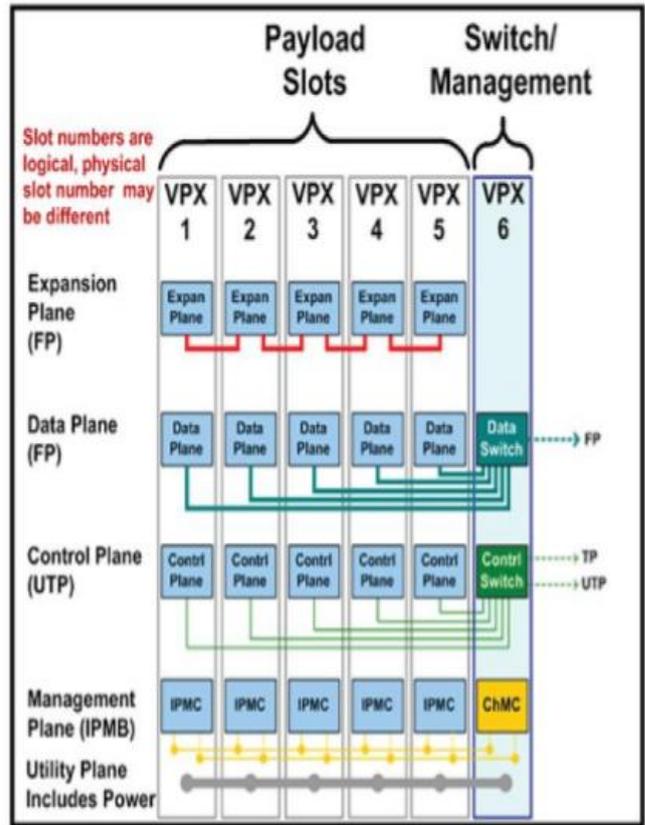
Gigabit Ethernet Switch Characterization over VPX Backplane

Base-T interface uses 4-pairs of signal wires at signal speeds of 125Mbaud. As this interface complies with the 1000Base-T standard, it can be easily wired to external connections, and used to interface with external Ethernet equipment.

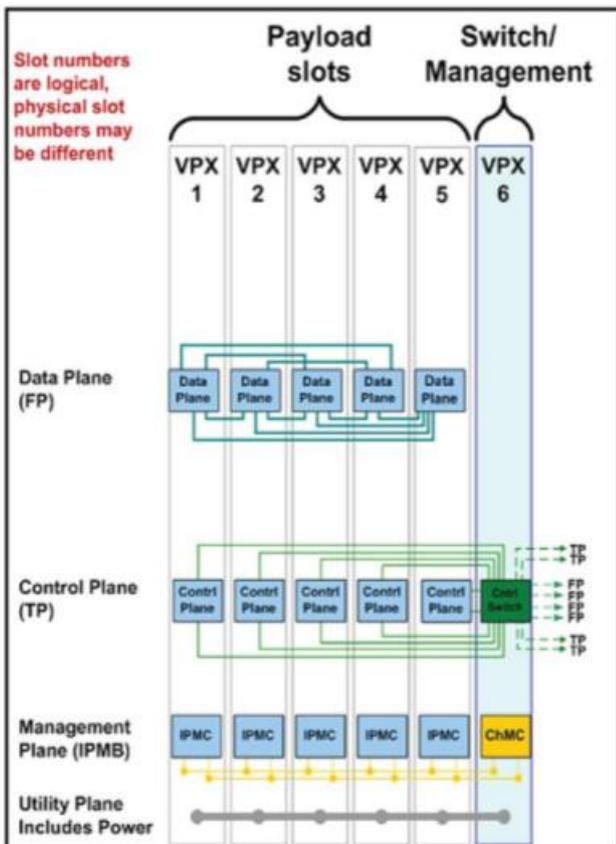
Fig. 1. OpenVPX Backplane Profiles using TP Control Plane Pipes: BKP3-DIS06-15.2.14 and BKP6-DIS06-11.2.10



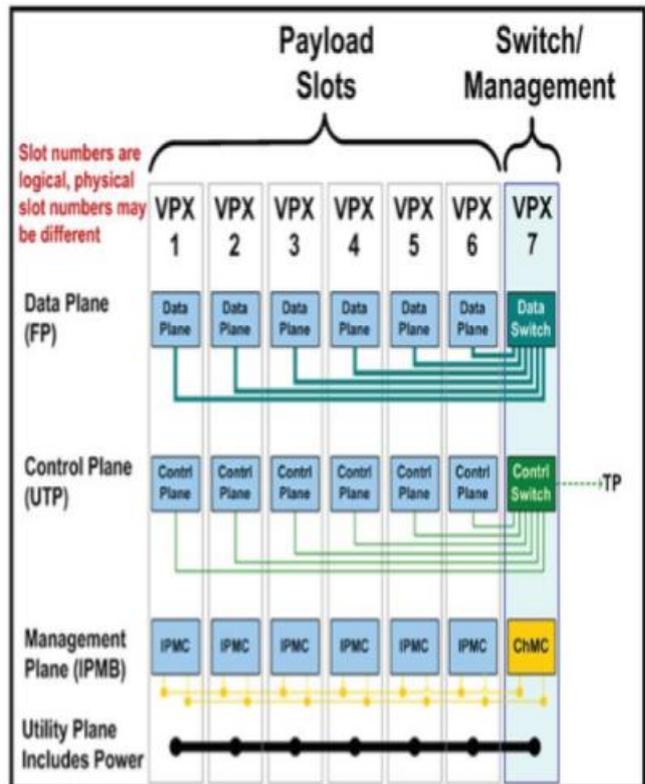
BKP3-DIS06-15.2.14



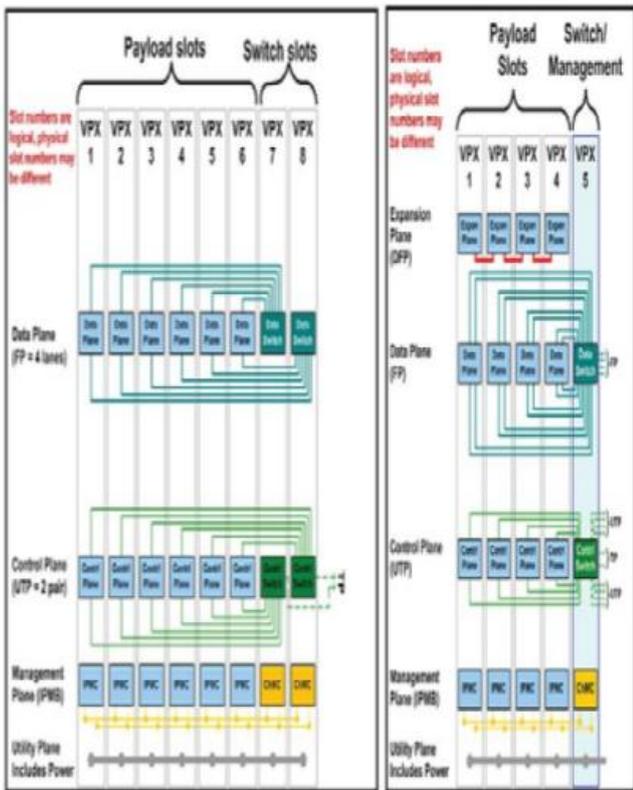
BKP3-CEN06-15.2.2



BKP6-DIS06-11.2.10



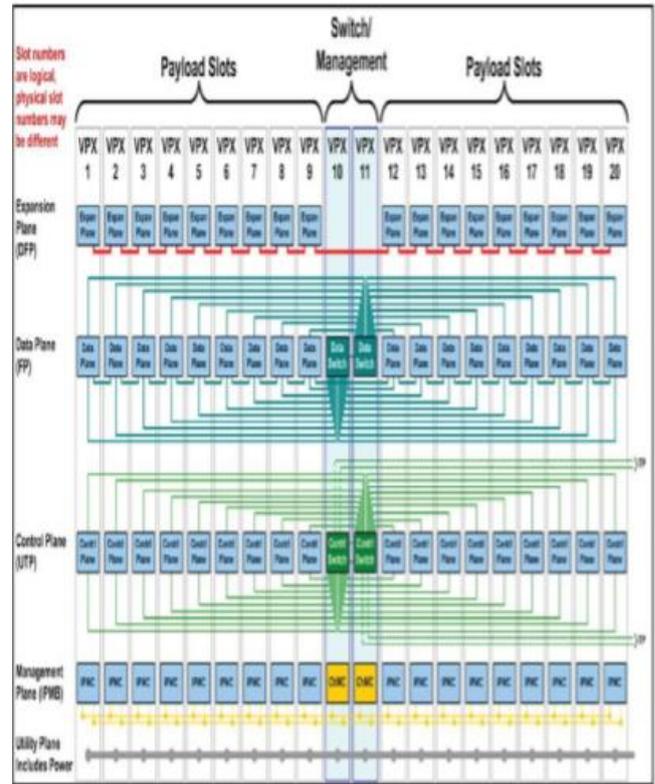
BKP3-CEN07-15.2.3



BKP6-DIS06-11.2.15

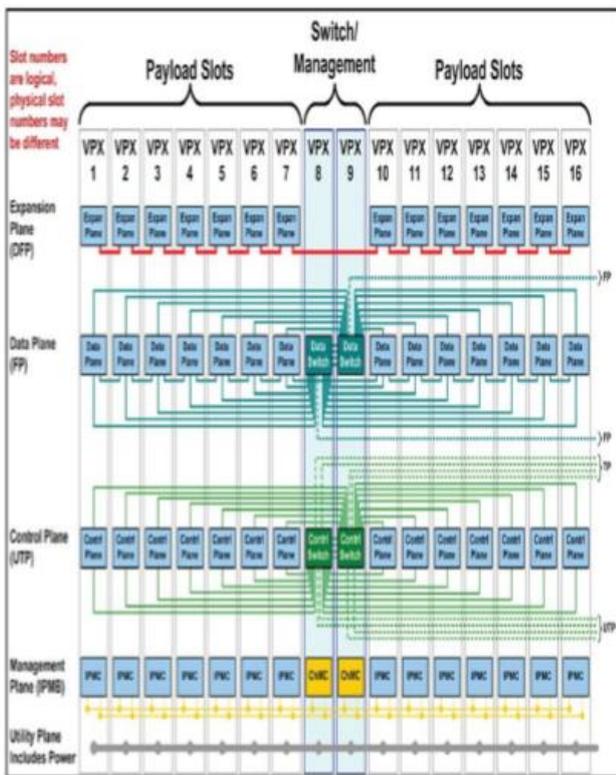
BKP6-DIS06-11.2.10

Fig. 2. OpenVPX Backplane Profiles using UTP Control Plane Pipes: BKP3-CEN06-15.2.2, BKP3-CEN07-15.2.3, BKP3-CEN08-15.2.15, BKP6-DIS06-11.2.10



BKP6-CEN20-11.2.3

Fig. 3. OpenVPX Backplane Profiles using UTP Control Plane Pipes: BKP6-CEN16-11.2.2 and BKP6-CEN20-11.2.3



BKP6-CEN16-11.2.2

G. Ultra-Thin Pipes for 1000Base-X

Ultra-Thin Pipe profiles mandate the use of 1000Base-BX Ethernet connections, but can also support 1000Base-KX connections, both of which have similar electrical specifications. Using half the number of signal pins as the Thin-Pipe interface, the Base-X interface uses 2-pairs of signal wires at signal speeds of 1.25Gbps.

An additional advantage of the Base-X interface is that the interface does not require coupling transformers, resulting in reduced component board space, and eliminating a generally large and highly mechanical component at each end of the interface. This aids in lowering Size, Weight and Power (SWaP), and increases system MTBF. The following OpenVPX backplane profiles show examples of Control Plane Ethernet on Ultra-Thin Pipes using central switch architecture as shown in Figure 3.

H. Control Plane Ethernet beyond Gigabit Speeds

The OpenVPX specification currently lists gigabit speeds (1000Base-T, 1000Base-X) for the Control Plane. However, it is conceivable that future revisions of the specification will adopt higher speed signals, such as 10GBase-T and/or 10GBase-X, using the same signal pins as currently defined. Extreme care will need to be taken when designing copper backplanes to carry these higher speed signals.

III. METHODOLOGY

Ethernet switch reach to Multi gigabit speeds and their internal architecture becomes more and more complex, giving better and better performance. Ethernet switch design becomes complex but design and validation methods and tools are advanced beyond conventional models and technical experience to effectively design and verify these designs. The capability to attain packed design functionality at haste is being confronted. To confirm a rapid hand-off to produce these greater performance designs, there is a serious requirement to confirm design performance at very first production, though the device is quiet in engineering change. This is particularly the case as complex design and application stretch method to large complex system level validation.

A. Proposed Idea

The highest effect on design success lies in design validation. And grounded on guesses in over-all and it becomes additionally critical when it is connected to avionic or defence systems, it must clear lots off tests like environmental, functional and RoHs, so design validation may become even more critical.

RoHs can be considered at time of component selection and production. But most critical is functional and environmental characterization. As we seen in introduction and literature survey most of electronics communication and control devices are VPX based. These all devices communicate Over VPX backplane which supports very high speed. This is the one more and most critical challenge in validating VPX based designs over VPX backplane.

If we are not able to characterize or validate for performance at its peak, then there is no use of designing the greatest, fastest and latest systems. For more complicated digital designs, in circuit emulation, enhanced simulation technologies and proper verification tools are barely keeping pace. To deal large complications in design to test to manufacturing process requires major enhancements even though for mixed signal design few decent tools are present. For user's system compatibility and reliability may be too costly. In businesses, distinctive on-site help charges are more for a small service call which may be approximate to replace a system. Due to lack of technical skill, and not having instant access to skilled repair or troubleshooting services consumers face even more problems. For businesses and consumers, the charges of solving a reliability or compatibility matter can rapidly worsen above the original price of the systems. Validation has an important role in serving to retain these costs low, dropping customer risk, and enhancing the longstanding worth of afresh bought systems. Surely, the complexity problems represented by latest technology don't just emphasis on validation problems; there are frightening challenges connected to materials, engineering methods, packaging, growth time, cost and reliability. But if we consider time, cost and efforts investments in validation is about 50% so it is more important.

In its technology roadmaps and forecasts of upcoming aerospace and military product growth, the VITA group has

specified that time-to-market-to- yield-to sample will be gated by test. This announcement is agreed by MIL/AERO manufacturers who complain that 50% of total system development cost and time requires for test debug. Complicated designs need extra time for test development, debug, characterization and breakdown analysis, and quick hand-off to production. The answers may be found in engineering validation, which examines breakdown and provides design and product engineers a pure roadmap to solve problem.

B. Traditional Validation Methods and Challenges

With electronic design automation (EDA) design verification tools, built-in-self-test (BIST), lots off test centre tools and design for test (DFT) approaches, manufacturers use a various of approaches to confirm first prototypes. This comprises convention built stand and loads instrumentation, automatic test equipment (ATE) and devoted engineering confirmation systems. Surely, each system has its benefits, but nothing brings the decisive info that is attainable from a committed engineering confirmation system.

Till the arrival of great speed, great performance ICs, validation engineers at numerous manufacturer companies designed collective or conventional designed benchmarking test instrumentation. This method was comparatively effective when systems were occupied with few complex ICs or with simple logic and analog abilities. Though, recently available highly advanced designs, where lots of small complex systems are embedded on single board, benchmarking test instrument cannot reliably handle the max range of at speed functional testing and can give max feature testing.

For complex VPX based systems with very great frequency and very small signal strength cannot handle the amount of analysis required by the bench-top instrumentation. Depending on device it is difficult and unreliable to test each iteration of product or net generation. The core competency which are demanded to derive which are beyond and they are extra practical level, extra benchmarking specialized skills. Requires dedicated software and extra system design which are difficult so they are not easy to build and combine as single, unified system.

So the technic is enhanced for validation and it has to only analyze the system prototype, and not production test at end and its different type.

Failures are getting tougher to analyze on system level embedded devices. Full speed functional testing has to provide by a validation system.

Characterization and quick device debug are critical stages to take best competitive systems to market, and validation techniques are also wanted to yield a fruitful device design.

Engineering validation emphasizes on prototype testing, when the virtual electronic design model is prepared into an actual physical operational device. This not only helps to guarantee that the design works as aimed, but it may also enhance production, worth and reliability and give the design engineer a chance to drive a ground-breaking design.

It's significant also to remember that latest systems are operating at quickly growing clock and data rates, consequential in multi bus architectures that permit unlike sections of a device to well run at altered speeds. Latest test technology, such as routine benchmarking test instrumentation and the extra commonly used manufacturing test equipment, may be solid pressed to encounter the timing requirements of these new devices or propose at-speed, full-functional testing.

To concentrate on setting and characterizing specifications, not only confirming specifications. A digitally concentrated checking system gathers and shows altogether pin data, letting complete logic examination in single pass. Equipment speed path error may be checked and verified using sequence expand and contract tuning to the drive data. To check digital capabilities beyond the given specifications turns out in quick discarding and greater product bound.

When selecting a validation systems and tactics are commonly chastised in the essential to decrease design-cycle, test-cycle time, means and cost, these factors are considered. Cost, size, and ease of use, repeatable and traceable results, and the ability to link to EDA tools, and mobility these features we have to include. The system which permit instinctive and interactive exploration of proposed prototype and proposes the ability to correct and characterize fresh design immediately. It is essential that the technique should easy for usage, enhanced for the sort of testing required to test and confirm the systems. To assess the source EDA facts and formats, interpret this data into functional arranged data, and then permit this statistic to be simply deployed for "what-if" scrutiny the software tools should be capable off. This may help and enable fast decision building for engineers. So, overcoming above challenges we are characterizing Gigabit Ethernet switch designs according to various specifications for various features to its maximum working capability.

IV. DEBUGGING, FUNCTIONAL AND ENVIRONMENTAL CHARACTERIZATION OF GIGABIT ETHERNET SWITCH

Board bring up is a critical activity in a project plan. Board bring up involves testing the freshly assembled board to bring it to a working condition. Board bring up involves activities like Ohmic tests, supply checks, booting and basic functionality checks. Board has to function as per the desired functionality. If the board doesn't function as desired, then the user has to start debugging to find the root cause. One of the critical board bring up task is booting. It is a common issue seen across various projects that it takes time for the board to

boot up. First, testing a non-bootable board is nearly impossible unless the engineer has a complete command of the task in hand. Secondly, the time spent to debug boards is very critical these days considering the tight project timelines. In such a competitive electronics field, missing a project timeline is like giving competitor edge. To speed up these tasks there are several automated tools available in the market which are kind of essential these days.

One of the important product requirements is reliability. It has to work under desired environment with desired functionality with minimal of failures. Reliability is one typical factor which can't be judged. The only way we can be confident of product functionality without failures is by doing an extensive validation and verification. So, we generally expose the product to various environmental conditions throttling it to maximum functionality by which come to a conclusion on the reliable operation of the product. This is what we call characterization.

A. Challenges in Board Bring up and debugging

- Coming up with bring up strategy
- Dealing with freshly manufactured boards
- Dealing with dead boards that don't function after sometime
- Debugging and recovering dead boards quickly and cost effectively
- Categorize the problems encountered in dead boards and, at the same time, create a fast information feedback loop to correct problems on the fly
- Fixing the firmware problems
- Fixing the timing(clock) and control signal problems
- Dealing with undetermined faults.
- Using automation tools to reduce manual work

B. Board bring-up and Debugging

Dead board: -

"Dead" commonly denotes to a board that is not responding, initializing or power-up to a desired state.

Problem phases can normally be fragmented down into two groups: hardware and software.

Common hardware faults occur during debugging

1. Power related faults
2. Layout faults
3. Mechanical faults
4. Component assembly faults
5. Component faults
6. Timing problems
7. Control signal problems
8. JTAG connectivity issue

Gigabit Ethernet Switch Characterization over VPX Backplane

Common software faults

1. Code with Bug
2. Initialization of Memory
3. Overflowing of Stack
4. Code which Self-modifying
5. Programming the EEPROM

After Manufacturing, boards are available to test for working functionality. The sequence of steps that need to be followed to eliminate any board damage and help in smooth board bring up.

- 1) **Visual inspection:** Visually check for the correct component placement. This is done by referring the board schematic and comparing with the actual board in hand.
- 2) **Ohmic test:** Before powering on the board checking for shorts on the board is a must. This is done using multi-meter. Identify critical points on the board to check for the shorts.
- 3) **Voltage test:** Use current limit power supply which powers the board. Then switch on the power supply to check for voltages all over the board. Note that engineer has to do voltage test only after ohmic test.
- 4) **Firmware loading and Boot-up:** Cargo basic boot code and practical code (firmware) to test CPU and peripheral task.
- 5) **Debug:** After the above steps, check for the functionality of the board. If the board doesn't function as per the specifications start debugging the board. Debugging involves various checking procedures which individual user has own approach. There are lots of available tools that may help in the debug procedure, in that the most effective tool for the work saves engineering time. Knowledge of the tool helps to reduce learning time and improves productivity.

C. Functional and Environmental Parameters

Designed hardware functional testing is complete to confirm that the underlying design is capable to provide the wanted load and below desired environments. Hardware performance testing involves functional check, exposing the device under test to various environmental conditions as per the specification.

To understand key model bottlenecks and constraints hardware performance checking will help us. To gain a clear picture of optimal and end capacity performance Stress testing helps. These parameters will nourish into future capability tactics and approaches to confirm that the hardware is capable to retain pace with the requirement of the industry.

D. Functional testing of Ethernet switch over VPX Backplane

Challenges are abounding in the Ethernet switch when it is used in the VPX backplane. The inaccessibility of backplane makes the testing cumbersome. So, for that we

must have some feasible means for measurements (ex. RJ45 ports, fibre ports etc.). Performance test over backplane requires compatible equipment's for communication check. Identifying the critical points in a switch permits the growth of a test approach that may concentrate on checking these areas. The checking approaches should consider multi layers, and could consider for calculations:

Wire speed unicast data throughput and latency for Layer 2/3 traffic.

- The capability to separate packets at wire speed grounded on MAC, IP addresses, TCP or UDP ports, or a combination of these.
- The capability to achieve ordering grounded on QoS marks.
- The capability to observe and sort out traffic grounded on operator definite rate limits.
- The capability to handle Head of Line blocking (HOL).
- Wire speed multiple cast working test.

Test methodology example

Following is a sample of a test procedure for a Gigabit Ethernet ports switch that supports the following features:

1. Full speed Layer 2/3 (for IPv4) switching with a min packet size of 64 bytes.
2. Exchanging capability per slot that provides total port capability on line card.
3. Sorting grounded on ACLs.
4. QoS management grounded on 802.1p or IP Sort of Service (TOS) bits.
5. Priority planning grounded on weighted round robin (WRR).
6. Shaping of Traffic.
7. Routing protocols, comprising multi path.

The test procedure is fragmented out into modules and whole system testing. In the actual world, local switching on the module happens; this is the greatest case situation for switch checking, since there is no contention for the switch. The poorest case situation is while whole traffic ingoing the switch necessarily traverse the fabric, competing for backplane ability and instigating over-subscription.

Module-level testing

In this situation, traffic will stay local to the line card. This means that switching will occur locally between ports on the same line card, and minimal traffic will traverse the backplane.

System level testing

In this situation, all inflow traffic is moved to ports on different line cards. This says that traffic will be resisting for backplane capability and will find out how the system cares over subscription.

By setting partially meshed traffic shapes, by mapping one ingress port mapped to one egress port and multi ingress ports mapped to unique single egress port.

E. Test methodologies

Layer 2 two-directional throughput and latency test.

This test finds the DUT's max Layer 2 sending rate without traffic wastage in addition to normal latency for unlike packet sizes. This validation is carried out full duplex with traffic sending in both directions. The Device under test necessary to execute packet analysing and L2 address look-ups on the inward port and after that change the header beforehand sending the packet on the outlet port.

Layer 2 throughput, QoS, and latency test.

This test concludes the DUT's max Layer 2 sending rate with packet loss and latency for unlike packet sizes. The Device Under Test necessarily conduct a L2 address lookup, verify the 802.1p precedence bit value on the entering port, transmit it to the nominated queue, and after that change the header beforehand sending the packet on the outward port.

Requirements for functional testing of Ethernet switch over VPX backplane are mentioned below

- 1) Working VPX backplane
- 2) Availability of Usable ports
- 3) Availability of compatible devices
- 4) Preparing proper test plan and test setup

Availability of usable Ports:

To get usable ports to connect DUT with test centre or test equipment, we require designing test boards to get these ports in usable form on front side. But designing Boards is again costly. So, we have to use uncommitted chassis, where you can get all connection on backplane. For that we can design test card which fit in rear side on which we can get maximum number of ports and we can connect with Spirent Test Centre and we can test it for its maximum load and maximum performance.

Availability of compatible devices:

Once we tested the performance on uncommitted backplane we can say that board is working and later we can perform actual test on committed backplane. But for that we require compatible devices. For example, if we want to check Ethernet switch then we require at least two SBCs which are has Ethernet port and are compatible.

Preparation of proper test plan and test setup:

Some test Bench markings are suggested By RFC (Request for Comment) group for Ethernet switch testing. But all that bench markings are not possible or difficult to perform using available resources so we have to prepare appropriate test bench as per the available resources.

We already have seen significance of all functional parameters in literature survey. We will characterize switch for these parameters using Spirent Test Centre for functional testing.

F. Functional parameters

Functional parameters for which characterization of Ethernet switch required

Throughput:

Throughput is the measure of the data transferred successfully from one place to another in a given time period.

Latency:

Latency is the time difference between time at which input is applied and the time at which output is obtained. Latency in consideration of computer networking is time required to propagate through the network channel and adapter hardware and execution time of OS and application. It influences the time application which must wait for data to reach at its end point

Frame loss:

Whenever data traveling through medium it may get corrupted or due to network congestion packet may be lost. Frame loss is the number of frames lost during communication from one point to another

Data Integrity and Error checking:

It checks the DUTs presence to send frames for specific traffic rates without mortifying the payload. Frames are sent with a prespecified data form and they are checked at the end point to verify for the integrity of the frame.

Jitter:

Time required in inter-packet reach to their end point can be said as jitter. Jitter is definite issue that generally present in packet networks and jitter should not results into any communication trouble.

QoS functional test:

It counts the basic performance of the DUT using and short of QoS when outlawed traffic is inserted into the network.

Max load test:

At maximum load, DUT may give errors or packet loss or may stop working or get damaged due to heat dissipation so. At maximum load, for an Ethernet switch, packet loss, throughput, latency is observed.

Interoperability:

Interoperability is defined as range available from common explanations to extremely technical explanations that put on to exact types of system, software or hardware. For hardware it is real time pin to pin match and wrking match.

1000base-TX ports testing with 100m cable: 1000base-TX ports are designed to communicate through cat5e or cat6 cables over 100m distances.

G. Environmental Parameters

Temperature and Humidity

Humidity and Temperature verifications are a way of validating a products working in varying environmental circumstances. It is a way of verifying coatings as well as the working of electronic equipment under pre-found circumstances. Particular situations of temperature and comparative humidity can be utilized to depiction the DUT and check functionality. Specifications involve time of exposure, corrosion, and permissible corrosion per part. Commercial, Military and industrial specifications can be successfully assessed to confirm suitable analysis. Notifying characteristics of cabinet, time length, corrosion, permissible corrosion per part and per test, as well as commercial military and industrial are portion of standard functional checking specifications.

H. EMC / EMI testing-

- Emission
- Radiated Emissions

Either Class A (commercial areas, limit is 10dB higher than residential) or Class B testing (residential).class A i.e. for commercial areas limit is 10 dB higher than residential. Class B is residential environment testing. Characteristically checked from 30 MHz to 1 GHz and maximum is 6 GHz, checked in a chamber such as EMI/EMC Test Lab's chamber or on a test site which is open area.

Conducted Emissions

Class A or B, corresponding to testing the Emissions. It's noise which is put by Product back on the AC Mains over the power supply cord. Checked for 150 kHz to 30 MHz, and after this radiated emission puts at 30 MHz.

AC Power Line Harmonics:

Correlated to the power factor of the supply, we have to confirm that the supply encounters this beforehand we start verifying by obtaining their DoC (Declaration of Conformity) and EMI/EMC report.

Flicker Testing and Voltage Fluctuation

Typically, an environmental check to confirm that the designed product would not become reason for lights to "flicker" producing a possible health threat to people.

I. Immunity

Electro Static Discharge

In it we test for static charge which generated in human body and discharges in device when we touch the

device, it is more dangerous to electronic devices. It is modelled as the same static charge pulse declared by standards committee.

Radiated Radio Frequency Immunity

A cleared sent signal from 80-1000 MHz with modulation given to the carrier wave. This testing looks like intentional transmitter noise nearby or other another device that radiating noise in the surrounding of our device. It is observed in a chamber and we require method to observe if DUT is affected by applied noise, for this generally we are using monitoring software which is outside the chamber.

Fast Transients

Very first by tested by Military and named as "chattering relay test" it is a sequence of pulses inoculated through the power supply or straight into I/O cables that are 3 meters and lengthier.

Surge Immunity

Its aim to produce the pulses that, our power supply can realize if there is a lighting knockout nearby. Before starting CE, we have to ensure this.

Conducted Immunity

It is low frequency radiated RF immunity test. It is given to the power supply and I/O cables 3 meters and lengthier. It includes 150 kHz to 80 MHz. Radiated RF immunity test carried out over at 80 MHz.

Magnetic Immunity, power frequency

It tests device being near to a magnetic interference source like a power transformer. If device don't have magnetic sensitive part then this is not necessary.

Voltage Dips, Interrupts and Variations

Defective AC or noisy AC lines can generate the situations replicated in this test. Remove the plug of our device, when it is operating, and the device will not be damaged, we will pass part of this testing.

Thermal and Humidity Test

Producing a low cost power electronics system needs cautious attention of the thermal area also the electrical domain. Beneath designing producing the system may clue to overheating and still system breakdown. Discovering an enhanced answer needs a decent in-depth of in what way to forecast the working temperatures of the system's power components and in what way the heat produced by individual components causes effect on neighboring devices, like microcontrollers and capacitors.

In general, we do not want onboard electronics of any aircraft to fail. This is just one example of safety critical systems where high level of reliability is a must. The US Air Force study says Avionics Integrity Program in its about two-decade study that failure of electronics systems in almost 55% of all considerations was because of thermal issues. A typical failure mechanism which leads to thermal problems is when the thermal interface materials degrade.

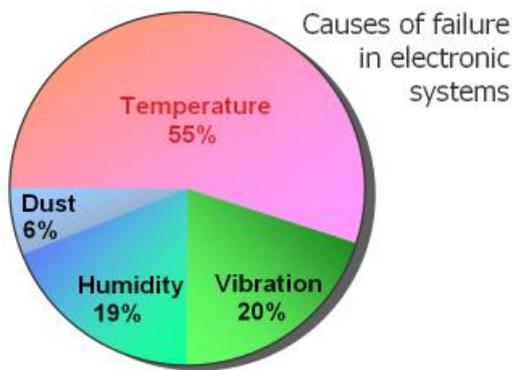


Fig. 4 Typical failure mechanism

EMI/EMC Test:

Performance of system may get degraded by Electromagnetic disturbance which is from part of same device or nearby device results into system failure is called electromagnetic interference (EMI).

Electromagnetic compatibility (EMC) is close accurate form in which a receptor (part of device or device) functions satisfactorily in general electromagnetic environment, deprived of familiarizing Unbearable electromagnetic trouble to other devices and system in surrounding.

Electromagnetic Compatibility (EMC):

The capability of device to work in its desired surrounding deprived of,

1. improper deprivation in working because of coupling to surrounding systems or
2. Producing improper degradation in the working of another system through coupling.

Emitter-Path-Receptor EMC model:

For complex device emitter and receptor may be independent systems or subsystem for the complex system.



Fig. 5. Emitter-Path-Receptor EMC model

From this EMI effect can be reduced in EMC model by

1. Reducing emission (emitter is Antenna)
2. Decreasing the coupling path efficiency.
3. Dropping the susceptibility of the receptor (Genius discrete IO module with daughter board).

Coupling path classification:

Conductive coupling:

Connecting cases and cables etc.

Precautionary measures for conductive coupling:

Common Impedance noise:

1. isolating op amp power leads at LF and HF
2. Lessen common-impedance
3. Abolish common paths

Methods to realize:

1. Small impedance electrolytic (LF) and local small value inductance (HF) avoids
2. Practice ground and power planes
3. Enhance system design

Radiative Coupling:

Not any conductive path is among emitter and receptor, receptor is present far away from the emitter and the emission radiation area which decays as $1/R$ where R is separation.

Inductive coupling:

No conductive path present among emitter and receptor, receptor is stand in close field of the emitter wherever the magnetic field is overriding and the immediacy of emitter and receptor causes to mutual coupling.

Precautionary measures for inductive coupling:

1. Cautious Routing of Wiring
2. Practice Conductive Screens for HF Magnetic Shields
3. Practice high Permeability Shields for LF Magnetic Fields
4. Decrease Loop Area of Receiver
 - I. Twisted pair wiring
 - II. Physical wire placement.
 - III. Orientation of circuit to interface.
5. Decrease Noise Sources
 - I. Twisted pair wiring
 - II. Driven shields.

Capacitive coupling:

No conductive path present among emitter and receptor, receptor is stand in close field of the emitter wherever the electric field is overriding and the immediacy of emitter and receptor causes to mutual coupling.

Precautionary measures for capacitive coupling:

1. Decrease Level of High dV/dt Noise Sources.
2. Practice suitable Grounding Schemes for Cable Shields
3. Decrease Stray Capacitance
 - I. Equalize input lead length.
 - II. Keep traces short.

Gigabit Ethernet Switch Characterization over VPX Backplane

III. Use signal-ground signal-routing scheme.

4. Practice Grounded Conductive Faraday Shields to Guard counter to Electric Fields.

Frequency Ranges:

Conductive Coupling:

Radiation Susceptibility = 0 to 30 MHz

Radiation Emission = 0 to 30 MHz

Radiative Coupling:

Radiation Susceptibility = 30 MHz to 2.7 GHz.

Radiation Emission = 30 MHz to 1 GHz

We will characterize switch for these parameters using Spirent Test Centre for functional testing, thermal chamber for temperature and humidity testing, Shock and vibration test chamber of shock and vibration testing and EMI/EMC chamber for CE compliance testing.

J. Functional Block Diagram of Gigabit Ethernet Switch

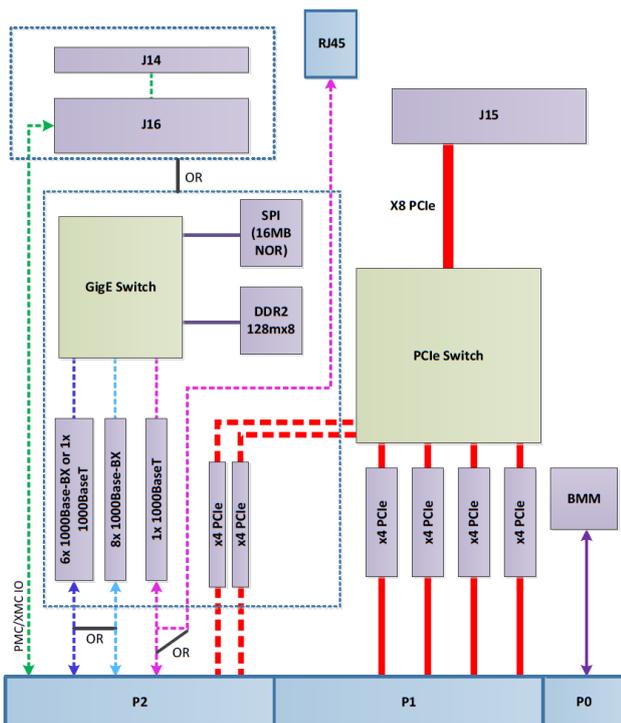


Fig. 6. Functional Block diagram of Ethernet switch under testing

V. RESULTS

A. Data Integrity, Error Checking and Frame Error filtering test

The basic arrangement for this test needs two test ports on Spirent and two test ports on the switch. Both ports send L2 traffic to the Device Under Test with a predecided data pattern with various frame size. The DUT collects the

traffic and sends it back to the same two emulated test ports to verify over two independent ports.

Spirent test parameters:

Table- I: Input parameters for Data Integrity and Error Checking Test and Frame Error filtering Test

Parameters	Description	Value
Frame Size	choose the frame size to utilize in the test	256B, 512B, 1024B, 1518B, 4096B, 9216
Traffic Rate	Start traffic rate that the sending port(s) will send	50% To 100%
Data Pattern	User chosen data pattern, for example All Ones	Fixed

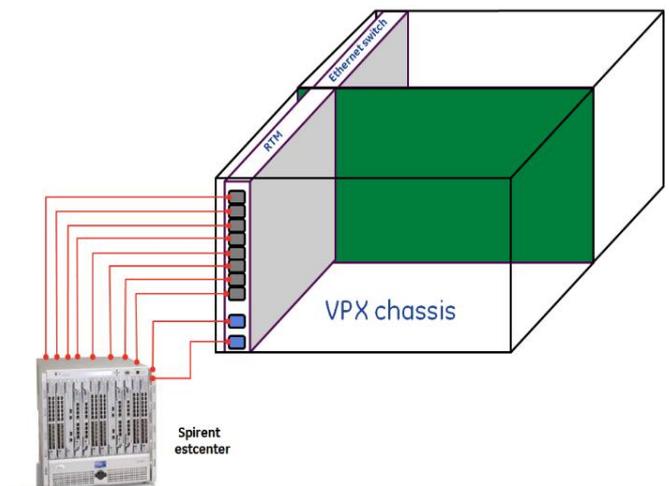


Fig. 7. Test setup

Test Methodology

1. Prepare set up to initialize the test with a preliminary traffic rate, e.g., 50% and then rise to 100%.
2. Configure for the suitable test parameters (Data Patterns, Frame size, and MAC address).
3. Carry out the test for stated period for each frame size. The traffic got by the Device under Test is accelerated back to the same sending test ports for examination. Under consideration test ports verify for the rationality of the frames and make sure data integrity on the payload and ordered frames examination.
4. Carry out the test again and again for various traffic rate from 90%, 100%.

Results

It shows that sent and received back to device under test with line rate of 50%, 60%, 70%, 80%, 90%, 95%, 99% and 100% displayed not any errors in frame sequence, data or traffic loss.

B. RFC 2544 Benchmark

Tests Methodology

Back-to-Back

Configure the test parameters for this test by referring table of input Parameters.

1. Initialize the test and carry out for every decided frame size.
2. It carries out the binary search to find out the lengthiest period the Device Under Test experiences in forwarding frames without any loss.

Frame Loss –

1. Select the test parameters for this test by referring the Input Parameters table.
2. Initialize the test and execute for all carefully chosen frame sizes. The test carries out a binary search for the uppermost traffic load that the Device Under Test can bear with the smallest frame loss.
3. As the test ends, record the frame loss values as both the frames size and the traffic rate changes.

Throughput –

1. Prepare test Set up and select Input Parameters by referring input parameter table.
2. Initialize the examination check and carry out for all frame sizes. The test does a binary check for the uppermost traffic load that the Device Under Test can bear with with the very good throughput.

Max load –

1. Select input parameters decide its values by referring input parameter table.
2. Initialize the test and execute for each frame sizes. The test accomplishes a binary search for the maximum traffic load that the Device Under Test able to hold with the optimize throughput.

Latency –

1. Fix the test measures for this test by referring input parameter table.
2. Choose the traffic rate for a comparatively small rate to confirm the minimum conceivable traffic loss and extra precise latency readings.
3. Initialize the test and execute same for each frame size. The test executes a binary search for the maximum traffic load that the Device Under Test able to bear with the smallest latency.

RESULTS: -

The Back-to-Back test gives the max number of frames that the Device Under Test is able to forward deprived of any frame loss for all the frame sizes.

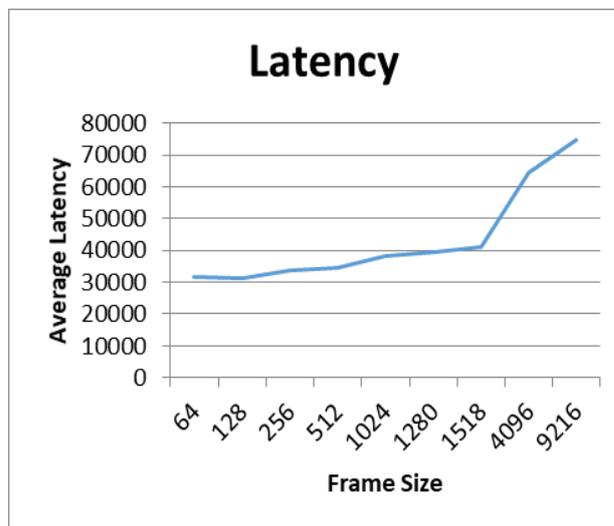


Fig. 8. Latency test

This test determines that frame loss is knowledgeable while the traffic rate surges overhead the 99% point, irrespective of the frames size and it is infrequent and extremely small and can be insignificant.

The Throughput check determines that the greatest collective throughput for the Device Under Test is observed while frame size is at a least of 64 Bytes. The consequences demonstrate the greatest traffic which is the Device Under Test is capable to forward deprived of some data loss for every of the frame sizes.

With max load test concludes that there is no frame loss and no error occurred.

The Latency test determines which the smallest average latency for the Device Under Test is detected while frame size is at a min of 64 Bytes size. The greatest throughput is illustrious while frame size is at a min of 64 Bytes size.

Stateless QoS Functional Test Objective

The intention of this test is to count the starting performance of the Device under test with and deprived of QoS while shapeless traffic is inserted in the network. Shapeless traffic is Layer 2 type and correct consumer application traffic does not emulate. The packet loss and latency get verified by this test the way out traffic port which degrade considerably when we enable QoS on the receiving Device Under Test. while QoS is deactivated on the DUT then take measurement and collect data is initial step. To measure and collect statistics after QoS with IP preference categorizing and enabling on DUT is second step.

Setup

Initial setup for this test needs four test ports. To produce Layer 2 traffic and connect to three ports. These links are well-thought-out the input ports to the DUT. Every port conveys a distinct flow using a exact IP Priority remarked value. The fourth test port is attached to a fourth DUT port to assess the egress network traffic grounded on the QoS service characteristics and settings.

Gigabit Ethernet Switch Characterization over VPX Backplane

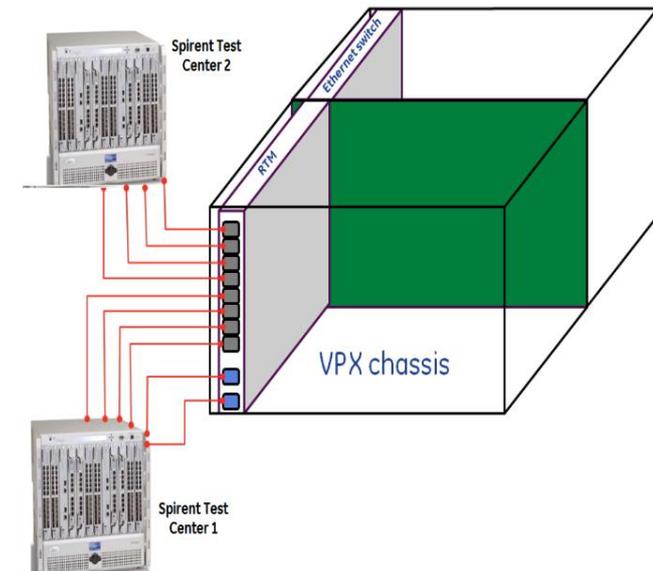


Fig. 9. Test setup for Stateless QoS Functional Test

Methodology-

TEST 1 – By disabling QoS on the DUT

1. Configure the network by disabling QoS on the DUT.
2. Configure the traffic rate for each type, consider Table 2 for input parameters for testing.
3. Initialize the traffic and simulate for the test duration. Received traffic by the DUT and isn't ranked or categorized.

TEST 2 – By enabling QoS on the DUT

1. Permit QoS on DUT and repeat the identical test.
2. Ingress traffic by the DUT is categorized, prioritized and treated consequently. The subsequent egress traffic port is observed for packet loss and latency.

Input Parameters

To run layer 2 QoS working test two groups of parameters are compulsory in prior. And one is for the test tool and another for the DUT.

Table- II: QoS Many-to-One Input Parameters Table

Parameters	Description	Value
Frame size	Random or fixed packet or frame size has to set	64,128,256,1024, 1516,4096,9216
Test Duration	Test duration we have to choose between seconds to hours	15min
Rate of traffic	For each priority level traffic rate	100% line arte
DUT-QoS	QoS administrative setting of DUT (disabled or enabled)	Shaping:-enable Non-shaping:-disable
DUT-Line Speed	The links speeds of the DUT ports	1000Mbps
DUT-QoS Type	DUT QoS type settings: COS, ToS IP Precedence, or DSCP	DSCP

DUT-QoS Policies	DUT QoS Policies applied to the ingress traffic	enabled
DUT-Queue Type	Stand in line mechanism such as Weighted Random Early Detection (WRED) and Weighted Round Robin (WRR) Queuing	WRED

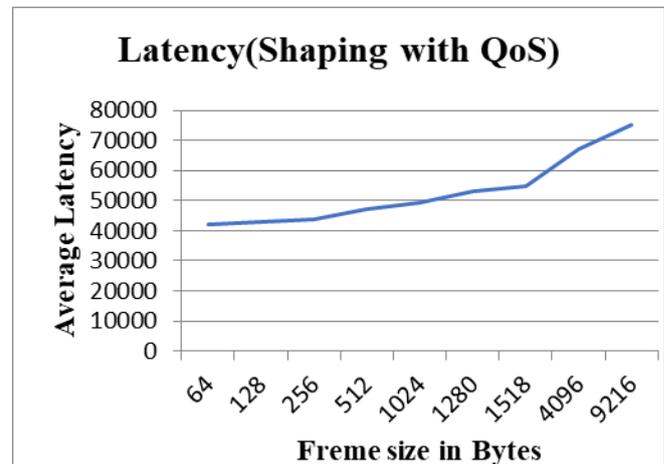


Fig. 10. Latency with quality of service activated

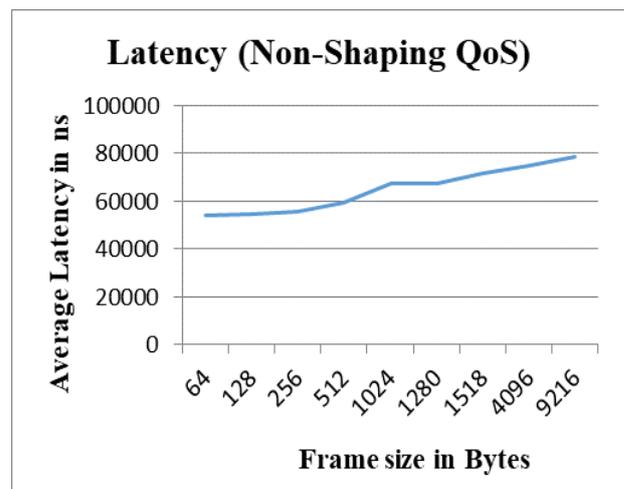


Fig. 11. Latency with quality of service not activated

The observation gives few packet loss but no fastidious order in latency is seen when QoS is disabled.

VLAN test:

Methodology-

- 1) Connecting port 1 and 8 to test centre
- 2) Set frame size to 128B and traffic rate to 90%.
- 3) Transferring data bidirectional from port 1 to 2 and 2 to 1

VLAN settings: -

Table- III: VLAN settings: -

Port no	VLAN ID	PVID
1,2	111	111
3-4	222	222
5-6	333	333
7-8	444	444

SETUP-

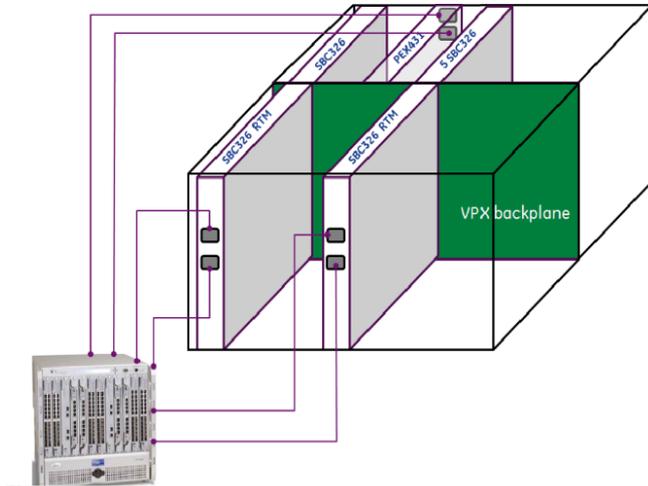


Fig. 12. Test setup for VLAN testing

We connect port 1 and 8 to test centre. We connect ports 2-3, 4-5, 6-7 using wires/cables and ports 1-2, 3-4, 5-6, 7-8 in VLAN providing different VLAN id and PVID

Results: -

With VLAN switch works fine without any data loss.

Actual 1000base-KX testing

Objective

Actual 1000base-KX testing means communication through backplane with compatible devices.

Methodology.

- 1) Connect switch and SBC's in their proper slots
- 2) Make proper configuration in switch
- 3) Update KX drivers for backplane Ethernet in SBC
- 4) Connect Spirent Test Centre.

Make setting in SBC's in such way that it will transfer data from one port to other without processing such as tunneled channel.

Setup

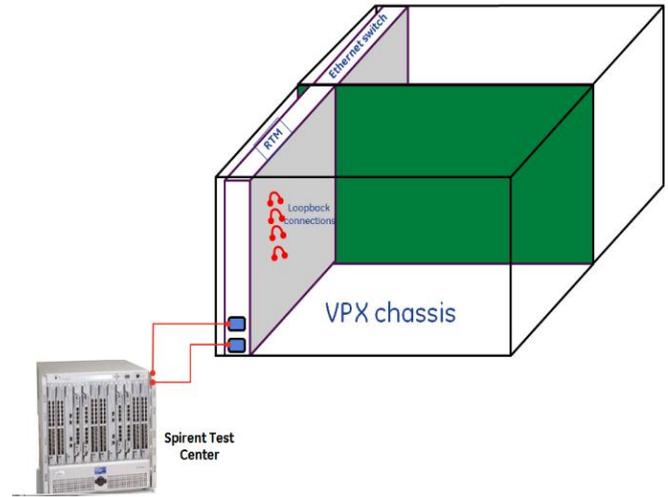


Fig. 13 Actual Backplane communication

Backplane communication is possible with 100% data rate.

C. Temperature and Humidity Testing

Test procedure:

Test procedure to verify the operation or functionality of the Ethernet switch is given in specification document. According to document to verify the operation or functionality at maximum temperature, store module at storage temperature 110°C for 16 hours and then run the functionality test according to temperature and humidity profile shown in below chart.

As per the document to verify the operation or functionality at minimum temperature store the module at -45°C for 16 hours and then run the functionality test for 3 hours at -40°C and to maximum +85°C Module.

Test setup-



Fig. 14 Thermal Chamber

Gigabit Ethernet Switch Characterization over VPX Backplane

We are using same setup which is used in VLAN testing, because from thermal chamber we can take minimum wires out so there is no chance of gap or external environmental effect.

For VLAN test we use different test card which has only two 1000base-TX ports and they are connected to Spirent Test Centre remaining are loop-backed and VLANed.

Temperature and Humidity profile:

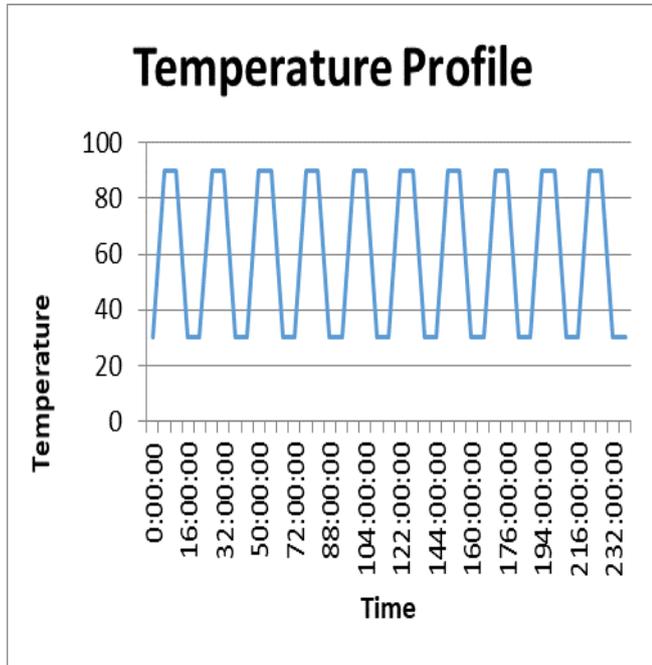


Fig. 15. Temperature Profile

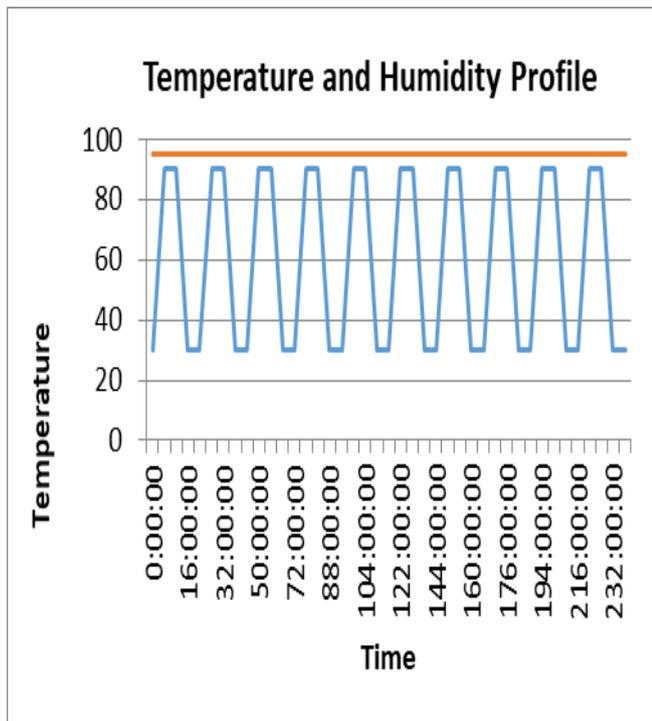


Fig. 16. Temperature and Humidity Profile

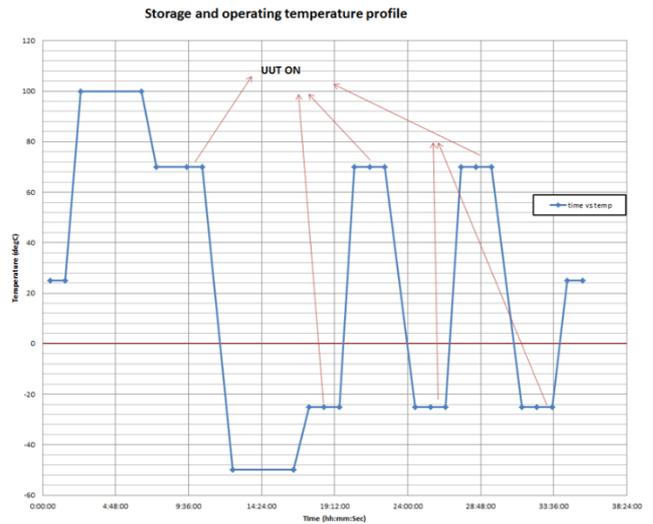


Fig. 17. Storage thermal test profile

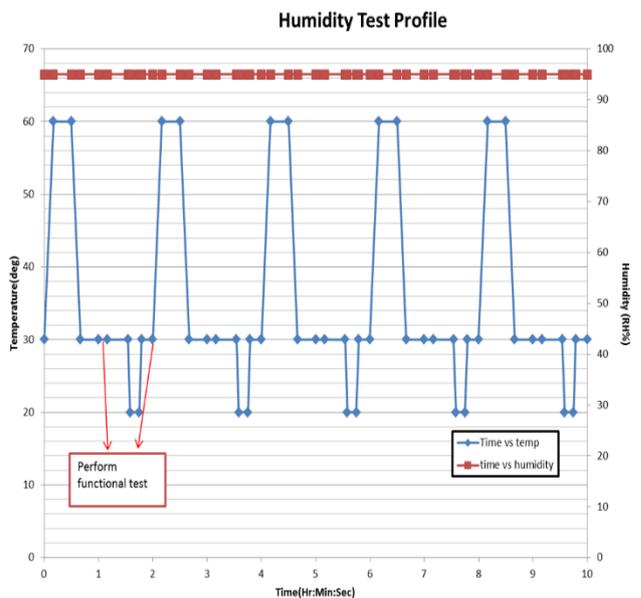


Fig. 18. Storage Humidity test profile

Result: -

We have completed thermal testing of PEX431 board successfully. An at all mentioned different environmental temperature and Humidity condition according to MIL-STD-810F PEX431 was functionally working as expected.

D. EMI/EMC Testing

Radiation Susceptibility Test, IEC61000-4-3, 80MHz to 2.7GHz:

In the EMI/EMC testing of DUT, a Pre-calibrated field was then imposed on the DUT to test the susceptibility of module for different frequency signal.

Setup diagram for Test:



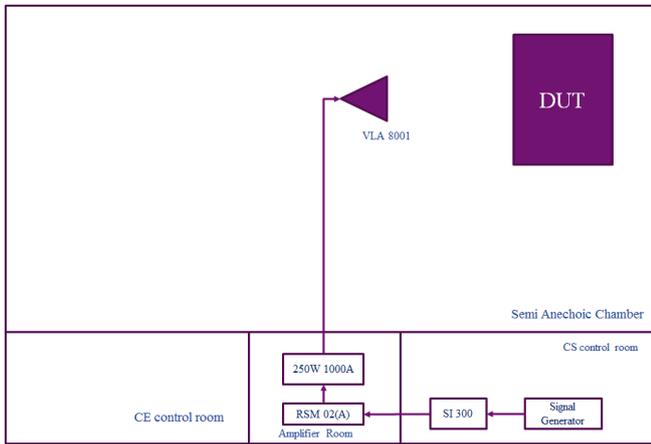


Fig. 19. RS Test Setup from 80 Mhz to 1Ghz

Test procedure:

- 1) Prepare the setup as shown in setup diagram.
- 2) Put DUT in VPX chassis and make sure that Power supply of chassis is CE compliance.
- 3) Configure all ports for bidirectional data transfer through cat6 cables.
- 4) Make sure hardware configuration is same as configuration in testing using cat6 cable and using fiber optic cable.
- 5) Configure all ports for bidirectional data transfer through fiber optic cable
- 6) Note down the readings for the DUT in both cases.
- 7) Repeat steps 5 & 6 for DUT and get readings and verify the result.

Applicable Standard: Test as per IEC 61000-4-3:-

1. Step Size: 1 %
2. Dwell Time: 2 sec.
3. Modulation: Amplitude modulation, 1 KHz, 80% depth
4. Field strength: 10 V/m, 80MHz – 1GHz , 3 V/m, 1GHz – 2GHz, 1 V/m, 2GHz – 2.7GHz

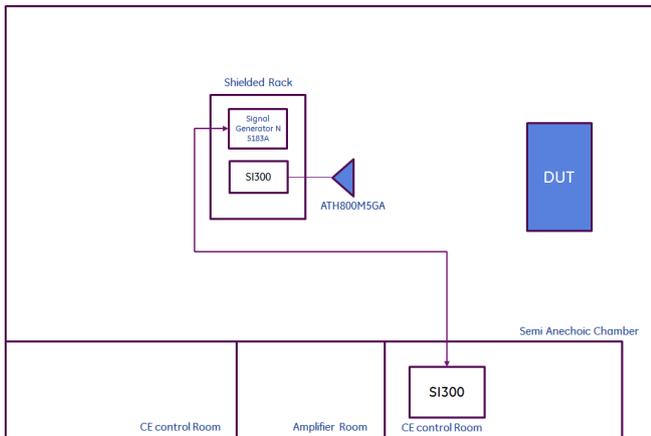


Fig. 20. RS Test Setup from 1Ghz to 2.7Ghz

Observations:

DUT functionality was verified remotely on Spirent Test Centre. No malfunctioning of module observed during & after the test.

Radiated emissions Test, CISPR 11, 30 MHz to 1.0 GHz:

Configuration and connections for RE Test:

Same as used for Radiation susceptibility test above.

Setup diagram for Test:

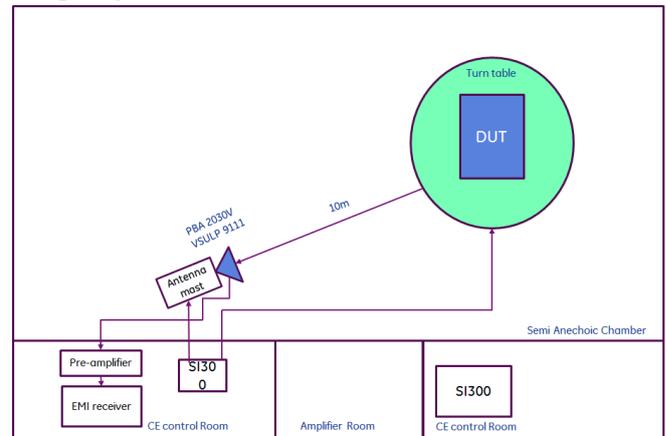


Fig. 21. RE Test Setup per CISPR 11,30MHz TO to1GHz

Test Procedure:

A preliminary scan was conducted with the peak detector selected at a 120 KHz RBW. The antenna was moved at stepped heights of 0.5 m from 1m to 4m. The turntable was rotated at steps of 45 ° from 0° to 360°. The observations for horizontal and vertical emissions are recorded in 2 (a) and 2 (b) respectively. A peak search was done and then a detailed scan was conducted at the identified frequencies.

The detailed scan entailed the use of a Quasi-peak detector. The selected frequencies are marked in the preliminary scan graphs by markers. The observations for quasi peak measurement are recorded in setup figure.

Difficulty during test:

While performing the test, in the first attempt the test was failed when the whole setup was near to module under test also the grounding was not proper for chassis.

Once we have isolated the setup from the module under test and kept under the ground surface, the failure at that frequency has been corrected but we were getting failure at other frequencies. Those frequencies suspected as the frequencies from power supply because power supply has some open-ended terminals. So, we have taken some other power supply and test passed successfully. Still for some of frequencies the field strength was just below 3 dB compared to level given by the CISPR 11, 30 MHz to 1.0 GHz, so we had kept whole setup outside the chamber and wires travelling from setup to module kept underground surface and test passed.

Result:

DUT functionality was verified remotely by observing data transfer on Spirent Test Centre. No malfunction observed during & after the test.

Gigabit Ethernet Switch Characterization over VPX Backplane

ESD Testing:

For ESD Testing Ethernet switch IEC 61000-4-2 standard is used. As per this standard the pulse waveform as shown in figure is applied and functionality of module will be analyzed. Also need to observe working of module during test whether it is failing or not.

If the module is failing during the test, analyze whether it is Catastrophic Failure or latent failure.

Table- IV: I/O Discrete module IEC 61000

Contact Discharge		Air Discharge	
Level	Voltage	Level	Voltage
1	2000V	1	2000V
2	4000V	2	4000V
3	6000V	3	6000V
4	8000V	4	8000V
X	Special	X	Special

Testing Steps:

- 1) Prepare the setup as shown in setup diagram.
- 2) Add target and modules required.
- 3) Prepare test setup and take cables at comfortable side.
- 4) Make sure hardware configuration is same as configuration is same as for full load test.
- 5) Note down the readings for the module.
- 6) Then replace test card with RJ45's with test card with SFP's

Repeat steps 5 & 6 for this module and get readings and verify the result.

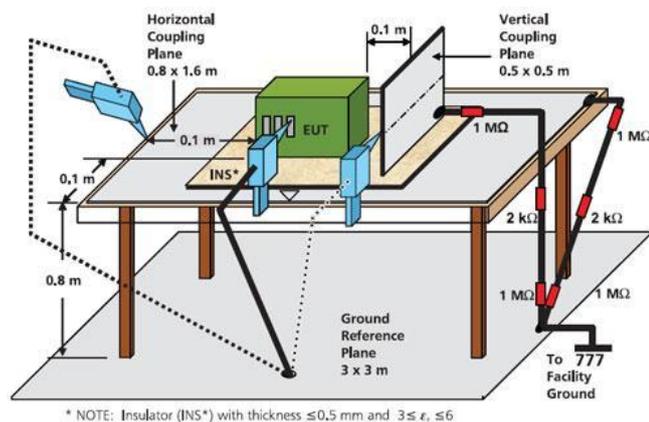


Fig. 22. Setup for ESD Testing

Difficulty during test:

While performing the test, in the first attempt the case of module was not properly grounded so module was failing during test after the application of high voltage pulse, this was latent type of failure. This failure was corrected by grounding it properly.

Results:

DUT functionality was verified remotely observing functionality on Spirent Test Centre. No malfunctioning of module observed during & after the test.

E. Power Consumption Testing

This test is carried out to check that board is consuming same power which is calculated at the time of design or it is consuming extra power than calculated.

Test Setup:

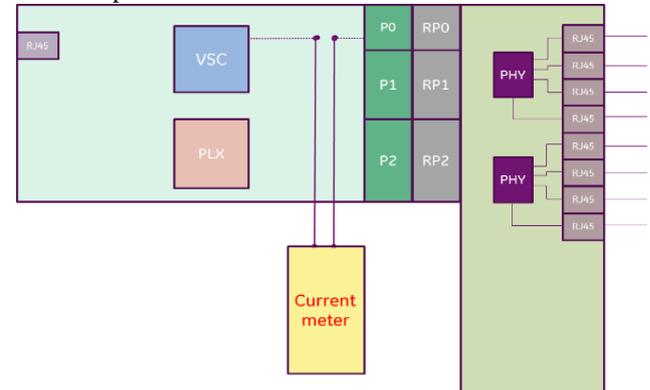


Fig. 23. Power consumption testing setup

Procedure-

- 1) Connecting all ports of the DUT to test centre and applying maximum load to the DUT.
- 2) Connect current meter in series with power supply and measuring current.

We know the voltage applied from that we can calculate power consumed by DUT.

Observations:

$$I(3.3V) = 4.35A \text{ and } I(1V) = 0.44A$$

Therefore total power consumed = $I(3.3V) * 3.3V + I(1V) * 1V$

$$P_{total} = 4.35 * 3.3 + 0.44 * 1$$

$$P_{total} = 14.79W$$

Result:-

Calculated power consumption at the time of design = 15W
Actual power consumption $P_{total} = 14.79W$.

VI. CONCLUSION

This paper includes the characterization and validation of design of Gigabit Ethernet switch over VPX backplane for its functional and environmental parameters. For functional testing Spirent Test Centre is used for packet generation and analysing packets. VPX backplane, gives large bandwidth and signal integrity so that we can communicate very efficiently through VPX backplane. For Ethernet different slot and module profiles are proposed by OpenVPX group which makes us possible to use switch with available and legacy backplane technologies with only small modification. All test results show that Gigabit Ethernet switch is working as per the specifications.



Designed Ethernet switch works satisfactorily with 100%-line rate and gives maximum data transfer rate. Maximum data transfer rate will get at large frame size, also switch supports Jumbo frame processing capability without fragmenting. In back to back test we characterize behavior of switch for busy traffic and for different frame size different no of back to back frames it supports without packet loss.

VPX backplane traces are less than 1m and to transfer data on this there is negligible propagation delay so measured latencies gives total latency due to Switch it includes receiving time, packet processing time inside switch fabric and transmission time.

Designed switch is Layer 2 managed Ethernet switch, when we turn on quality of services in Ethernet switch it transfers least priority packet after most priority packets and then low priority packets because of this waiting time of low priority packets increased. VLAN testing is also successful so we can form different virtual LAN's and we can configure ports in different logical groups.

In thermal testing Gigabit Ethernet switch module works satisfactorily from minimum at -40°C to +85°C. Humidity testing concludes that module works up to 95% humidity with 20°C to 60 °C.

Radiated susceptibility, radiated emission and ESD test are passed which gives assurance of switch board neither affect neighboring modules nor get affected from neighboring modules. It consumes approximately same power, calculated during design calculations.

Due to fast evaluation in Ethernet technology we can design multi gigabit Ethernet switch like 10G/40G/100G Ethernet switches which are communicating over VPX backplane. Also, fast advancement in semiconductor and PCB technology we can design very robust design which can sustain very harsh environments. Also, we can make these boards sustainable to vibrations also by providing good mechanical strength to board.

REFERENCES

1. VPX sub headline on second look. GE VPX short book.
2. VITA-42 specifications
3. VITA-42 specifications
4. IEEE Std 802.3 2012 (Revision of IEEE Std 802.3-2008)
5. IEEE Std802.3ap standards
6. Ethernet switching white paper – GE-IP
7. 802.3z and 802.3ae standards
8. VITA-46 specifications
9. TCP/IP Illustrated, Volume 1 by Kevin R. Fall and W. Richard Stevens
10. Interconnections Bridges Routers Switches and Internetworking Protocols, 2nd edition by Radia Perlman
11. VITA-65 specifications
12. RFC-2544 layer 2 and RFC-2889-layer 3 Ethernet switch benchmarking
13. The Internet Engineering Task Force (IETF) website
14. <http://www.ietf.org/>
15. Request for Comments website
16. <http://www.rfc-editor.org/>
17. LAN switching first step By Matthew J. Castelli. Published in 8th July 2004 by Cisco Press. Part of the first step series.
18. Spirent Test Centre, Packet generator manual
19. Air Force Avionics Integrity Program report on "failure of electronics systems in aircrafts"



AUTHORS PROFILE

Vinayak Kumbhar. Completed Bachelor of Engineering in Electronics and Telecommunication and M.Tech in wired and Wireless Communication. Now working as Assistant Professor in DKTES Textile and Engineering Institute, Ichalkaranji.



Lalita Admuthé. Received the M.E. and PhD. Degree in electronics engineering both from Shivaji University Kolhapur, India. Since 2013 she has been a Professor in Electronics Engineering at DKTE's Textile and Engineering Institute Ichalkaranji. Currently she is working as Dy-Director and Head of Electronics Engineering Department.



Institute, Ichalkaranji.

Vinod Kumbhar. Completed Bachelor and master of Engineering in Electronics and Master of Engineering in Electronics and Telecommunication. Now working as Assistant Professor in DKTES Textile and Engineering