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An Optimized FPGA Based System Design for the Arrhythmia Detection using ECG

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Abstract: ***Electrocardiogram signals are highly susceptible to interferences caused due to various kinds of noises including artefacts', disruptions in power lines attained from the human interferences and device disturbances. These noise signals tend to lower the quality of signals that result in crucial environment for detecting and diagnosing different types of arrhythmia. In order to avoid this issue, multiple filtering techniques are being incorporated out of all Gaussian filters with Haar DWT portray better outcomes in noise elimination and smoothening of signal. The process of ECG signal filtering allows performing the testing and validation of in the actual world emulation. Enhancement in PSNR ratio is observed by using the ECG signal filters along the reconstructed signal. For a given input ECG signal, the levels of the signal peak decide if the patient is suffering from arrhythmia or not. If peak is low, patient is detected with the arrhythmia disease, if high patient is normal. The results can be observed in simulation. FPGA prototyping of the design is carried out along the hardware debugging in chip scope pro tool. The design is realized using Verilog coding with the technique of morphological filtering. For the purpose of debugging the hardware device used is Artix-7. The FPGA methodology is success full in a position to detect arrhythmia. The framework based on FPGA is structured and executed in the paper which can detect a type of arrhythmia which indicates Atrio Ventricular block along with all the noises removed. The simulation results are obtained by taking ECG signals from MIT-BIH arrhythmia database. The proposed FPGA based system design is proven to be optimized as it showed very less utilization of resources when compared to previous arrhythmia detection system designs.***

Index Terms**: *Arrhythmia, Atrix-7, FPGA, Haar DWT, Morphological Filtering***

I. INTRODUCTION

The heart disorders are proven to be the major cause of death, identifying these heart defects at the earlier stages helps the physicians to save number of lives. Any heart defects found undiagnosed proves to be fatal. The simplest way of identifying any abnormalities in the heart is by visualization of the recorded Electrocardiogram by the physicians. The term Electrocardiogram (ECG) in medical science represents the biological electrical activity of human heart.

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This signal has been used as an important parameter over the years in diagnosing the cardio-vascular diseases and in determining the stress levels of a person. The Three basic techniques are used for measuring ECG, one is the standard clinical ECG, second is the vector cardiogram (VCG) and third monitoring
ECG. In the clinical method, the ECG is measured through 12 different potentials from the leads attached on patient's body surface. The monitoring of ECG used for long term monitoring of heart rhythm in intensive care units using one or two leads. This approach of ECG is also termed as arrhythmia analysis. A single heart beat is characterized by P, QRS complex, ST and T waves [1] as shown in "Fig.1,"

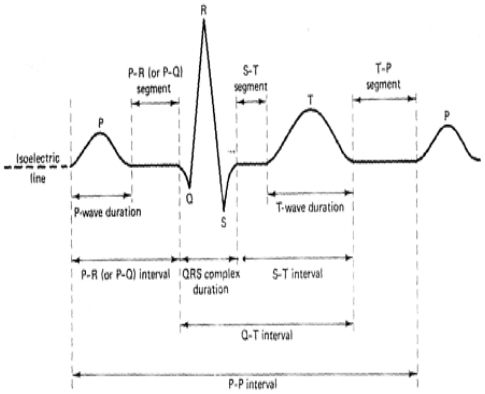

Fig.1 A Typical ECG beat [1]

As shown in the "Fig.1," each segment of ECG represents a particular physiological condition, the visual inspection and analysis of these segment duration is the aid used by physicians in detecting any disorders. To extract this information for machine analysis the recorded ECG signal need to be processed, the ECG signals are very low frequency signals in the range of 0.05 to 100 Hz and are always accompanied with different noises namely baseline wander, power line interference, muscle noises, these noises creates problems in interpreting the lower amplitude signals. The noise reduction is thus an important part of ECG signal processing before analysis or interpretation [2]. Among the noises the baseline wander, power line interference are removed by linear and polynomial filtering but the muscle noise cannot be removed by filtering process due to spectral content overlap with the PQRST complex. An ensemble averaging method is preferred by the researchers for removing this type of noise [3]. Cardiac arrhythmias are the disturbances present in the heart rhythm resulting in fast heart rates or slow heart rates that is abnormal heart rate.

This is considered as a serious problem because when the heart rate is not normal it cannot pump effectively. This can have a gradual effect on other vital organs in the body such as brain, lungs etc. Hence such arrhythmias have to be diagnosed and treated successfully. Various arrhythmias [4], [5] conditions include Sinus Bradycardia, Sinus Tachycardia, Atrial Flutter, Atrial Fibrillation, Ventricular Tachycardia, first degree atrioventricular block, second degree and third degree block. Certain Patients with arrhythmia conditions show the symptoms but some of the patients do not encounter any such physical symptoms nor may they be found by diagnosing a single snapshot of an ECG signal. The diagnosis of such arrhythmias requires a continuous monitoring of the heart electrical activity via Electrocardiography. This requires the patient to be in ICU conditions for longer periods. To avoid this circumstances a automated detection system is thus required for identifying the arrhythmias in real time and start with the treatment procedures quickly. The objective of the study is to design and develop the arrhythmias detection system for ECG signaling using Haar wavelet transformation and morphological filtering based on FPGA. To simulate, implement new architecture based on FPGA and test with improved design constraints like area (slices and LUT's), operating frequency, power consumption, and compare the proposed design with previous architectures. The paper focused on the design of improved FPGA based automated arrhythmia detection system mainly a second degree atrio ventricular block which is characterized by the dropped heart beat. The improvement is with respect to the utilization of resources in the construction of hardware.

II. REVIEW OF LITERATURE

Chazal et al. [6], implemented a technique for the automated processing of Electrocardiogram (ECG) signal for the division of heartbeats. The technique designates physically recognized heartbeats as five beat classes prescribed by ANSI/AAMI EC57: standard, i.e., typical beat, Supra-Ventricular Ectopic Beat (SVEB), Ventricular Ectopic Beat (VEB), combination of an ordinary and a VEB, or unusual beat type. The MIT-BIH arrhythmia database is considered which was divided into dataset with individual dataset having around 50000 beats from 22 recordings. Feature sets were depended on pulse intervals, ECG morphology, and RR-intervals. The evaluation brought about affectability in sensitiveness of 75.9%, a positive predictivity of 38.5%, and a positive rate of 4.7% for false condition of SVEB class. For the VEB class, the affectability was 77.7% whereas that of the positive predictivity was 81.9%, and the positive rate was 1.2%. Kazakeviciute et al. [7], focused on the programmed EEG spike recognition technique that is based on morphological filtering method. The parameters considered for distinguishing are shape, count, area, time of spike occurrences.

The work of Zhang and Lian [8], demonstrated a novel framework of Electrocardiograph (ECG) algorithm for detecting QRS in case of ECG devices based on multi-leveled morphological filtering used to eliminate the effect of impulsive noises. The framework also utilizes modulus accumulation units derived from multi-frames. Arrhythmia database with the wearable ECG devices, attains a mean QRS detecting rate of 99.6% with a sensitivity of 99.81% and finally the percentage of positive prediction to be 99.80%.

The study of Ghorbanian and Ghaffari [9], indicated an algorithm that is responsible for categorizing six kinds of Electrocardiogram (ECG) signal beats. The study concentrates over utilizing the neural networks for ECG beat classification. Many stages of pre-processing are involved that indicate the usage of most suitable input vector for the operation of neural classifier. The benefits of the proposed work are that with extreme ease the differences among the various kinds of ECG signals are fore grounded along with extracting there features prominently.

Apart from this, another advantage of the presented work is the minimization of data dimension by applying suitable vector for classifying the neural networks for it. The observation of Chan et al. [10], showed that pulse identification is essential for recovering the important functioning of heart capacities. The inter-based intervals and the morphologies of the heartbeats can reveal the heart contraction condition. Here, a scheme was developed to incorporate combination of heartbeat data that could deal with the data obtained from template match methods and energy thresholding techniques. The scheme would perform the function of generally distinguishing the QRS match and heartbeat, individually. The proposed scheme is simulated in SIMULINK 2.0 and for its assessment MIT/BIH arrhythmia database is used. The outcome showed exceptional affectability of recognizing QRS and premature contraction of ventricles.

Zheng and Huang [11], suggested the implementation of a DWT and Multi-Resolution Analysis (MRA) in the domain of homomorphic encryption. From the proposed method, the multi stage DWT/IDWT can be conducted with lesser expansion towards the homomorphic domain of encryption. A new signal procedure is suggested in the work that expands data in the final step of restricting it. The case study of a 2-D Haar wavelet transformation is investigated to initiate secure processing of data. Audithan and Chandrasekaran [12], study the implementation of an effective and high computational speed persisting method that could extract the regions of text from a present document. The study stresses over introducing Haar DWT that has the fastest operational speed when compared to all the other wavelets as it has coefficients either set as -1 or 1. The technique of Haar Wavelets is used to detect the edges of the specific regions, the proposed work suppresses the false alarm triggering prominently.

Vijendra and Meghana [13], observed that ECG signals are exceptionally suspicious on various kinds of noise artifacts, obstructions in the power line acquired from Instrumentation attenuations and human hindrances. These disturbances attenuate the quality of the signal, which is used for diagnosing different kinds of arrhythmias. To overcome this issue various techniques of filtering are being included, out of which Gaussian separating in Haar DWT wavelet change demonstrates the better outcomes in smoothening the signal and eliminating the noise.

The data input attained from MIT-BIH Waveform Database (WFDB) to guarantee the Co-recreation information execution utilizes MATLAB Simulink. The execution of hardware is completed utilizing Xilinx Spartan-6 FPGA Kit. Rajpurkar et al.[14], developed an algorithm that functions in exceeding the performance of evaluating the massive volume of arrhythmia attained from electrocardiograms, recorded by a monitor that has a single-lead. A dataset is collected that consists of about 500 times the total count of identical patients that the previously created datasets. Over the dataset a 34- layered neural network is trained that aids in the mapping of sequences to ECG samples towards a sequence classes of rhythm.

Lobodzinski and Laks [15], introduced a new device for long-term ECG monitoring called as the Patch ECG monitors (PEM), permitting the clinicians to detect arrhythmic events with an improvisation. The potential constraint of these devices is the measurement of the problems with artifact immunity and their capability to reduce discernable QRS when the noise is present. Nasiri et al. [16], presented a new approach for classifying arrhythmia disease. The methodology is a combination of both Genetic algorithm methods and Support Vector Machine (SVM). Initially, electrocardiogram signal is processed under extraction to gain twenty two features. The experimental outcomes revealed that the presented approach classified better ECG signals. There were four kinds of arrhythmia distinguished from one another with about 93% of accuracy.

In the work presented by Alonso-Atienza et al. [17], showed that early discovery of Ventricular Fibrillation (VF) and quick ventricular tachycardia (VT) are critical for accomplishing the defibrillation treatment. In this work, the novel framework of crucial arrhythmias detecting algorithm that is the combination of various proposed ECG parameters by utilizing Support Vector Machine (SVM) classifiers are utilized. A total count of 13 parameters was held for computation representing temporal, complex and spectral characteristics of ECG signal. The outcomes show that combining of ECG parameters utilizing statistical learning theories enhances the efficiency for the detecting crucial disease of arrhythmias.

Kanhe and Hamde [18], showed that the study proposes an ECG compression method utilizing discrete Hermite characteristics. The ECG signals are distributed over the discrete Hermit function allowance and the 2-D wavelet compression is accomplished. The regeneration of the signals is acquired by applying the reverse 2-D wavelet transform with maximal likenesses in the indicative characters. The consequences of the compression technique are verified by the utilization of the standard execution measure, for example, the Normalized Cross correlation coefficient (NCC). Compression Ratio (CR), Percent Root mean square difference (PRD) and Compression Ratio (CR).

Martinez et al. [19], assessed a single-lead ECG framework in view of the wavelet change (WT). The complex of QRS is detected and the database considered for the study include MIT-BIH Arrhythmia, QT, European ST-T and CSE databases, were proposed for approval. The sensitivity measured from the QRS detector was found to be 99 66% and a positive predictivity value of + = 99 56% on the main lead of the approval databases (greater than 980,000 beats), whereas in case of notable MIT-BIH Arrhythmia Database, and greater than 99.8% was achieved.

Meddah et al. [20], discussed about the QRS complex detection is seen as a basic component to identify heart disease-arrhythmias. In this study, a constant plan executed on FPGA to display the QRS complexity algorithm identification. For optimal execution on FPGA, the study tends to adjust the PAN and TOMPKINS calculation. A measurable report on the database MIT BIH, gives a decent precision rate, utilizing a 56 % of the assets in the FPGA Virtex cx5vlx50t card.

Tripathi and Ayub [21], in his proposed work, found the recognizing capability of arrhythmias in heart rate changeability view. Heart rate changeability in typical ECGs and arrhythmias are identified by taking five ECG pulses from every ECG into consideration. The RR interval is investigated to identify heart rate changes in Arrhythmia. It is discovered that in arrhythmia, continuous RR interval in peak differs, while in typical ECGs, RR peak interval is relatively steady. Heart rate variations are observed as in ordinary ECGs are up to 7.5%.

Besrour et al. [22], presented a strategy for R wave's areas utilization over the investigation of multiscale wavelet. The basis for the proposal was Mallat's and Hwang's approach for recognition by means of signals respective to wavelet coefficients. Incorporating the Gaussian function's first derivative in the form of model wavelet, the point-wise result of the wavelet coefficients (PWC) are applied over some scales progressively, keeping in mind that amplitude has to be maximized correspondingly with reducing the noise. By utilizing this technique, the recognition rate of R wave is over 99.91% for the MIT-BIH and 99.97% for QT database.

From the literature it is found the automated system for the detection of arrhythmias is based on the detection of QRS complex and the accurate identification of QRS complex is a tedious task as the recorded ECG signal is affected by different noises among which the major ones are power line interference and baseline wandering noise, hence the removal of these noises is a important step for detecting arrhythmias. The challenge lies in the design of efficient filtering technique which removes the noises without effecting the signal shape and spectral characteristics. And to design cost-effective algorithm which can detect QRS complex effectively which is used to detect arrhythmias.

III. DESCRIPTION OF THE SYSTEM DESIGN

The various stages involved in the automated detection of arrhythmias is depicted in the "Fig.2,"

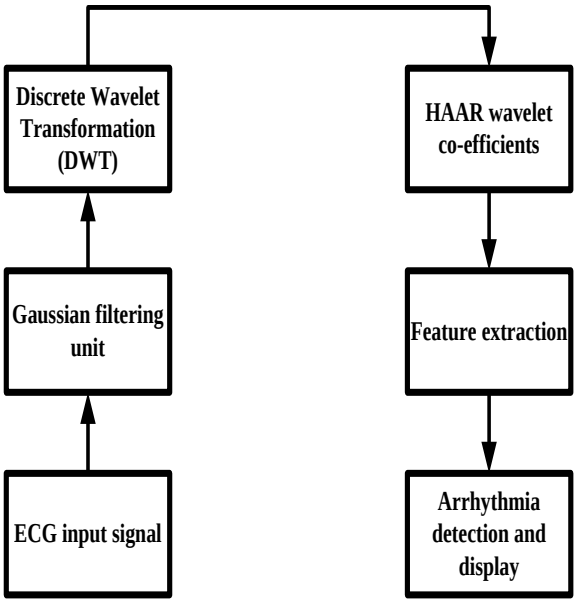

Fig.2 Block diagram illustrating ECG signal pre-processing stage and arrhythmia detection

To initiate improvement in the quality of survival, the role of health care is vital. The high cost relevant to the health care issues tends for developing new services all over the world. A non-invasive method the electrocardiogram (ECG) is successful in diagnosing the diseases related to heart. The ECG signal analysis process involves removing the noises corrupting the signal, detect the R peaks by detecting QRS complex to found the beats and to extract the ECG signal amplitude, duration characteristics for analysis in detail. The signals of ECG are combined with various type of noises originated from various sources including electromagnetic fields and physiological process. The noises are not just restricted to the baseline wanderings, artifacts corresponding higher frequency range, along with other signals generated by the human body. The most usual sort of disturbance is the Power Line Interference (PLI). This is the power line that consists of noise signals containing 50Hz sinusoidal signals and its harmonics. A baseline wandering is caused in the human body recorded in the form of ECG signal kinds. All these noises affect the signal and in certain cases the signal required may be lost, hence it is very much required to preprocess the signal before analyzing the ECG signal.

The main task involved in the preprocessing stage is to remove these noises using suitable band pass filters. The baseline wandering noise of frequency range 0.5 Hz is removed by using a linear time invariant high pass filter, linear and band stop filter is used to remove the power line interference noise. The next step after the preprocessing stage involved in signal analysis is QRS complex detection which detects the required heart beats in which first the QRS complex is enhanced and noise components are suppressed, the QRS complex is enhanced using linear filtering and non linear transformation methods. Once the R peaks are detected the other morphological features such as P, T and other components are delineated. The individual feature of ECG which includes PQRST are characterized and described with the aid of three parameters using Gaussian filter which includes amplitude (ai), phase (θi) = 2π/ti and width (bi) . The displacement of the ECG signal vertically is z, is defined by "(1),"

$$Z(a_i, b_i, \theta_i) = \sum_{i \in P,Q,R,S,T^-,T^+} a_i \Delta\theta_i e^{\left(\frac{-\Delta\theta_i^2}{2b_i^2}\right)} \quad (1)$$

Where the value of θi=(θ-θi) is known as the relative phase. There exists no z-offset for model-fit assuming z=0, enabled at an iso-electric stage. The ECG waveform is extracted by numerically integrating the above equation using sets of ai, bi, θi [23]. Extracting the features of ECG signals, plays a vital role in the task of diagnosing arrhythmia. Each cardiac cycle of an ECG signal comprises of P-QRS-T waves. The extraction of features determines the human heart functioning in terms of interval levels and amplitude. The ECG waveform extracted using "(1)", is as shown in "Fig.3,".

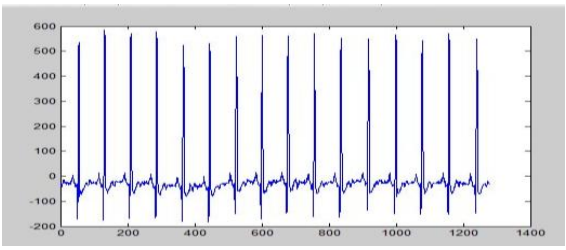

Fig.3 Extracted ECG Waveform

IV. METHODOLOGY

The FPGA based arrhythmia detection system consists of morphological filtering, Harr Discrete wavelet transform filtering, thresholding and comparator stage. The proposed system design for arrhythmia detection consists of following operations morphological filtering, DWT filtering and Thresholding. The design of the proposed arrhythmia detection system "ECG_AD_module" is developed to incorporate all the above operations.

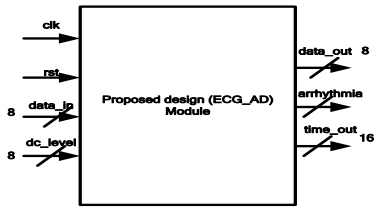

Fig. 4.1. The top level view of the proposed ECG_AD_module

The "Fig.4.1," shows the top level design of the proposed "ECG_AD_module" which takes in the 8-bit digitized input ECG signal and the 8-bit dc_level signal. The clock and reset signal are the other inputs to the top module. The outputs from this module is the 8-bit data_out signal lining the "QRS" peak detection, the 1-bit arrhythmia signal indicating the arrhythmia condition and the time-out indicates the period of QRS peaks.

The internal architecture of the proposed "ECG_AD_module" is designed as shown in "Fig.4.2,". The design starts with the morphological filter module which processes the input ECG signal. The processed ECG signal is forwarded through a series of DWT filtering module to extract the significant higher frequency components. These higher frequency ECG signal coefficients acts as important features in the detection of arrhythmias. The filtered coefficients are passed through the Thresholding module for presence of QRS peak detection which are helpful in predicting the presence of Arrhythmias.

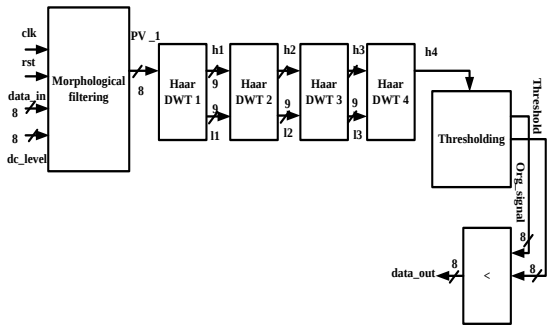

Fig.4.2. The internal architecture of ECG_AD_module

The signal flow for the entire architecture starts with the flow of 8-bit ECG signal and the 8-bit dc_level signal. The filtered 8-bit ECG signal is then passed through Haar DWT filters to generate a 9-bit higher(h1,h2,h3) and lower(l1,l2,l3) signal coefficient signal. The final block of this DWT filter bank generates a higher coefficient signal h4 which serve as input to the thresholding block. The Thresholding block generates the 8-bit original signal org_signal and the 8-bit output Threshold signal which are fed to a comparator module to produce a 8-bit data_out signal.

The top level design of the morphological filtering block is shown in "Fig. 4.3,". The clk and reset signals serve as basic inputs to the block. The ECG signal is input as 8 bit data_in and the thresholding reference input as 8 bit dc_level signal. The morphed ECG signal is output from the module as an 8-bit data-out signal.

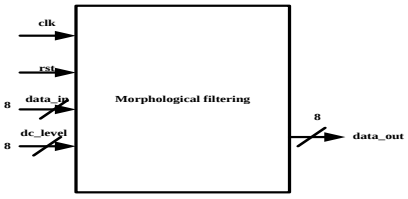

Fig.4.3 Morphological filtering module

The internal architecture of the morphological filtering process is discussed as in the "Fig. 4.4," below.

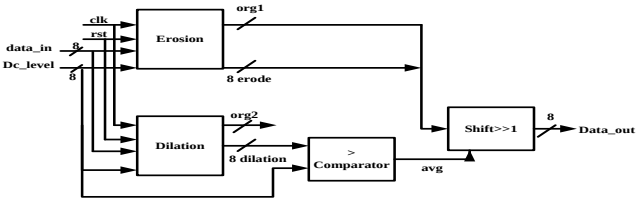

Fig.4.4 The internal morphological filtering blocks

The morphological module comprises of the erosion and dilation operations. The 8-bit input ECG signal is fed to the erosion and dilation blocks in parallel. The two functional blocks generates two output signals original signal and the erosion or dilated signal. The erosion output is an 8-bit erodde signal and dilation output is an 8-bit dilation signal. The dilated signal is compared with the dc_level value input using a comparator module. This comparator module generates the average signal. The average signal and the original 1 signal is then added and shifted to the right by the shifter module to generate the morphed ECG signal that is an 8-bit data_out.

The top level view of the Haar DWT filtering is shown in "Fig.4.5,". The inputs to this module are the clk, reset and the 8-bit data_in signal. The block extracts the higher an lower frequency components from the ECG signal which are output from this module 9-bit high_out and 9-bit low_out signals respectively.

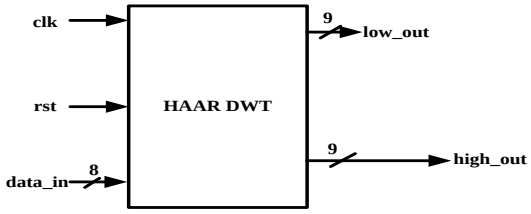

Fig.4.5 Top level view of Haar DWT.

The operational blocks required for implementing the HAAR DWT is as shown in "Fig. 4.6," The architecture is split into two levels HAAR level and the Add-sub level. The data _in signal is fed to the Haar level which generates the LL_out and HH_out signal. These two signals are fed into the Add_sub level to generate the 9-bit low_out and 9 bit high_out signal.

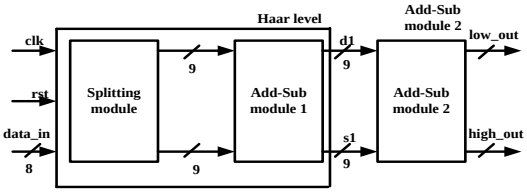

Fig. 4.6 Internal Architecture of Haar DWT

The Haar level DWT which forms the part of DWT filter is shown in "Fig. 4.7,". The data_in signal is input to the block to generate the low low coefficients ll_out and high high coefficients hh_out.

Fig.4.7 top level view of Haar level DWT

The functioning of the Haar level module is done using two modules. The splitting module and the Addition subtraction "Add-Sub" module. The splitting modules perform the separation of even and odd components of the incoming ECG signal. The separated even and odd signal is then fed into the Add-Sub module to get the LL_out and HH_out signal.

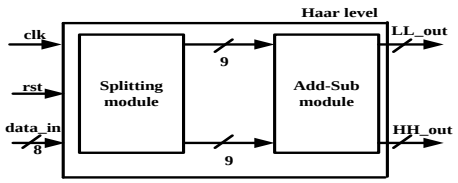

Fig. 4.8 Internal modules of Haar level

The clk and reset signal are fed to the splitting module along with the 8-bit data-in signal to generate the 9-bit even and odd signal components.

The top level view of the Add-Sub module is shown in "Fig. 4.9," The even and odd signal components produced from the splitter module is fed here as inputs. The module generates the 9-bit output signals predict and update.

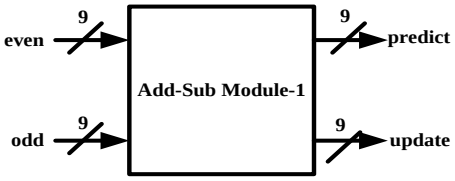

Fig.4.9. Top level view of Add-Sub module.

The internal operational blocks for the design of "Add-Sub module" comprises of a subtractor module, the shifter module, the concatenate module and the signed adder module. The architectural details of the Add-Sub module is shown in "Fig.4.10,".

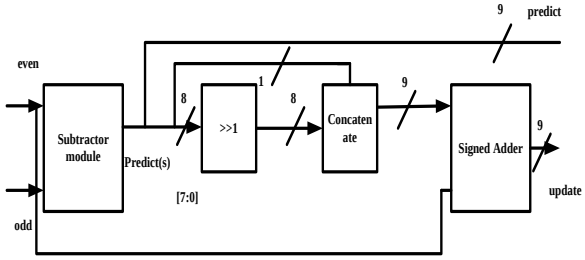

Fig.4.10 Architectural details of "Add-Sub" module

The even and odd signal components are input into the subtractor module which generates the difference signal between the odd and even components. The difference signal is termed as 8-bit Predict signal. This predict signal is passed through a shifter block where the right shift of the predict signal is performed. The right shift operation is similar to the division operation by 2. The division operation is then followed by a concatenation operation in the "concatenate module" where the right shifted prediction signal is concatenated with the normal prediction signal. The result of the "concatenate" module is then fed to the "Signed Adder" module along with the even signal. The output of this "signed adder" module is the update signal.

The top level view of the second addition subtraction module "Add-Sub" module is shown in "Fig. 4.11," with inputs taken from the previous "Add_sub 1" module. The inputs to this block are 9 bit signal termed d1 and s1. The signals are taken and processed by this block to generate the 9-bit d0 and s0 signals.

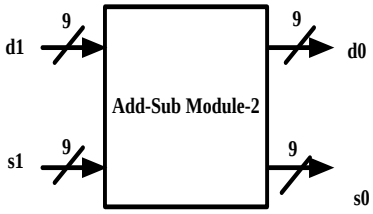

Fig. 4.11 Top level view of Add-Sub module.

The operational blocks required to implement the "Add-Sub module-2" block are shifter, subtractor, concatenator and signed adder as shown in "Fig. 4.12,". The input 9-bit d1 signal is split into 8bit and 1-bit signals. The 8-bit signal is right shifted once by the shifter block and the shifted result is concatenated with 1-bit signal to generate the 9 bit signal. The 9-bit concatenated signal is subtracted with the s1 signal input. The result of this "Subtractor" module is forwarded to the "Signed Adder" block which perform signed addition of the d1 input signal and "Subtractor" module result. The result of this block is the 9 bit d0 and s0 signals.

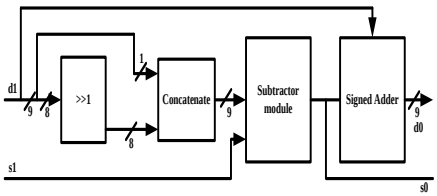

Fig. 4.12 Sub-Add2 internal modules

The top level view of the thresholding operation is shown in "Fig.4.13,". The inputs to this module is the 8 bit signal din generated from the Haar DWT module. The other input signal is the dc_level that acts as a reference signal for QRS peak detection.

Fig. 4.13 Top level view of Threshold module

The operational detail of the Thresholding module is depicted as - The incoming input signal is stored in memory for upto 20 locations. A max signal is considered which holds the dc_level value initially. The stored memory values are compared with this Max signal. The Max value is then compared with the stored 20 signal values, if any of the signal values is greater than the Max signal value then Max is initilaised with that signal value, else Max value remains with the initial dc_level value. By doing sucvhopertaioin the signal values greater than the dc level is found.

V. SIMULATION RESULTS

The arrhythmia detection system designed needs to be verified using appropriate tools which supports for the design. The design was modeled using Xilinx 14.7 and simulated using modelsim.

The executed arrhythmia detection system provides detailed description of detection results. The design was coded in Verilog, which remains as one of the standard HDL's in VLSI. The synthesis was performed using Xilinx 14.7 ISE and simulations using Modelsim6.3f and Implemented on Artix 7 FPGA Board. The Device used is 7A100T-3 CSG324.

A. ECG Arrhythmia Detection Module Results:

The proposed arrhythmia detection top module designed as shown in "Fig.4.1," with inputs 8-bit data_in (7:0), 8-bit dc_level (7:0), clock and reset. The module outputs are the 16-bit data_out (15:0), 16-bit time_out (15:0) signal and a 1-bit arrhythmia signal. The ECG signal that needs to be input to the proposed Arrhythmia detection system "ECG_AD_Module" is taken from the MIT-BIH Data Base. This database consists of collection of ECG samples of persons suffering from arrhythmia disorders. To verify the functioning of the proposed module, one of the sample from the MIT_BIH database is utilized as shown in "Fig.5.1,".This sections takes in the two examples as a case from the database and finds out if arrhythmia is present or not. The first sample ECG signal taken from database is as shown in "Fig.5.1,"

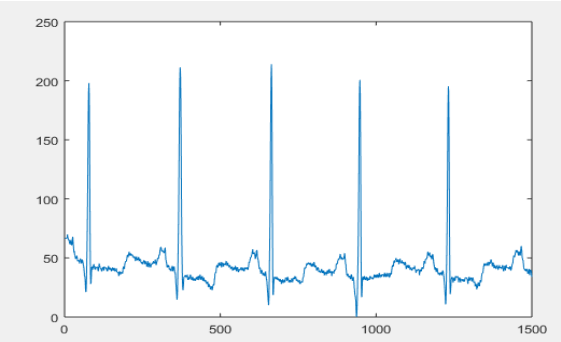

Fig. 5.1 ECG Signal Read from MIT-BIH Data Base

The simulation results from proposed design are as shown in "Fig.5.2,". The clock is activated while the reset signal is kept low for the operation.The ECG signal read from the database is displayed across the **data_in** signal. The measured **dc_level** from the sample is displayed as "**00111100**". The data_out signal output from the detection module indicates the detection of "QRS" peak from the ECG signal. Finally a transition from low to high on the **arrhythmia** output line indicates the presence of arrhythmia.

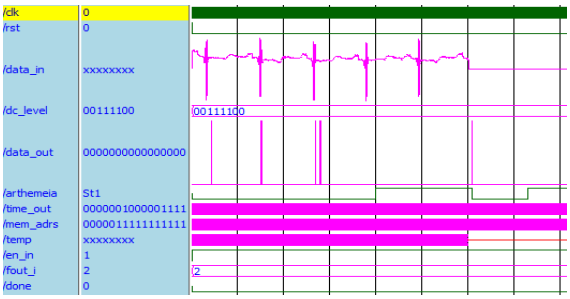

Fig.5.2 ECG Arrhythmia Detection Simulation Results

The second ECG signal sample taken from the database is displayed as shown in "Fig.5.3,".

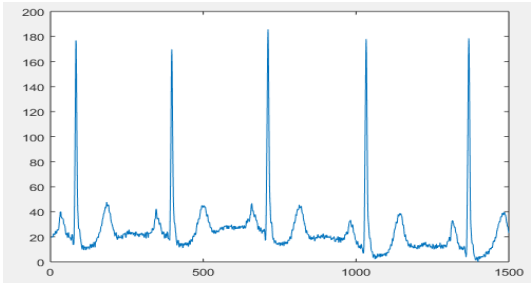

Fig.5.3 Reading the ECG Signal from MIT-BIH Data Base

The simulation results for the above input ECG signal is shown in "Fig.5.4,". The **clock** signal is active and the **reset** signal is kept low. The **data_in** line shows the ECG signal read from the database. The dc level measured from this ECG signal is "**00111100**". The **data_out** signal shows only a single peak, for five number of "QRS" peaks, indicating strong chances of arrhythmia in the person.

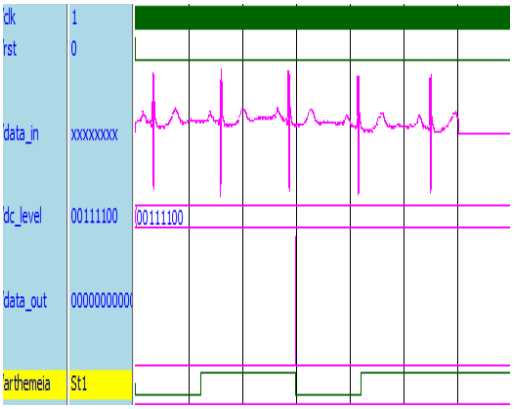

Fig. 5.4 ECG Arrhythmia Detection Simulation Results

The third ECG sample waveform taken from the database is shown in "Fig.5.5,"

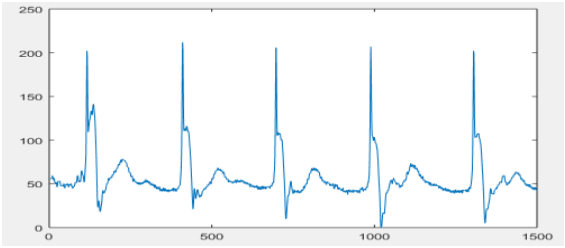

Fig. 5.5 Reading the ECG Signal from MIT-BIH Data Base

The simulation waveforms for the above ECG signal is shown in "Fig.5.6,". The data_-in line shows the ECG signal read by the module. The dc_level obtained from the input ECG signal is "00111100". The data_out signal shows four peaks for five "QRS" peaks from the ECG signal and a high signal on the arrhythmia line indicating the small chance of presence of arrhythmia in the patient's ECG.

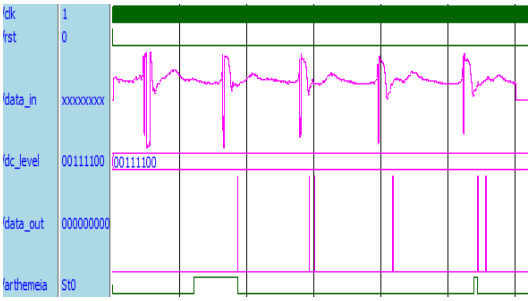

Fig. 5.6 ECG Arrhythmia Detection Simulation Results

Table 1: Design summary for the top module of ECG_AD module

Logic Utilization	Used	Available	Utilization
Number of Slice Registers	539	126800	0%
Number of Slice LUTs	2197	63400	3%
Number of fully used LUT-FF pairs	241	2495	9%
Number of bonded IOBs	51	210	24%
Number of BUFG/BUFGCTRLs	1	32	3%

The RTL schematic view for the top module of the "ECG_AD_module" is shown in "Fig.5.7,".

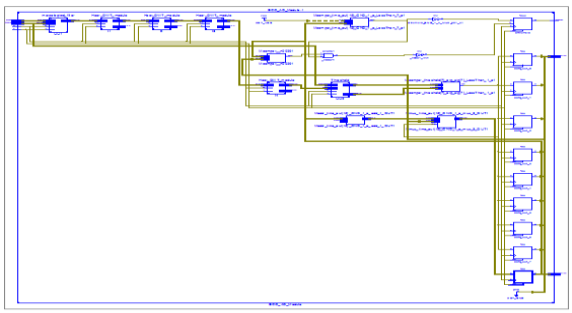

Fig. 5.7 ECG Arrhythmia Detection RTL Internal Architecture Module

The area utilized on the FPGA by the designed "ECG_AD_module" is shown in "Fig.5.8,"

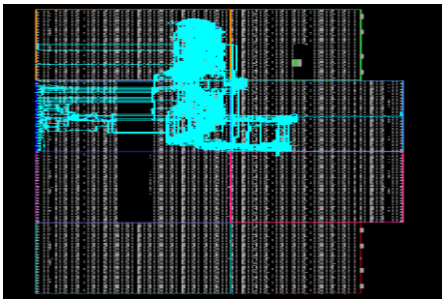

Fig.5.8 ECG Arrhythmia Detection design consumed chip-area on Artix-7 using FPGA Editor

The inputs to morphological filtering block used to preprocess the ECG signal are the clock signal, reset signal, 8-bit data_in(7:0) signal and 8-bit dc_level(7:0) signal. The output from this module is the 8-bit data_out(7:0) signal. The erosion and dilation of the input ECG signal is performed. The waveform result of the ECG signal after performing filtering operations is displayed in "Fig.5.9 (a),"

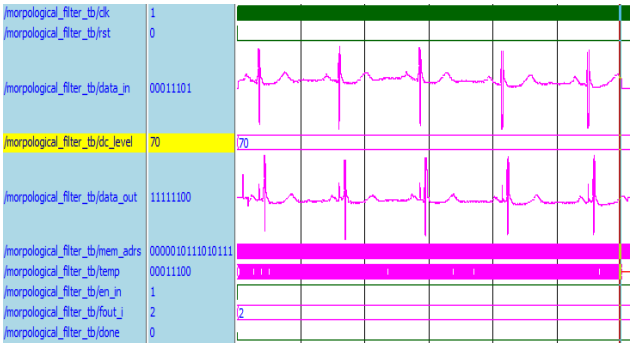

Fig. 5.9(a) Morphological Filtering Simulation Results

The waveform for the erosion operation performed on the ECG signal is shown in "Fig.5.9(b),".

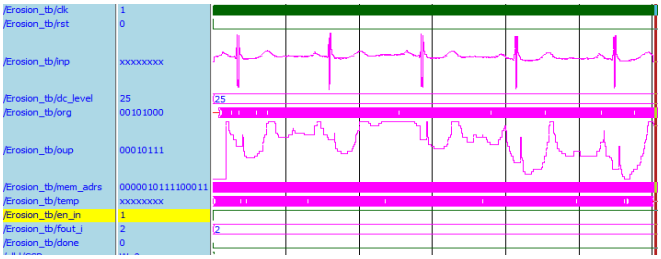

Fig. 5.9(b) Morphological filtering- Erosion

The dilation operation performed on the ECG signal is shown in "Fig. 5.9(c),".

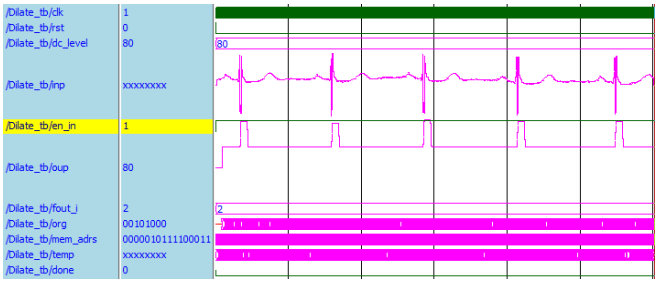

Fig.5.9(c) Morphological filtering- Dilation

The schematic view for the designed "morphological_filter" module is shown in "Fig.5.10,".

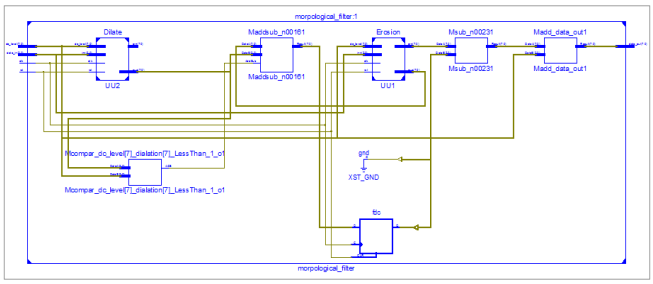

Fig. 5.10. Morphological Filtering RTL Internal Architecture Module

Table 2: Design summary for the morphological filtering module

Logic Utilization	Used	Available	Utilization
Number of Slice Registers	230	126800	0%
Number of Slice LUTs	1082	63400	1%
Number of fully used LUT-FF pairs	93	1219	7%
Number of bonded IOBs	26	210	12%
Number of BUFG/BUFGCTRLs	1	32	3%

The "Haar_DWT_module" top level module design takes the inputs from the morphological _filter outputs. The input to this module is 8-bit data_in signal, clk and rst signals. The output signals from the module are high_out(8:0) which represents the higher frequency components of the ECG signal and low_out(8:0) represents the lower frequency components. The simulation waveforms for the designed "Haar_DWT_module" is shown in "Fig.5.11," it clearly indicates the higher and lower frequency details in the ECG signal.

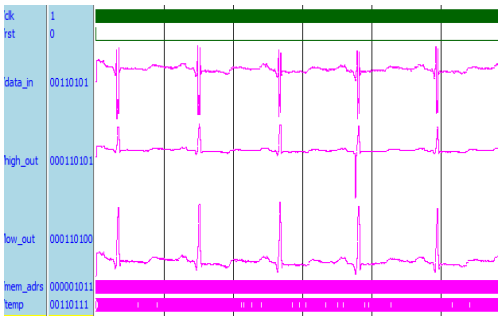

Fig. 5.11. Haar-DWT Simulation Results

The RTL schematic view for the "Haar_DWT_module" is shown in "Fig.5.12,".

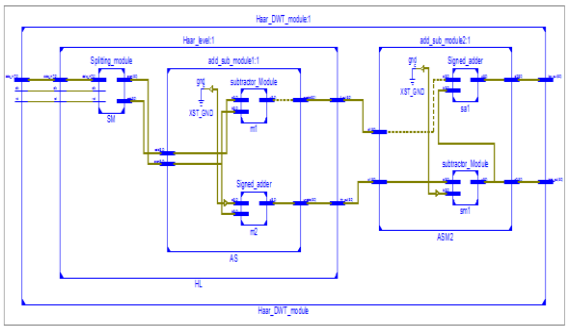

Fig. 5.12. Haar-DWT RTL Internal Architecture Module

Table 3: Design summary for the Haar-DWT module

Logic Utilization	Used	Available	Utilization
Number of Slice Registers	17	126800	0%
Number of Slice LUTs	139	63400	0%
Number of fully used LUT-FF pairs	9	147	6%
Number of bonded IOBs	28	210	13%
Number of BUFG/BUFGCTRLs	1	32	3%

The top level module of the "Threshold" module design takes the inputs dc_level (7:0) measured from the ECG signal. The 8-bit input signal inp(7:0) obtained from "Haar_DWT_module" output is fed here. The output obtained from this module is the 8 bit original signal org(7:0) which represents the inp(7:0). The 8-bit threshold(7:0) signal indicates the presence of "QRS" peaks in the ECG signal. The simulation waveforms for the "Threshold" module is shown in "Fig.5.13,". The waveform clearly show the detection of the higher frequency peaks in the ECG signal.

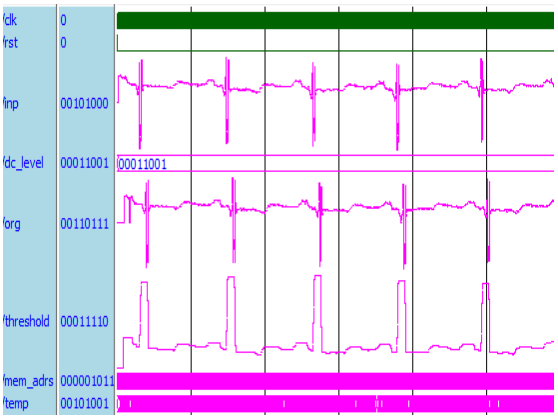

Fig. 5.13. Thresholding simulation result

The RTL schematic view for the "Threshold" module is shown in "Fig.5.14,".

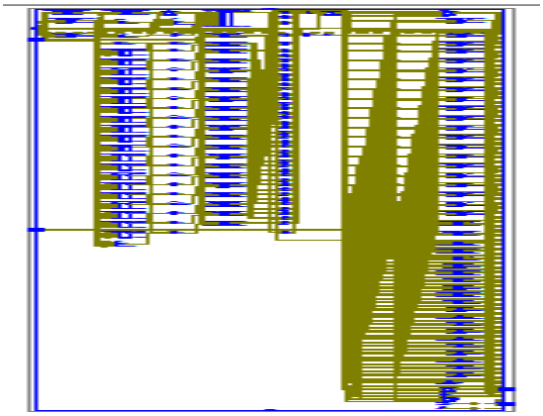

Fig. 5.14. Thresholding RTL Internal Architecture Module

Table 4: Design summary for the Thresholding module

Logic Utilization	Used	Available	Utilization
Number of Slice Registers	212	126800	0%
Number of Slice LUTs	1139	63400	1%
Number of fully used LUT-FF pairs	73	1278	5%
Number of bonded IOBs	34	210	16%
Number of BUFG/BUFGCTRLs	1	32	3%

B. FPGA Implementation of the Proposed Design

The proposed design for ECG arrhythmia detection module is implemented on Artix-7 FPGA and physically debugged using Chip scope-pro Tool.

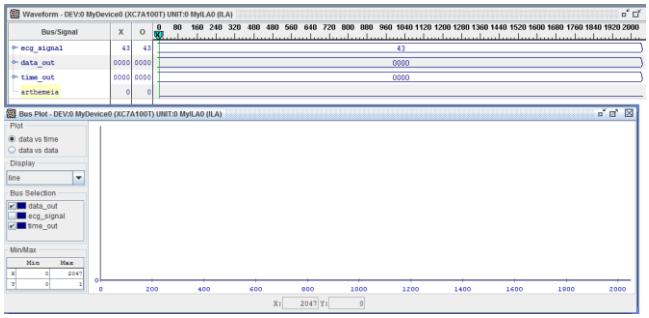

Fig.6.1. Proposed ECG-AD-Module, When reset =1 using chip-scope-pro tool

When rst=1 from the "Fig.6.1," ecg_signal is fed as the input and correspondent data_ out for the arrhythmia detection is achieved. In this case patient is suffering from arrhythmia.

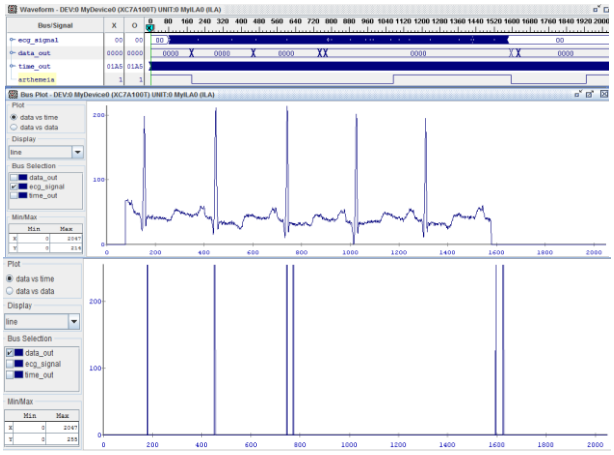

Fig.6.2. Proposed ECG-AD-Module, When reset =0, using chip-scope-pro tool

When rst=0 from the "Fig.6.2,", ecg_signal is fed as the input accordingly data_ out for the arrhythmia detection is achieved. In this case patient is normal.

The proposed arrhythmia detection system designed based on FPGA from the results showed that it utilized less number of resources in terms of total number of pins, registers and memory bits when compared to previous design found from the literature. The proposed design when compared with most proven design [24] proved to be more efficient in terms of resource utilization, the results showed that the total registers are 792 when compared to that of the previous design [24] to be 3532. Total pins and memory bits are 43 and 51177, that in case of previous design [24] are 128, 131072 respectively. The comparison overhead in terms of total registers is found to be 78% and in terms of total memory bits is found to be 61%.

VI. CONCLUSION

Arrhythmia is a special kind of cardiac disorder that exist in the heart rhythm due to abnormal fast rates or abnormal slow rates. Patients with such a disorder do not find symptoms that are normally observed for other cardiac disorders and may turn to be life threatening if not diagnosed in earlier stages. The symptoms for such a disorder may not be found by diagnosing a single snapshot of an ECG signal. In these cases the life threatening arrhythmias has to found out by a continuous monitoring of the ECG signals which is a very tedious and a time consuming process, as it requires a continuous observation from the specialist. Thus there is a requirement of a system that can detect the arrhythmia conditions, from the ECG signals.

The proposed work presents the development of a system that can detect the presence of arrhythmia in a patient from the ECG signal. The system is developed based on a levels of "QRS" peaks present in the ECG signal. The system performs the following signal processing operations, morphological filtering, feature extraction using Haar DWT and Thresholding. The morphological processing involves erosion and dilation operations on the ECG signal. The morphed signal is filtered using Haar DWT to obtain the higher frequency. The higher frequency components signal levels are checked in the Thresholding operation for detecting the QRS peaks. The arrhythmia will be detected for absence of the QRS peaks in the ECG signal.

The proposed system "ECG_AD_module" model development was performed using Verilog HDL and the design was on the FPGA kit. The simulation was performed for the proposed model where the ECG signals were read from a MIH database and input to the system. The output waveforms generated from the simulations confirmed the presence of arrhythmias in the ECG signals obtained from patients suffering these disorders.

The design was successfully implemented on the FPGA and the hardware results were similar to the waveforms to that observed in simulations. The FPGA implemented signal thus could successfully read the ECG signal and detect the arrhythmias by producing an output signal that goes high when arrhythmias are detected.

The performance of the implemented "ECG_AD_module" was compared with other arrhythmia detection system. The total number of registers utilized for the proposed design was 77.57 improved than the previous design [24].

REFERENCES

1. Tompkins, Willis J. "Biomedical digital signal processing," Editorial Prentice Hall , 1993.
2. Sörnmo, Leif, and Pablo Laguna, "Electrocardiogram (ECG) signal Processing," Wiley encyclopedia of biomedical engineering, 2006.
3. Bhateja, Vikrant, et al., "A composite wavelets and morphology pproach for ECG noise filtering," International Conference on Pattern Recognition and Machine Intelligence. Springer, Berlin, Heidelberg, 2013.
4. Keating, Mark T., and Michael C. Sanguinetti, "Molecular and cellular mechanisms of cardiac arrhythmia," Cell 104.4 , 2001, pp. 569-580.
5. Parák, Jakub, and Jan Havlík, "ECG signal processing and heart rate frequency detection methods," Proceedings of Technical Computing Prague 8, 2011.
6. De Chazal, Philip, Maria O'Dwyer, and Richard B. Reilly, "Automatic classification of heartbeats using ECG morphology and heartbeat interval features," IEEE transactions on biomedical engineering 51.7, 2004, pp. 1196-1206.
7. Kazakeviciute, Margarita, Algimantas Juozapavicius, and Ruta Samaitiene, "Morphological filtering of EEG," Materials Physics and Mechanics 9.3, 2010, pp. 185-193.
8. Zhang, Fei, and Yong Lian, "QRS detection based on multiscale mathematical morphology for wearable ECG devices in body area networks," IEEE Transactions on Biomedical Circuits and Systems 3.4, 2009, pp. 220-228.

9. Ghorbanian, Parham, et al. "Heart arrhythmia detection using continuous wavelet transform and principal component analysis with neural network classifier," Computing in Cardiology, IEEE, 2010.
10. Chan, H. L., et al. "Heartbeat detection using energy thresholding and template match," Engineering in Medicine and Biology Society, IEEE-EMBS, 27th Annual International Conference of the IEEE, 2006.
11. Zheng, Peijia, and Jiwu Huang, "Discrete wavelet transform and data expansion reduction in homomorphic encrypted domain," IEEE Transactions on Image Processing, 2013 pp. 2455-2468.
12. Audithan, S., and R. M. Chandrasekaran, "Document text extraction from document images using haar discrete wavelet transform," European Journal of Scientific Research 36.4, 2009, pp.502-512.
13. Vijendra, V., and Meghana Kulkarni, "ECG signal filtering using DWT haar wavelets coefficient techniques," Emerging Trends in Engineering, Technology and Science (ICETETS), International Conference on. IEEE, 2016.
14. Rajpurkar, Pranav, et al. "Cardiologist-level arrhythmia detection with convolutional neural networks," arXiv preprint, arXiv: 1707-01836, 2017.
15. Lobodzinski, S. Suave, and Michael M. Laks, "New devices for very long-term ECG monitoring," Cardiology journal 19.2 , 2012, pp. 210-214.
16. Nasiri, Jalal A., et al. "ECG arrhythmia classification with support vector machines and genetic algorithm," Computer Modeling and Simulation, EMS'09, Third UK Sim European Symposium on. IEEE, 2009.
17. Alonso-Atienza, Felipe, et al. "Detection of life-threatening arrhythmias using feature selection and support vector machines," IEEE Transactions on Biomedical Engineering 61.3 2014, pp. 832-840.
18. Kanhe, R. K., and S. T. Hamde, "ECG signal compression using 2-D DWT Hermite coefficients," Signal and Information Processing (IConSIP), International Conference on. IEEE, 2016.
19. Martínez, Juan Pablo, et al. "A wavelet-based ECG delineator: evaluation on standard databases," IEEE transactions on biomedical engineering 51.4, 2004, pp. 570-581.
20. Meddah, Karim, HadjerZairi, and Malika Kedir Talha, "New system cardiac arrhythmia detection on FPGA," Modelling, Identification and Control (ICMIC), 7th International Conference on. IEEE, 2015.
21. Tripathi, Avinash, and Shahanaz Ayub, "Heart Rate Variability Detection in Arrhythmia," Computational Intelligence and Communication Networks (CICN), International Conference on. IEEE, 2015.
22. Besrour, Rym, ZiedLachiri, and Noureddine Ellouze, "Detection of an electrocardiogram R wave based on the multiscale products: MIT/BIH arrhythmia and Qt databases evaluation," Signal Processing and its Applications, ISSPA 2007, 9th International Symposium on. IEEE, 2007.
23. Clifford, G. D., et al. "Model-based filtering, compression and classification of the ECG," International Journal of Bio electromagnetism 7.1. 2005, pp. 158-161.
24. Alhelal, Dheyaa, et al. "FPGA-based denoising and beat detection of the ECG signal," Systems, Applications and Technology Conference (LISAT), IEEE, 2015.

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