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Nano Power Current Reference Circuit consisting of Sub-threshold CMOS Circuits

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Abstract: *a low voltage CMOS Nano power current reference circuit has been presented in this paper and also the circuit simulation performance in 180-nm UMC CMOS technology. Most of the MOSFETs operate in sub-threshold region consisting of bias-voltage, start-up and current-source sub-circuits. A stable reference current of 4-nA lying in supply voltage range of 1 V-1.8 V has been generated with line sensitivity of 0.203% /V. Within the temperature range of 0°C to 100 °C, and the voltage level of 1.8 V, the temperature coefficient was 7592ppm/°C. At the same voltage supply, the power dissipation was found out to be 380 NW. It is suitable to use this circuit in sub threshold power aware large scale integration.*

Keywords: *Low power, low voltage, sub threshold, temperature coefficient.*

I. INTRODUCTION

Various papers contain the references of Nano ampere current [1][2]. But these Nano ampere current circuits dissipate large amount of power and output current are largely depending on temperature but the circuit is not appropriate to be used in those environments in which the change in output current result in change in temperature because it increases in proportion with increase in temperature. This work proposes a method to design a constant current reference circuit that is capable of working in sub-threshold region over a large range of temperature. These problems will be resolved by current reference circuit and implemented for use in ultralow-power LSIs. The resistors are not used here as the power is dissipated in few Nano watts. A reference current, insensitive of supply voltage and temperature is applied to this design. The organization of this paper is done as follows: section 2 comprises of operation principle and circuit configuration, section 3 comprises of important parameters, section 4 comprises of simulation results and section 5 comprises of the conclusion and all the simulation.

All this was performed in Cadence UMC CMOS process by using Spectre EDA Tool.

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II. OPERATING PRINCIPLE

The current reference circuit is shown in figure 5. The circuit comprises of PTAT voltage generator, start-up circuit, bias voltage circuit and a PTAT voltage generator.

A. Features of sub-threshold current

Since the order of operation of sub-threshold current is of the order of Nano-amperes, it is possible to achieve ultralow-power operation by sub-threshold operation. The sub-threshold current I is given as below for a value higher than 0.1 V of drain-source voltage of MOSFET:

$$I = KI_0 \ exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right) \quad (1)$$

K is an aspect ratio of transistor and Io $(= \mu C_{ox} (\eta - 1) V_T^2)$ a parameter which depends on process, μ denotes the mobility of a carrier, $C_{ox}\left(= \frac{\varepsilon_{ox}}{t_{ox}}\right)$ denotes the capacitance of gate-oxide, ŋ denotes the sub-threshold slope factor, the oxide permittivity is denoted by ε_{ox}, K denotes the Boltzmann constant, T and q denotes the absolute temperature and elementary charge respectively and V_{TH} denotes the threshold voltage of MOSFET. The features of a sub-threshold MOSFET are analysed and a constant parameter for p and n MOSFETs are used respectively.

B. Constant current sub circuit

There is a current source circuit in this circuit. Only the MOS resistor functions in deep triode and strong inversion regions while rest other MOSFETs operate in sub threshold region. On comparing with basic β multiplier [3]: a resistance resistor is not required which is capable of occupying large area on LSI chip and for suitable bias voltage V_{BIAS} for a MOS transistor [4], a zero temperature coefficient of current can be achieved.

C. PTAT Voltage Generator

It comprises of a differential pair with current mirror. During the operation of MOSFET in sub-threshold region, the gate to gate voltage (V_{GG}) can be derived from equation 1 as follows:

$$V_{GG} = \eta V_T \ln\left(\frac{K_{D1}\ K_{M2}}{K_{D2}K_{M1}}\right) \quad (2)$$

K_{D1} and K_{D2} are the aspect ratios of differential pair whereas K_{M1} and K_{M2} are aspect ratios of PMOS current mirror. By making $(K_{D1}K_{M2})/(K_{D2}K_{M1})>1$, PTAT voltage can be generated [5].

D. Bias Voltage sub circuit

The Bias voltage sub circuit controls the characteristics of MOS resistor M_R. The voltage for M_{D1} and M_{D2} in a generator circuit are generated by M_B for functioning in deep triode and strong-inversion region.

The characteristics of PMOS M_R resistor that operates in deep triode region helps in determining the current I_{REF} in the circuit. If $V_{GSR} >> V_{TH} - V_{DSR}$, the current is calculated as given below:

$$I_{REF} = \mu C_{ox} K_R \, (V_{GSR} - V_{TH}) V_{DSR} \quad (3)$$

The MOS M_R and M_B have the same length of gate L and width W and they are biased to same current. In order to increase the value of M_R, a voltage is added to the gate source voltage of M_B. The threshold voltages of equal sized MOSFETs M_R and M_B are similar for generating current to robust process variation.

E. Startup Circuit

The stable state in a zero bias condition is avoided by a start-up circuit.

III. IMPORTANT PARAMETERS

A. Temperature Coefficient

The change in the output current with the change in operating temperature gives a measure of temperature coefficient. The output current I_{REF} has its temperature coefficient as given by:

$$TC = \frac{1}{I_{REF}} \frac{dI_{REF}}{dT} \quad (4)$$

B. Line Sensitivity

The ability of a circuit to vary supply voltage for maintaining the specified output current is known as line sensitivity.

$$L.S = \frac{\Delta I_{REF}}{\Delta V_{DD} \, I_{REF}} \times 100 \quad (5)$$

C. Load regulation

Under the condition of varying load, the ability of a circuit to maintain the specific value of output current is known as load regulation.

$$L.R = \frac{I_{noload} - I_{maxload}}{I_{maxload}} \times 100 \quad (6)$$

D. Power supply rejection ratio

For having better performance of circuit, PSSR should be high. The rejection of noise in supply voltage at different frequencies is known as power supply rejection ratio. It is the ability of the circuit to reject the noise present in supply voltage at different frequencies.

$$PSRR = 20 \log_{10} \frac{output\ ripple\ voltage}{input\ ripple\ voltage} \quad (7)$$

IV. SIMULATION RESULTS

The Cadence EDA tool was used to simulate this circuit in 180 nm CMOS process by schematic analysis by spectre and layout analysis by virtuoso at room temperature. The ADE window is used for circuit simulation of different circuit analysis like AC, Trans, corner, DC, parametric, Monte Carlo etc. The reference output current is calculated by performing DC analysis.

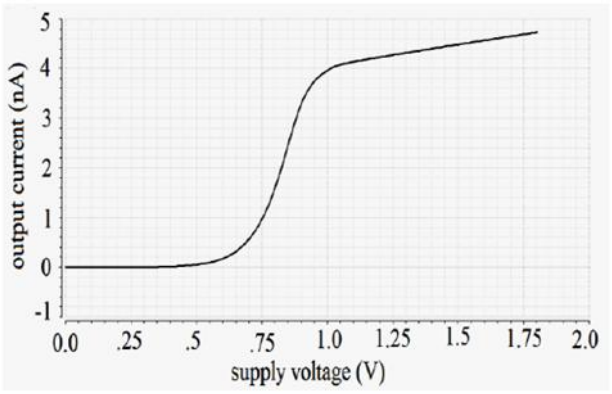


Fig. 1 Simulated output current at room temperature as a variation of supply voltage

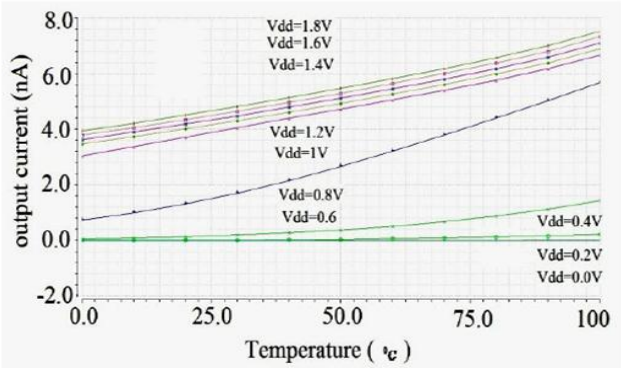
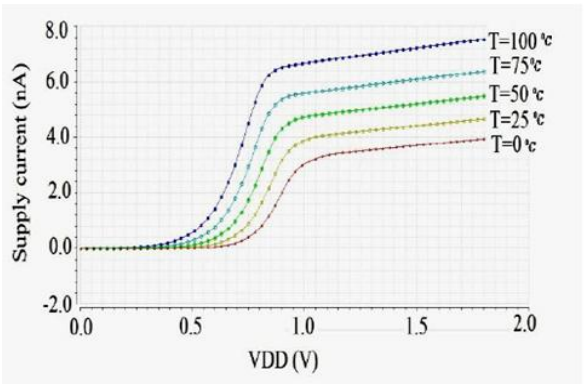
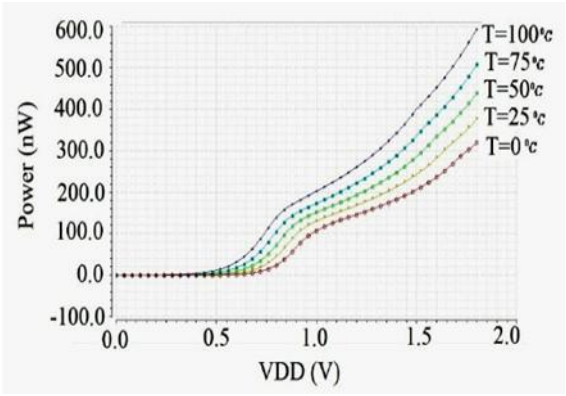


Fig. 2 Simulated current IREF as a function of temperature



[a.] **Fig. 3 Measured output current I_{REF} as a function of Supply voltage**



[a] **Fig. 4 Simulated DC power as a function of supply voltage for different value of temperature**

V. CIRCUIT DIAGRAM

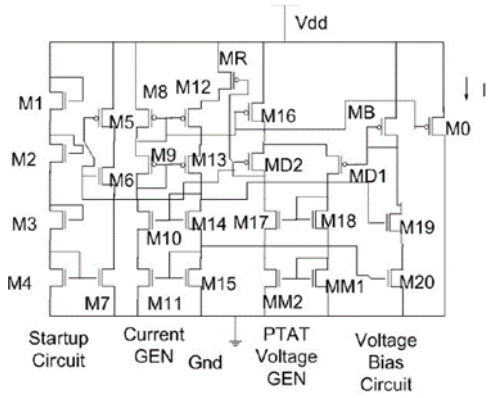


Fig. 5 Proposed current reference circuit

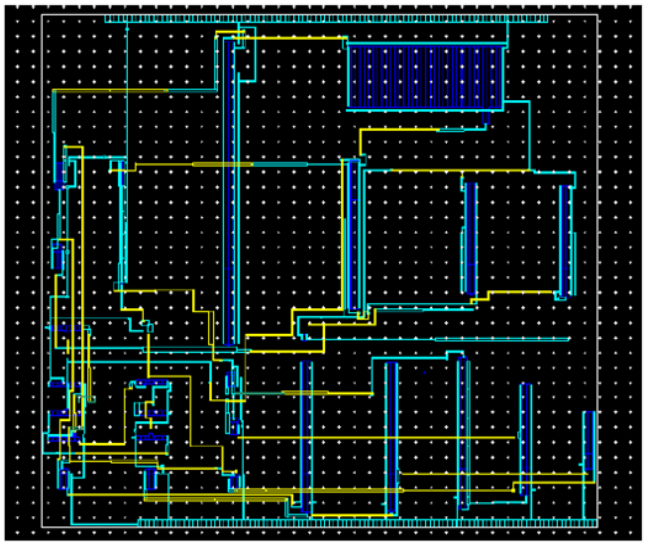


Fig. 6 Photo of Chip

The reference current IREF is generated as a variation of operating voltage at absolute temperature. At the operating voltages higher than 1 V, the circuit is designed to work accurately. At an operating voltage range between 1 to 1.8V, the sensitivity is 0.203%/V. The Nano ampere operating current, which is independent of the temperature and the operating voltage can be produced by this circuit. For an operating voltage 1.8 V and temperature range of 0° to 100° C, the plot of output current IREF and variation of operating temperature is shown in figure 2. At a supply voltage of 1.8V, the temperature coefficient was found to be 7592ppm/°C. At different values of operating temperature, the DC power of a circuit at a supply voltage of 1.8 V is shown in figure 4.

Table 1 Comparison of CMOS current reference circuit

parameters	Ref. [3]	Ref. [4]	Ref. [5]	Ref. [6]	This work
CMOS technology	1.5µm	3µm	2µm	2µm	0.18µm
V_{DD} (V)	1.1	3.5	1.2	5	1-1.8
I_{REF} (nA)	.41	774	1-100	285	4
TC ppm /°C	2500	375	1100	230	7592
LS % /V	6	0.015	10	-	0.203
Temp °C	-20 to 70	0 to 80	-40to 80	0 to 75	0 to 100
Power (μW)	0.002	10	.07	-	0.38
Die area $(mm)^2$	0.046	0.2	.06	-	0.0306

VI. CONCLUSION

A Nano-ampere reference current generated circuit has been implemented in this work, which is capable of operating at a wide range of supply voltage, and the simulation of performance was done in 180-nm CMOS process. A constant reference current of 4 nA is generated by this designed circuit. Within the operating voltage range of 1 to 1.8V, the line regulation was found to be 0.203%/V. The temperature coefficient was calculated ot be 7592ppm/°C. At a supply voltage of 1.8 V, the power consumed by circuit was 380nW. The other new structures of MOS and the current trimming technique are implemented for reducing the value of temperature coefficient, dissipation of power and improving the value of line regulation.

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