Performance Analysis of Three-Phase DVR with Modified Switching Band Controller

Vasudeva Naidu Pudi, Srinivasa Rao Sura, Prasad Bolla

Abstract: ***This paper deals with the mitigation of voltage related PQ issues by using three phase neutral clamped VSI topology is used to realize the DVR and the design of DVR for the selection of suitable interface inductor, DC capacitor storage series resistance and the capacitance. Here three-phase four wire DVR with modified switching band controller topology is proposed, which overcome the frequent band violation, poor controllability and heavy filter currents, and compared to three-phase four wire DVR with conventional filter topology. The compensation capability of the proposed topology is analyzed based on simulation studies and corresponding results are compared with different switching control strategies. The consequent merits and demerits switching loss in VSI, ripple in compensated load voltages and error between reference injected voltages and actual injected voltages in different switching control strategies are discussed.***

Keywords: **Dynamic Voltage Restorer (DVR), Neutral Clamped VSI,Switching Band Controller, Synchronous Reference Theory (SRF) and Power Quality (PQ).**

I. INTRODUCTION

The demand for electricity is booming due to growth in population and economy in the last decade. The quality and reliable power are essential for sustainable development of any country. Now a day's a large number of Renewable Energy Sources (RES) are integrated to the distribution the grid to achieve reliable and to meet the present electrical energy demand. However, the interaction of RES requires the use of power the electronic converters. However, they introduce distortion in Voltage (V) and Current (I), which leads to many PQ issues [1],[2]. Moreover, other PQ issues like voltage unbalance and voltage sag/swell are arising due to various power system faults, large single phase loads like traction loads, induction furnace loads and connection /disconnection of heavy loads in the distribution grid. Non-linear loads, for example, control hardware gear including Adjustable Speed Drives (ASD), Switched Mode Power Supplies (SMPS), and data processing equipment type of loads, starting of large motors, lightning and switching surges, etc., causes, harmonics in distribution grid [3]. The adverse effects with these PQ issues are excessive neutral currents, overheating of the electrical Equipment, voltage distortions leading to malfunctioning of the relays, increased power losses in the distribution systems and interference with the communication systems [4]. Hence, there is a need for corrective measures to achieve quality and reliable power. There are several approaches proposed by the researchers for mitigating the PQ problems in the existing literature. Earlier researcher's proposed passive filters consisting of inductor and capacitors tuned for a particular frequency, are used to reduce these power quality problems, but these filters have the limitations like bulky in size, involve in series and parallel resonance, need for the high rating and require proper reactive power coordination. To overcome the above mentioned problems, active power filters are introduced in [5]-[8]. They are also called custom power devices (CPDs) when these are utilized in power distribution systems [3]. Recently many researchers have been proposed CPDs overcome power quality issues in distribution systems. The custom power devices include D-STATCOM, DVR and UPQC have been realized using power electronic converters [9]. However, control of these power electronic converters is a key concern for mitigating the PQ issues in distribution systems.

In present era the major power quality issue facing industries, local customers are voltage sag, voltage swell, interruptions etc., so in this paper is designed the dynamic voltage restorer (DVR) to compensate the voltage related issues in load end or at PCC. The design of DVR the primary consideration is selection of VSI topology, Various VSI topologies are used for mitigate voltage related problems at the PCC like three phase 3-wire VSI topology, H-bridge VSI Topology, three phase 4-wire VSI topology etc., but in this paper designed neutral clamped VSI topology based DVR is shown Fig.1. Here VSI consist of switches 1, 3, 5 in upper limb and 4, 2, 6 in lower limb with diode in parallel to each switch. Two identical D.C. Storage capacitors (common DC-link) are connected in parallel to VSI. By taking energy stored in DC link each leg of VSI is independently controlled [10]-[12]. The second important aspect in design of DVR is the selection of suitable coupling transformer, it can experience saturation during the transient period after a voltage sag starts. For preventing this, normally the value of flux taken is twice that of steady state limit. The DVR coupling transformer performs two important functions: voltage boost and electrical isolation. The third consideration in design of switching band filter circuit which consist of interfacing inductor and the passive capacitor (Cse) finally the selection of reference DC link voltage values is also essential [13]-[14].This method has a major drawback i.e reverse dc voltage is applied using control algorithim, which leads to increase in switching loss, and which in turn injects ripples into the injected voltage. These ripples reduces the system performance.

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Hence in this chapter three-phase four wire DVR with modified switching band controller topology is proposed, which over comes the switching losses, poor controllability and improve the system performance. The DVR consist of switching band filter hence the performance of depends on the values of filter components. The simulation studies carried out and the compensation capability of proposed method with different switching control strategies, merits and demerits, switching loss in VSI, ripple in compensated load voltages and error between reference injected voltages and actual injected voltages are discussed.

II. SYSTEM REPRESENTATION

Schematic of conventional three phase three leg-four wire DVR topology is shown Fig.1.This topology consists of voltage source inverter (VSI) connected in series to load at the PCC through injection transformer, interface filter (interface inductor (L_{se}) and capacitor (C_{se}). The purpose of interfacing filter is to shape inject voltages while tracking the reference injected voltages. Here v_{la} , v_{lb} , v_{lc} represents the instantaneous phase voltages at the PCC, which may be distorted because of faults that can exist in the system are single line-to-ground fault, double line-to-ground, line-to-line fault and three-phase fault. The injected voltages v_{inja} , v_{injb} v_{injc} represents the actual injected voltages obtained using hysteresis control technique, i_{sa} , i_{sb} , i_{sc} represents the source currents and i_{la},i_{lb},i_{lc} represents the load currents. The capacitance C_{dc} is the dc storage capacitor used for maintaining the input voltage of VSI at reference value of V_{dcref} . However, instantaneous voltage across C_{dc} is denote as v_{dc} in following text.

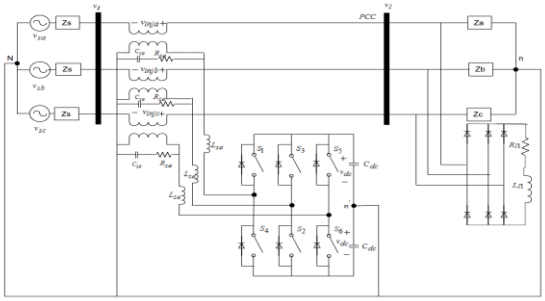

Fig.1 Schematic diagram of conventional three phase four wire DVR topology

A. Different Operations of DVR

In-Phase Boosting Technique:

The phasor diagram of the DVR compensated distributed system through in-phase boosting technique is shown in Fig. 2. The load voltage is $\bar{V}_{l1}^{1}$ before occurrence of sag and the load draws a current $\bar{I}_{l1}^{1}$ at a power factor angle ϕ . The source current $\bar{I}_{s1}^{1}$ is in phase with the load voltage $\bar{V}_{l1}^{1}$. It can be observed from Fig.2 that the terminal voltage will be $\bar{V}_{t2}^{1}$ with phase jump δ due to the sag in the system. In DVR through in-phase boosting operation during balanced sag, the series active power filter (SEAPF or DVR) injects voltage in phase with source current and voltage sag to achieve nominal voltage. In case of unbalanced voltage sag with phase jumps, by in-phase boosting operation nominal load voltage can be attained but phase jumps are not eliminated. Hence, in-phase boosting operation is not applicable for mitigating the negative and zero sequence sag voltages. Hence, first the negative sequence voltage, $\bar{V}_{t2}^{1-}$ and zero sequence voltage $\bar{V}_{t2}^{10}$ of the terminal voltage sag $\bar{V}_{t2}^{1-}$ should be mitigated to make it balanced sag. After mitigating $\bar{V}_{t2}^{1-}$ and $\bar{V}_{t2}^{10}$, DVR also injects $\bar{V}_{inj}^{1+}$ in phase with the source current $\bar{I}_{s2}^{1}$ to achieve the nominal load voltage $\bar{V}_{inj}^{1+}$ with respect to $\bar{V}_{t2}^{1+}$ labelled as X which is shown in Fig.2. Therefore, real power is injected into the system by DVR in order to achieve $\bar{V}_{l2}^{1}$.

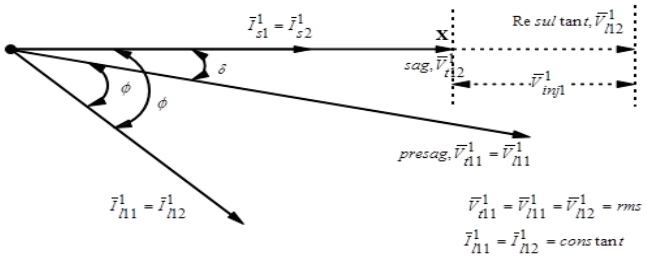

Fig. 2. Phasor diagram for DVR through in-phase boosting operation

Pre-Sag Supply Voltage Boosting Technique

In this method, the series injected voltage is vector difference between the presage voltage and the sag voltage (i.e., $\bar{V}_{inj}^{1} = \bar{V}_{t1}^{1} - \bar{V}_{t2}^{1}$), which is shown in Fig.3. This method of operation is called as DVR-presag. Here, the DVR injects both real and reactive power. In all the above methods, except pre-sag supply voltage boosting operation, the mitigation of voltage sag with phase jumps is with respect to positive sequence voltage sag($\bar{V}_{t2}^{1+}$). The DVR require positive sequence voltage components only but in above methods it inject the negative sequence voltage ($\bar{V}_{t2}^{1-}$), zero sequence voltage ($\bar{V}_{t2}^{10}$) and along with $\bar{V}_{inj}^{1+}$. Hence the VA loading increase.

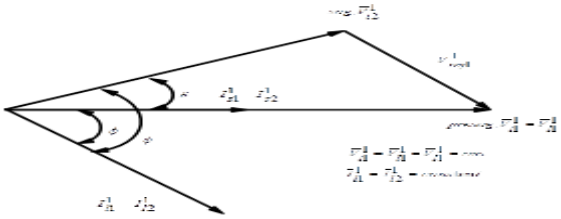

Fig.3. Phasor diagram for DVR- presag operation.

B. Control Theory for Generation of Reference Quantities in DVR

The DVR has two important tasks first one is the generation of reference injecting voltages and secondly comparing these voltages with that of actual voltages generated by voltage source inverter (VSI).

C. Generation injected voltages by using synchronous reference frame (SRF) method.

Synchronous Reference Frame (SRF) theory:

This theory discussed is used to generate reference compensating voltages for DVR. Here it is used to generate reference injected voltage for DVR. By using park transformation the three phase instantaneous voltages in *abc* reference frame are transferred to *dq0* rotating reference, and the expressions of voltages as given below.

$$\begin{bmatrix} v_{sq} \\ v_{sd} \\ v_{s0} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \\ \sin(\theta) & \sin(\theta - 2\pi/3) & \sin(\theta + 2\pi/3) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} v_{sa} \\ v_{sb} \\ v_{sc} \end{bmatrix} \quad (1)$$

$$\theta(t) = \int_0^t \omega(t)dt + \alpha(0) \quad (2)$$

$$v_{s\_dqo} = T_{abc}^{dqo} v_{s\_abc} \quad (3)$$

Now, at $\theta = \omega t$, the frequency component of source voltages include both oscillating components ($\tilde{v}_{sd}$ and $\tilde{v}_{sq}$), average components ($\overline{v}_{sd}$ and $\overline{v}_{sq}$) and under unbalanced source voltage with harmonics. Switching loss of VSI (v_{loss}) component should be added to $\tilde{v}_{sd}$ obtain total $d-$axis reference injected voltages. In oscillating components $\tilde{v}_{s\_q}$ having source voltage negative-sequence components and harmonic under distorted load conditions. So that cancel the $\tilde{v}_{s\_q} = 0$ and $v_{s0} = 0$ Voltages should be supplied from controller. Therefore the $d, q, 0$ reference load voltages are given in equation. 4,

$$v_{ld}^* = \tilde{v}_{sd} + v_{loss} \quad (4)$$

$$v_{lq}^* = v_{sq} = 0 \ , v_{l0}^* = v_{s0} = 0$$

Injected reference voltages ($v_{inj\_dqo}^*$) in *dqo* reference frame ($v_{inj\_dqo}^*$) as given in equation.5.

$$v_{inj\_dqo}^* = v_{s\_dqo} - v_{l\_dqo}^* \quad (5)$$

To transfer the injected voltages from *dqo* to *abc* inverse Park transformation is used and voltages are as given in equation (6)

$$v_{inj\_abc}^* = T_{dq0}^{abc} v_{inj\_dqo}^* \quad (6) \text{ and } (7)$$

$$\begin{bmatrix} v_{inj\_a}^* \\ v_{inj\_b}^* \\ v_{inj\_c}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\omega t) & \sin(\omega t) & 1/\sqrt{2} \\ \cos(\omega t - 2\pi/3) & \sin(\omega t - 2\pi/3) & 1/\sqrt{2} \\ \cos(\omega t + 2\pi/3) & \sin(\omega t + 2\pi/3) & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} v_{inj\_d}^* \\ v_{inj\_q}^* \\ v_{inj\_0}^* \end{bmatrix}$$

III. SWITCHING CONTROL

A. Inverter's output filter design of DVR:

In the DVR compensator system, the inductance of the L_{se} is the sum of leakage inductance of transformer and inverter interface inductor. This inductance L_{se} along with capacitor C_{se} acts as an active filter. Here i_L , i_C denote load current and capacitor current, i_{inv} , v_{inv} denote inverter output current and voltage respectively. The polarity of v_{inv} depends on the boundary conditions of the hysteresis controller. The schematic diagram of this active filter is shown in Fig.4a.

The DVR voltage trajectory is a parabolic and leads to second order response as it combination of L & C which oscillates between limits of $v_{dvra}^* - h$ and $v_{dvra}^* + h$ as shown in Fig.4b. Due to the oscillating nature of the response the voltage across capacitor is not linear, even when a reverse DC voltage is also applied. This violation leads poor quality of load voltages which increases THD (%) and decreases reactance of capacitor at switching frequency which leads to higher rating of capacitor, hence cost of DVR increases. This is a major drawbacks of the conventional filter which can be eliminated by proper selection filter circuit.

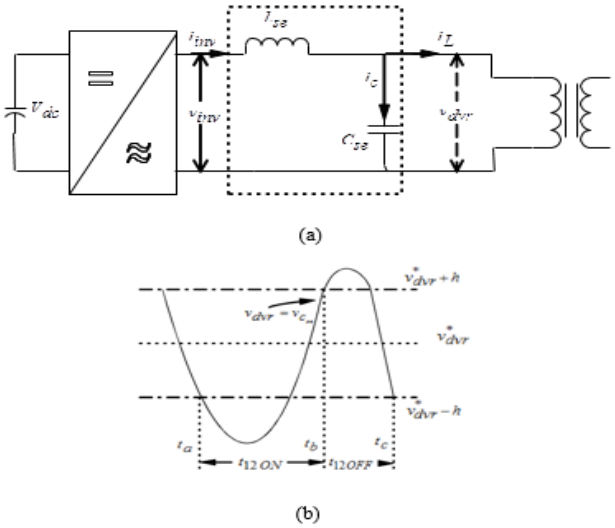

Fig..4 Schematic diagram of DVR (a) filter circuit (Conventional), (b) Output voltage across the capacitor

B. Modified Filter Circuit for Band Controller:

The drawback of the conventional filter is overcome by adding a resistor (R_{se}) in series with filter capacitor as shown in Fig. 5 (a). This value of resistance makes resistive voltage drop v_{Rsw} greater than capacitive reactance voltage drop (v_c) at switching frequency. Now the active filter act as like R-L circuit, making the DVR voltage (v_{dvr}) linear as shown in Fig. 5(b). Since these injected voltages are linear the above drawback is nullified.

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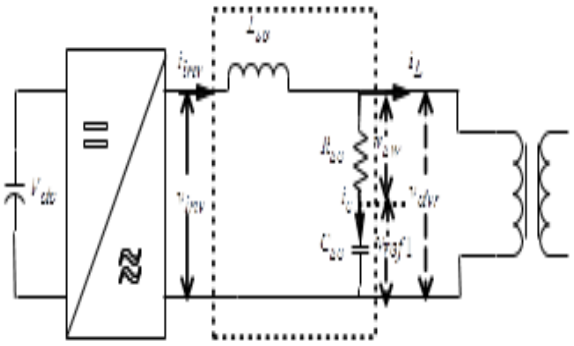


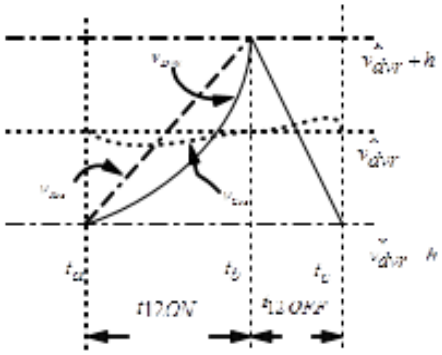


Fig..5. Schematic diagram of DVR (a) modified filter circuit, (b) Output voltage across the capacitor

C. Switching Frequency Variation:

if $v_{dvra} \geq v^*_{dvra} + h$, $+V_{dc}$ is applied across the active filter components. Now Applying KVL and KCL above filter circuit we get,

$$L_{se}\frac{di_{inv}}{dt} = V_{dc} - v_{dvr}; dt = t_{12on} \tag{8}$$

$$di_{inv} = di_{load} + di_c \tag{9}$$

Since the variation of load current compared to the capacitor current is small it is neglected. The duration of the positive slope can be derived from the above equation as in (10),

$$t_{12ON} = \frac{L_{se}di_c}{V_{dc} - v_{DVR}} \tag{10}$$

if $v_{dvra} \leq v^*_{dvra} - h$, $-V_{dc}$ is applied across the filter components. Applying KVL we get

$$-L_{se}\frac{di_{inv}}{dt} = V_{dc} + v_{dvr}; dt = t_{12OFF} \tag{11}$$

$$t_{12OFF} = \frac{L_{se}di_c}{V_{dc} + v_{DVR}} \tag{12}$$

From (10) and (12), the time duration of one switching cycle can be calculated as,

$$T = t_{12ON} + t_{12OFF} = L_{ts}di_c\frac{2V_{dc}}{V_{dc}^2 - v_{DVR}^2} \tag{13}$$

Change in capacitor current di_c can be found from the capacitor dynamics equation in (13).

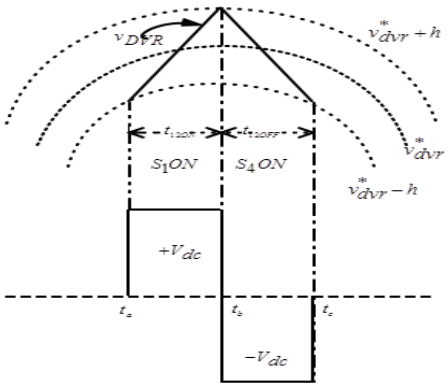


Fig.6 switching operation of band controller

Differentiating and rearranging the above equation, the change in capacitor current can be written as in equation (14)

$$di_c = \frac{1}{R_{se}}\left(dv_{dvr} - \frac{i_c t_{12ON}}{C_{se}}\right) \tag{14}$$

Assuming the reference voltages are perfectly tracking actual injected voltage, the difference between these voltages is equal to double width of the band for one switching cycle. This leads to minimum the change in capacitor voltage at high frequencies. Thus,

$$dv_{dvr} = \left(v^*_{dvra} + h\right) - \left(v^*_{dvra} - h\right) = 2h \quad \text{and} \quad \frac{i_c t_{12ON}}{C_{se}} = dv_c \approx 0 \tag{15}$$

Substituting (15) in (14), the change in capacitor current is obtained as

$$di_c = \frac{2h}{R_{se}} \tag{16}$$

The time duration for one switching cycle is found by,

$$T_{sw} = \frac{L_{se}}{R_{se}}\frac{4h}{\left[(V_{dc})^2 - \left(v^*_{dvr}\right)^2\right]} \tag{17}$$

Assuming that only fundamental component is present in reference voltage the expression for switching frequency of band controller is given eq. (18),

$$f_{sw} = \frac{R_{se}}{L_{se}4hV_{dc}}\left[(V_{dc})^2 - \left(v^*_{dvr}\right)^2\right] \tag{18}$$

From the above expression for the switching frequency the only time dependent variable is reference voltage. Rearranging (18), we get,

$$f_{sw} = \frac{R_{se}}{L_{se}8hV_{dc}}(2V_{dc}^2 - V_{mref}^2 + V_{mref}^2\cos(2\omega t)) \tag{19}$$

From equation (19) it can be concluded minimum value of switching frequency the reference voltage should reach the maximum value and maximum switching frequency occurs at zero crossing of reference voltage. The modified expressions as given below,

$$f_{sw\min} = f_{sw}\,|_{wt=\left(n\pi+\frac{\pi}{2}\right)} = \frac{R_{se}}{L_{se}4hV_{dc}}\left(V_{dc}^2 - V_{mref}^2\right) \quad \text{For n=1, 2..}$$

$$f_{sw\max} = f_{sw}\,|_{wt=(n\pi)} = \frac{R_{se}}{L_{se}4h}\left(V_{dc}\right) \quad \text{For n=1, 2, 3…} \tag{20}$$

D. Fixed Hysteresis current controller (FHCC)

This section discuss the basic operation of a switching band controller for DVR, the reference injected voltages v^*_{injabc} for the DVR are calculated using equation (7). VSI is realized by these reference injected voltages and controlled by using switching controller techniques. The switching signals for the VSI are generated using switching band controller with a fixed value of ± *h*. The switching sequence of VSI for control of DVR is given as,

if $v_{inja} \geq v^{*}_{inja} + h, S_1 = 0, S_4^{'} = 1$ (S_1 is *OFF*, $S_4^{'}$ is *ON*)

else if $v_{inja} \leq v^{*}_{inja} - h, S_1 = 1, S_4^{'} = 0$ (S_1 is *ON*, $S_4^{'}$ is *OFF*)

end

Similarly the same logic can be applied for other legs of VSI.

IV. DESIGN OF SYSTEM PARAMETERS FOR VSI AND ACTIVE FILTER

The various parameters which influence the compensation capability of DVR are DC link voltage (v_{dc}), interface inductor (L_{se}), switching Resistance (R_{se}), filter capacitance (C_{se}). First step is select the DC link voltage (v_{dc}) which is equal to 1.6 times the peak value of system line voltage (V_{lm}) in order to derive injected voltage. These injected voltages depend on filter capacitor currents whose rms value is expressed as

$$i_c = \sqrt{\left(I_{inv}^2 - I_{load}^2\right)} \quad (21)$$

From the Fig 4(a) it seen that the capacitor branch current (i_c) is divided into two independent components given as

$$i_c = \sqrt{\left(I_{c1}^2 + I_{sw}^2\right)} \quad (22)$$

Where $i_{c1}$the current corresponding to the reference injected DVR voltage and i_{sw} is the switching frequency current. The rms value of switch band voltage is given as

$$V_{sw} = V_{Rse} = I_{sw} R_{se} = \frac{h}{\sqrt{3}} \quad (23)$$

The required fundamental reference voltage drop across capacitor can be written as,

$$V_c = V_{ref1} = I_{c1} X_{c1} = \frac{I_1}{2\pi f_1 C_{se}} \quad (24)$$

Now the rms DVR voltage can be computed as

$$V_{dvr} = \sqrt{\left(V_{ref1}^2 + V_{sw}^2\right)} \quad (25)$$

A. Design of Series Active Power Filter Parameters (Capacitance (C_{se}), Switching Band Resistor (R_{se}) and Interface Inductor (L_{se}))

From Fig.4.4 the equivalent circuit of DVR the parameters for design of filter capacitor and switch band resistor can be obtained. From the above equations (23) and (24) the values of filter capacitor and switch band resistor are given as,

$$R_{se} = \frac{h}{I_{sw}\sqrt{3}} \text{ and } C_{se} = \frac{I_{c1}}{V_{ref1} 2\pi f_1} \quad (26)$$

To shape and track the reference injected voltages an interfacing inductor is necessary. The value of inductor should be design based on the switching frequency of the DVR. The values of interfacing inductor is obtained as follows,

$$L_{ts} = \frac{1}{f_{sw\max}} \frac{V_{dc}}{4h} R_{se} \quad (27)$$

V. RESULTS

After the design of VSI paramerters now compensate load voltages at PCC using modified switching band controller DVR with neutral clamped VSI as shown in Fig.1 and simulation studies is done in MATLAB. The system parameters considered for the above analysis are given in Table.1.

System Parameters

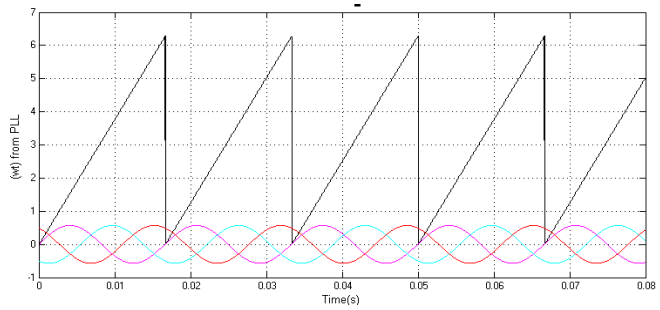
System quantities	Values
System voltages	V_m = *200 V* peak voltage, *50 Hz*
Feeder impedance	*Zs = 1+j0.314Ω*
Non linear load	Three-Phase bridge rectifier consisting of *R-L* Load (*100* Ω and *100 mH*)
Linear load	Unbalanced load: Z_{la}=*150+j31.41Ω*, Z_{lb}=*75+j31.41Ω*, Z_{lc}=*50+j3.141Ω*
VSI parameters	R_{se} =*1.2Ω*, C_{se} =*10 μF and* L_{se} = *15mH*
Coupling transformer	*10 MVA,200/200,50Hz, R=0.002 pu, X=0.6 pu*
DC link voltages	V_{dcref} =*1100 V*, C_{DC1} =*2,200μF and* C_{DC2} =*2,200μF*
Hysteresis band	*h = 10% Compensated Voltage*

The DVR is connected in series with load, the reference injected voltages are calculated using equations (1) and (7) and these reference voltages are compared with actual injected voltages using hystestersis band control which genrates switching pulses for VSI.

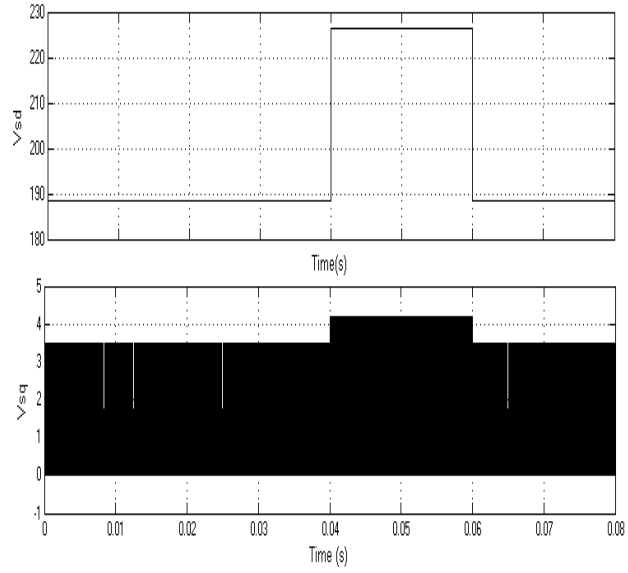
Case-1: Performance of modified controlled DVR under voltage swell occurs between interval of time 0.04 to 0.06 sec.

Fig.7 shows that the voltage compensation, performance using the proposed method at 20% swell with the combination of nonlinear load and linear load. Initially, design proper phase locked loop (PLL) is used to provide rotational speed (*wt* in rad/sec) to reference frame (*dq0*), the rotational speed shown in fig, in this particular rotational speed using in equations (1), (4) and (5) and generates the dq0 rotating reference source voltages, load voltages and generate abc refernce injected voltages. Now the neutral clamped VSI is realized by these reference injected voltages and controlled by using fixed hysteresis switching controller techniques. The switching signals for the VSI are generated using switching band controller with a fixed value of ± *h* (which is depends upon the compensated voltage, i.e., 10% compensated voltage)

The switching frequency of the VSI is calculated using eq (20), in this frequency generates signals to VSI. The DVR injects voltages (V_{dvrinj}) at PCC and compensates the swell at the load voltages and makes the voltages balanced and sinusoidal and maintain active power constant. Fig. shows the load voltages before compensation, DVR injected voltages, load voltages after compensation, error difference between reference injected (V_{dvr}^{ref}) and actual injected voltages (V_{inj}).



(a)



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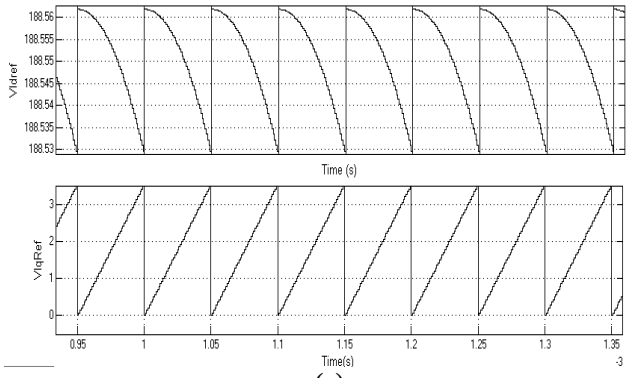

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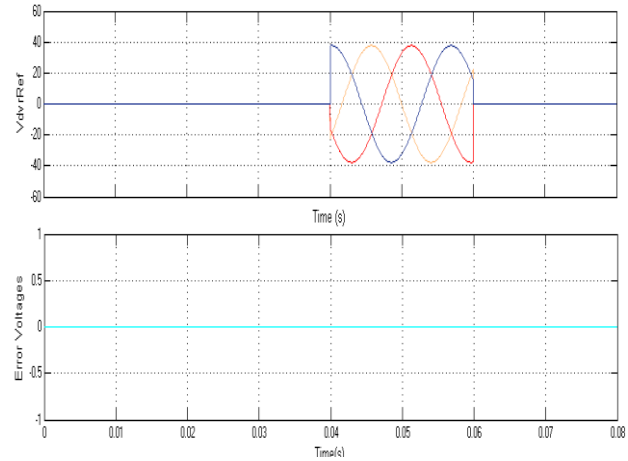
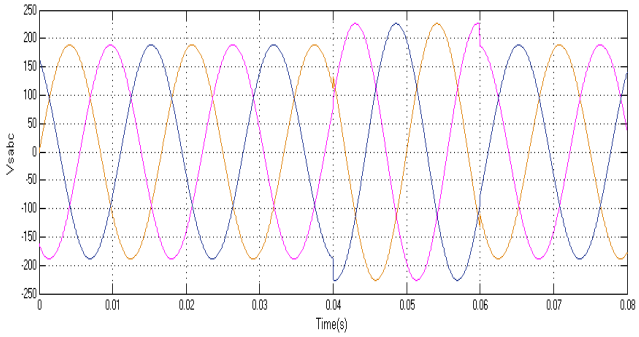
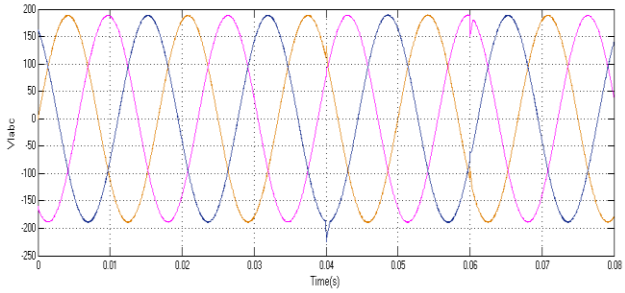


(d) and (e)



(f)

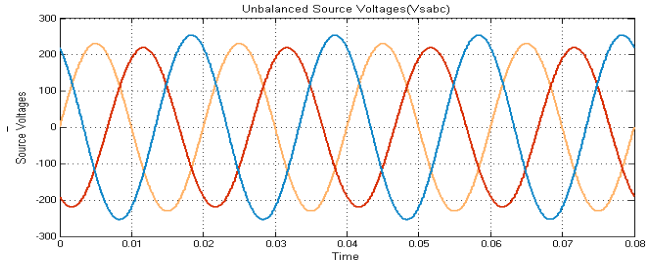


(g)

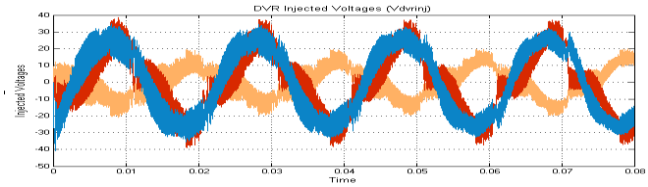
Fig.7 (a) Rotational Speed (wt) from PLL (b) *dq0* rotating reference source voltages (c) *dq0* rotating reference load voltages, (d) , (e) are injected voltages and error voltages (f) Load voltages (V_{labc}) before compensation and (g) Load voltages (V_{labc}) after compensation

Case2: Performance of modified controlled DVR under unbalanced source voltages:

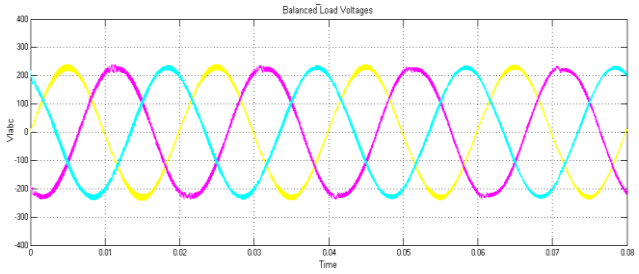
In case-2 it assumed that the source voltages are unbalanced and duration of these unbalanced voltages is in the interval 0s to 0.08s. To make these unbalanced voltages balanced at PCC using modified switching band controller based DVR. Now the DVR injects the voltages (V_{inj}) at PCC. To make the load voltages balanced. Fig.8 (a) to (c) shows unbalanced source voltages, DVR injected voltages (V_{dvrinj}), load/PCC voltages, and active power before and after compensation.



(a)



(b)

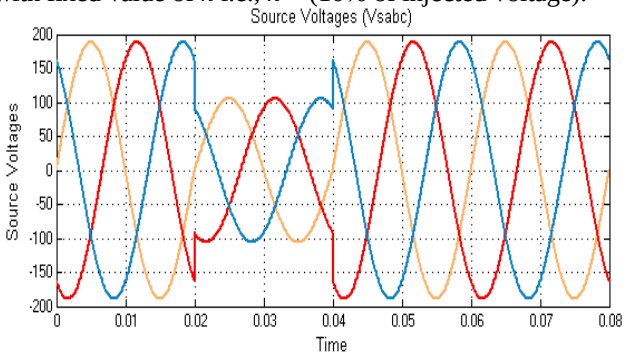


(c)

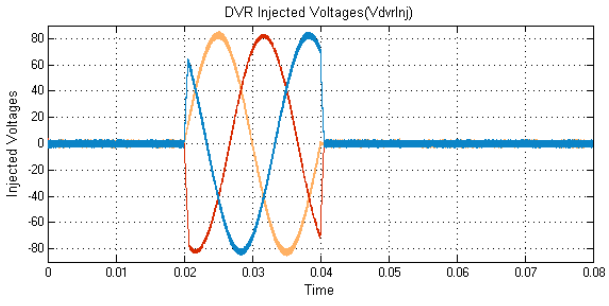
Fig.8 (a) Source voltages (V_{sabc}), (b) Injected voltages (V_{dvrinj}), and (c) Load voltages (V_{labc})

Case3: Performance of modified DVR at PCC voltage fluctuations

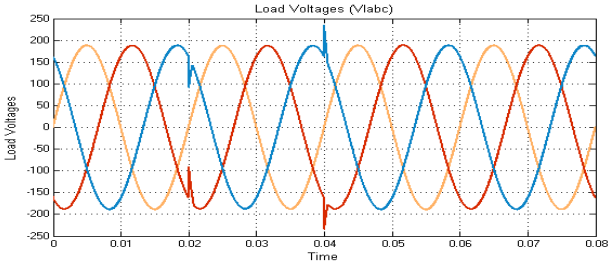
In this case a nonlinear and unbalanced load is assumed at steady state condition and the simulation studies is done for period of 0s to 0.*08 s*. In this case a sag of 40% of applied voltage without phase jump is considered in all phases. The voltage sag is created at time t = *0.02 s* and is cleared at time t = *0.04 s*, where load voltages are restored nominal values. The waveforms for source voltages and load voltages are plotted in Fig.9 (a). To regulate load voltages with help of DVR circuit using improved filter structure a band controller with fixed value of *h* i.e., *h* = (10% of injected voltage).



(a)



(b)



(c)

Fig.9 (a) Source voltages (V_{sabc}), (b) Injected voltages (V_{dvrinj}), and (c) Load voltages (V_{labc})

VI. CONCLUSION

This paper has discussed design of Modified switching band voltage control for a synchronous-reference- frame (SRF) based DVR and regulating the load voltages under different voltage related problems are presented. The modelling of modified filter circuit band controller is discussed for carrying out the simulation studies and maintain constant switching frequency with help of system parameters. It is observed from the analysis, from SRF theory generate the accurate reference injected voltages and PLL provides particular rotational speed. Switching controller i.e hysteresis band controller generates accurate injected voltages and having low error value between references injected voltages and actual injected voltages, smooth and no ripples in voltages.

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