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Design of Nanotechnology Based Hazard Free Digital Circuit using Quantum Dot Cellular Automata

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Abstract*: Currently digital circuits have a high flying role in most communications applications. In this Paper, a successful approach to risk-free circuit analysis and design using quantum dot cellular automata is explored at the Nano level. This paper, which we use for both integrated and continuous digital circuits, is a basic component of QCA circuit operation. The Quantum Dot Cellular Automata Designer Tool is very useful for designing a large risk-free circuit. So the proposed risk-free circuit is designed and simulated using this designing software utensil for three input stages. The proposed framework for the risk-free circuit requires only a small number of major gate operations compared to previous structures because of its three input levels.

Keywords: Combinational logic circuit, Sequential logic circuits, QCA, Majority gate.

I. INTRODUCTION

Logic circuits for digital systems can be joint digital circuits or continuous digital circuits. A compound circuit is represented with logic gates whose outputs are only computed from the current combination of input conditions in any case. The set of Boolean functions understood the function performed by the compound circuit. Asynchronous series circuits that use identical clock pulses at the input levels of all one bit storage elements are called clock series circuits. These circuits show bandwidth problems, and their time is easily decomposed into independent discrete steps, each of which can be analyzed separately. When a clock pulse is not active, the response loop is destroyed because the outputs of a bit of storage element cannot be switched on even if the combined logic value that drives their inputs.

Quantum Dot Cellular Automata (QCA) is a computational method for substituting field effect transistor (FET) [8] devices that was introduced by Lent et al in the beginning of 90s. and important after its fiction and experimental success using the Coulomb siege event [9]. QCA is a transistor less computational paradigm that addresses device density issues and interconnected problems.

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The two excess electrons charging the fundamental quantum point cell and counts in the Coulomb interactions of the electrons [5] [6]. Quantum dots are Nano-structures, which are made from standard semi conductive materials. These structures are conceived as quantum wells. By using quantum dot cellular automata instead of interconnecting wires, cells can transmit information throughout the circuit [10]. The input majority gate and inverter are the two most important operators used in QCA technology. The majority of gates and inverters can only be built to carry out any QCA circuits.

II. QCA BUILDER

Circuit Builders need a more precise simulation and design layout tool to determine the operation of QCA circuits. QCA Building Tool is a publicly available building and simulation tool for quantum dot cellular automata developed at the ATBS Laboratory in the University of Calgary. The QCA designer Tool is currently supports three different simulation machines and several CAD features required for complex circuit design[3] [4]. The first shows which cell must be polarized or which cell must be fully polarized through its digital logic simulator. The next is a linear approximation machine[12], which uses the non-linear cell-to-cell response function to re-determine the steady state of cells within a structure. The third two-state Hamiltonian uses the approximation of the full quantum mechanical model of such a system. [3][4].

III. QCA FUNDAMENTALS

A. QCA cell

One of the basic units of the QCA is the QCA cell made up of four quantum dots in the corners of a square, where two electrons live. Electrons are quantum mechanical particles that can mine between points in a cell. QCA cell is the basic unit of QCA and made up of four quantum dots in the corners of a square, where two electrons live. Electrons are quantum mechanical particles that can mine between points in a cell. The next to each other placed electron in the cell will interact. Due to this interaction, the polarity of a cell is affected directly by the polarization of the neighboring cells. Cell polarization is used to denote binary information logic 1(P=+1) and binary information logic 0 (P = -1) respectively [6]. QCA cell polarization is shown in Figure 1.

P = +1 P = -1

Figure 1: QCA cell polarization

B. QCA Logic Devices Majority gate (MG) and inverter are the fundamental logic elements available with QCA. Normally the Digital circuits are generated using a combination of Majority gate and inverter.

C. QCA Wire

In the tool, the QCA wire with the support of electrostatic repulsion and not current flow, helps propagate logic conditions. In the QCA wire, due to the electrostatic interactions between the cells, the binary signal is transmitted from the input to the output [5][7]. Figure 2.a and 2.b shows the distribution of the 90 ° and 45° QCA wire. In the place of the 90 ° QCA wire, a 45 ° QCA wire may be used. Generally the design consists of originating binary signal changes between two coordinates.

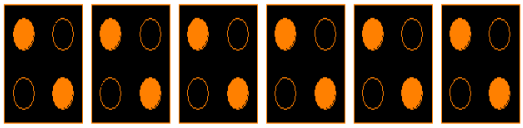

Figure 2.a: 90° QCA wire.

Figure 2.b: 45° QCA wire.

D. QCA Reverser

The QCA reverser is shown in Figure 3 with its different structure. This is caused usually by the corner touching cells. The electromagnetic interaction of the cells is reversed because the quantum-points related with the different polarizations are misaligned between the cells [2][7]. The reverser is built by neighboring QCA cells in the diagonal, which causes the Coulomb forces to place two electrons in the cell's wells as opposed to the source.

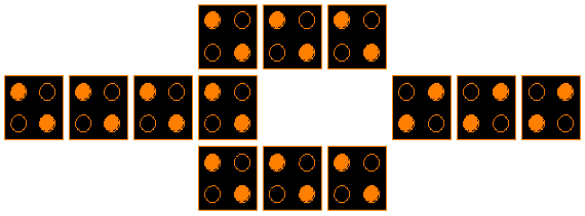

Figure 3.a: QCA Reverser

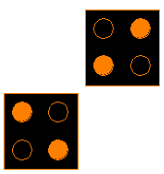

Figure 3.b: QCA two cells Reverser

Figure 3 QCA Reverser

E QCA Majority Gate

The bulk gateway generates an output that reflects most entries. The QCA majority gate contains three input terminal cells and one release cell. The three input cells are X, Y and Z, the majority being the login function of the gate is

$$Maj(X,Y,Z) = XY + XZ + YZ. \quad (1)$$

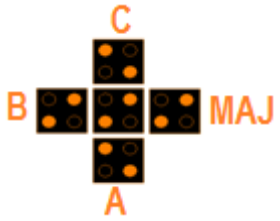

Figure 4.a: QCA majority gate

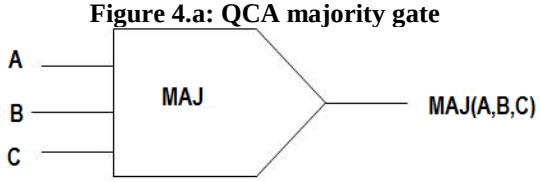

Figure 4.b: Majority gate Symbol

Figure 4: Majority Gate

The Figure 4 shows the most basic QCA majority gate. The drive to get to the land of the majority device ensures that it takes over the most of its neighbours polarization. Most of the device cell follows the polarization because it represents a very low energy state. The polarity of an input to the QCA majority gate and AND & OR gate function use binary logic 1 and binary logic 0 respectively. The mathematical implementation of the above functions would be written as follows:

$$Maj(A, B, 0) = A.B \quad (2)$$

$$Maj(A, B, 1) = A+B \quad (3)$$

Therefore, by using three input majority gates all QCA logic circuits can be created. Normally the digital circuits are fabricated with the support of majority gate designing techniques to create a well-organized QCA format [1].

IV. HAZARD FREE CIRCUITS

To design asynchronous series of circuits, one must be careful to comply with precautions and restrictions to ensure that circuits are operating properly [11]. With only one input change at any time, the circuit must be operated in a basic manner and free from important races. Additionally, there is another phenomenon called risk, which causes the circuit to crash. Threats are redundant switching transistors that may appear in the output of a circuit due to different paths that exhibit different propagation delays. There are risks in combined circuits that can produce a temporary false-output value. When this condition occurs in an asynchronous serial circuit, it can create an incorrect state.

A. Hazard in combinational circuits

Risk is a situation in which a variable change produces a temporary change in output when there is no change in the output. Suppose that the following circuits shown in Figure 5 are at risk.

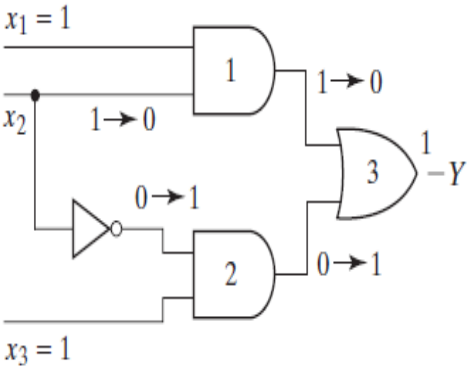

Figure 5. Combinational Logic circuit with hazard

Suppose all three input conditions are initially equal to 1. Then rely on the change of x 2 from 1 to 0. If propagation through the fill circuit is taken into account, the output may temporarily go to 0. Boolean function of the round product is inscribed. When this type of execution output is 0, it can be 1. This is called standard 1-risk. If executed in round-product sums, the output is temporarily 1, while it is 0. This is referred to as the standard 0- risk.

Another type of risk, known as dynamic risk, is that when the output is changed two or three times, it must change from one to zero or zero. Analysis of maps of specific circuits can identify risk. The solution to mitigate risk is to combine the words of two groups with another min term word and another question period.

B. Hazards in Sequential Circuits

Let us consider the asynchronous series circuit shown in Figure 6 below. In asynchronous series circuits, clock pulses are not used. The change of the internal state occurs when there is a change in the input variable. Their memory components are time delay components or unopened flip-flops and they often simulate joint circuits with feedbacks. Their set is more difficult than a set of synchronous circuits in the clockwise direction. They are used when the speed of operation is considered as important. The interaction of the two units must be designed by asynchronous circuits as each unit has its own independent clock.

$$Y = x_1 x_2 + x_2' y$$

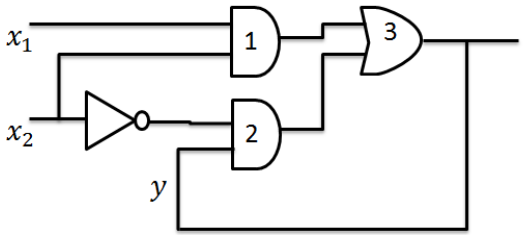

Figure 6. Sequential Logic Circuit with hazard

If the circuit total yx1x2 = 111 and the input x2 becomes zero, the next total state must be 110. However, because of the risk, the output Y may be temporarily 0. If the fault signal returns, the output of gate 2 fill circuit before switching to gate 2, the output of gate 2 will be 0, and the circuit will switch to fault total 010. This can be removed by adding an additional gate.

V. QCA IMPLEMENTATION

Quantum dot cellular automata calculation continues by orienting cells based on the polarization of neighboring cells. Quantum Dot Cellular Automata Reverser The neighbor in the diagonal is built of quantum dot cellular automata cells, which allow the Coulomb compared to the source for opposing, it forces to place two electrons in the wells.

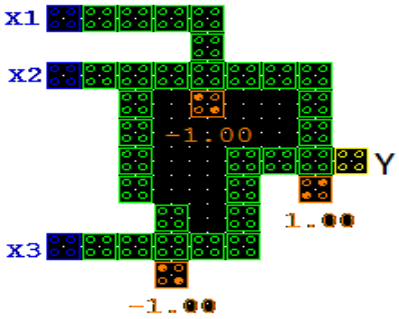

Figure 7. QCA implementation of combinational logic circuit with hazard

The joint risk-free circuit is designed with four inlet majority gates and one Reverser. Similarly, the designed continuous circuit consists of an inverter and three input majority gate. The Figure 7, 8 shows the QCA implementation of the combined circuit and continuous circuit.

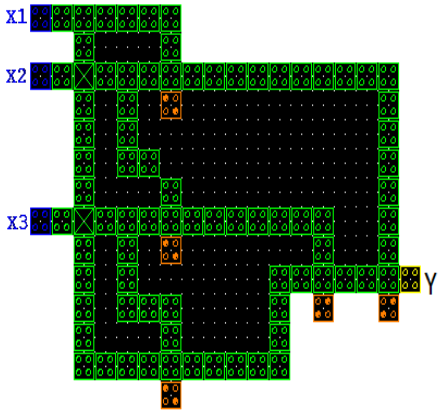

Figure 8. QCA Circuits implementation [combinational logic circuit with hazard free circuit]

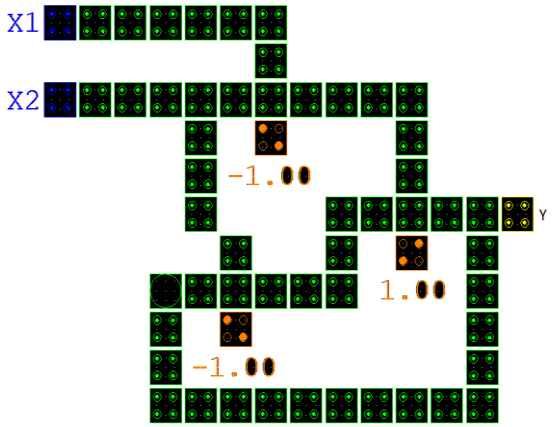

Figure 9. QCA implementation of sequential logic circuit with hazard

In combined circuit operation, the total number of cells required is 36 cells, 218.69 nm x224.69 nm area and continuous circuit activation, total number of cells required is 57 cells, 314.20nm x218.12 nm area. The total number of cells 90 and 397.43nm x305.23 nm is shown in Figure 8 for the risk-free joint logic circuit.

VI. SIMULATION RESULTS

The combined logic risk free circuit and continuous logic risk hazard circuit function are checked using the QCA tool - Designing and Simulation (Version 2.0.3). The digital joint logic risk free circuit is shown in Figure 10 and the continuous logic risk cost circuit is shown in Figure 11. Joint and continuous logic circuits have four clock zones. Clock 0 is used initially to receive the A and B entries.

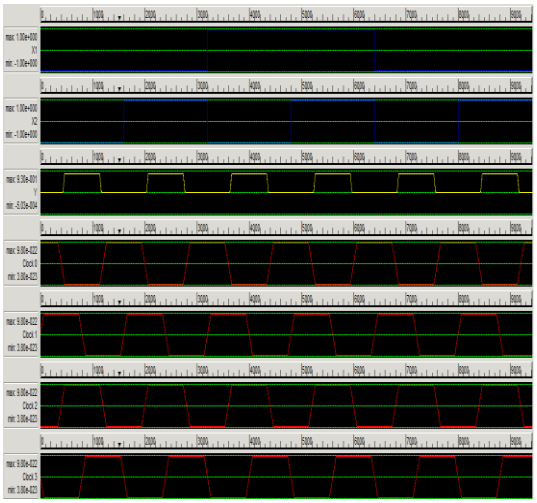

Figure 10. Simulation result of combinational logic circuit with hazard free

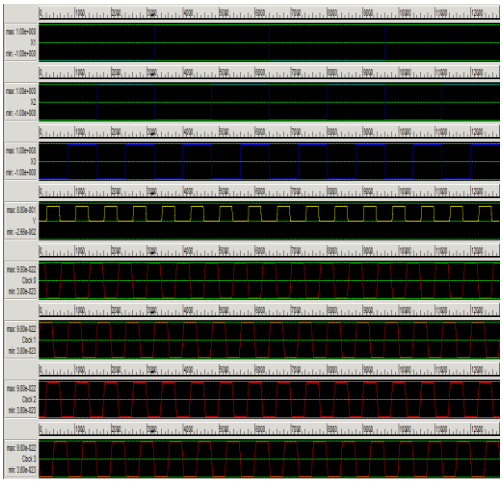

Figure 11. Simulation result of sequential logic circuit with hazard

VII. CONCLUSION

The design approach and implementation of a joint and continuous risk-free circuit is presented in this research work. The joint and continuous risk-free circuit implementation has been designed, structured and tested using QCA Designer software. The proposed layout for joint and continuous logic risk-free circuits is significantly smaller than circuits that are using CMOS technology, and reduces the area and complexity of the circuit than previous QCA circuits. The structured QCA circuits can be used to represent for three input information levels only.

REFERENCES

1. Ganesh,EN, Lal Kishore and Rangachar, MJS, "Implementation of Quantum cellular automata combinational and sequential circuits using Majority logic reduction method", International Journal of Nanotechnology and Applications. Volume 2,1, 2008.
2. Townsend, WJ, and Abraham,JA, "Complex gate implementations for quantum dot cellular automata," in Proceedings of 4th IEEE Conference of. Nanotechnology, pp. 625–627, 2004.
3. Walus,K, Schulhof,G and Jullien,GA, "High level exploration of quantum-dot cellular automata (QCA)," in Conference proceedings of 38th Asilomar Conference on Signals, Systems and Computers, vol. 1, pp. 30–33, 2004.
4. Walus,K, Dysart,T, Jullien,G and Budiman,R, "QCADesigner: A rapid design and simulation tool for quantum-dot cellular automata,", IEEE Transaction on Nanotechnology., vol. 3, 1, pp. 26–29, 2004.
5. Heumpil Cho, and Swartzlander,EE, "Adder Design and Analyses for Quantum-Dot Cellular Automata", IEEE Trans. Nanotechnology., Vol.6,3, 2007.
6. Walus,K, Jullien, G.A. and Dimitrov,V, "Computer arithmetic structures for quantum cellular automata",. Asilomar Conference on Signals, Systems, and Computers, 2003.
7. Walus,K, Schulhof, G, Jullien,GA, Zhang,R and Wang,W, "Circuit design based on majority gates for applications with quantum-dot cellular automata," in Conference Proceedings of 38th Asilomar Conf. Signals, Systems and Computers, vol. 2, pp. 1354–1357, 2004.
8. Walus,K, Jullien,GA, Dimitrov,VS, "Computer Arithmetic Structures for Quantum Cellular Automata", Asilomar Conference on Signals, Systems and Computers, Pacific Grove, 2003.
9. Wang, W, Walus,K, Jullien,GA, "Quantum-Dot Cellular Automata Adders" Copyright IEEE Nanotechnology Conference, , 2003.
10. Zhang,R, Walus,K, Wang,W and Jullien,GA, "A method of majority logic reduction for quantum cellular automata," IEEE Trans.Nanotechnol., vol. 3,4, pp. 443–450, 2004.
11. Lilly Beaulah,H,Thangaraj,K and Chitra,M, "Design of a New Energy Efficient L4 Leach Protocol based Visual Sensor Network for Forest Monitoring System", Asian Journal of Research in Social Sciences and Humanities (AJRSSH), Vol 6, issue 7, pp. 662-671, 2016
12. Gomathi,M, Shanmugaraja,P, Ilanchezhian,P, Thangaraj,K, and Komalavalli,D, "Analysis of Social Media Community Using Optimized Clustering Algorithm ",Proceedings of the International Conference on Intelligent Computing Systems , 2017

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