

Design and Implementation of Perceptron Neuron in Machine Learning for Handwritten Character Recognition



Nitesh Reddy M, Sakthivel R, Sharath Reddy M, Varun Hemanth L

Abstract: Due to the exponential increase of electronic devices that are connected to the Internet, the amount of data that they produce have grown to the same extent. In order to face the processing of these data, the use of some automatic learning algorithms, also known as Machine Learning, has become widespread. The most popular is the one known as neural networks. These algorithms need a great deal of resources to compute all their operations, and because of that, they have been traditionally implemented in application specific integrated circuits. However, recently there have been a boom in implementations in field programmable gate arrays, also known as FPGAs. These allow greater parallelism in the implementation of the algorithms. Field Programmable Gate Arrays (FPGA) implementation based feature extraction method is proposed in this paper. This particular application is handwritten offline digit recognition. The classification depends on simple 2 layer Multi-Layer Perceptron (MLP). The particular feature extraction approach is suitable for execution of FPGA because it is utilized with subtraction and addition operations. From Standard database handwritten digit images of normalized 40x40 pixel the features are extracted by the proposed method. It has been discovered by experiential outcomes that 85% accuracy is achieved by proposed system. Overall, as compared to other systems, it is less complex, more accurate and simple. Further this project explains IEEE-754 format single precision floating point MAC unit's FPGA implementation which is utilized for feeding the neurons weighted inputs in artificial neural networks. Data representation range is improved by floating point numbers utilization to a higher number from smaller number that is highly suggested for Artificial Neuron Network. The code is developed in HDL, simulated and synthesis results are extracted using Xilinx synthesis tools. In order to validate its computational accuracy of the FFT, an MATLAB validation script is used to verify the output of HDL with standard reference model.

Keywords: FP MAC Unit, Handwritten character recognition, Machine Learning, Multilayer Perceptron

I. INTRODUCTION

Pattern recognition, computer vision, and artificial intelligence has a research field namely, handwritten character recognition. The computer that performs handwriting recognition has the ability of acquiring and detecting characters in touch-screen devices, pictures, paper documents and other sources, then these are converted into machine-encoded form. Their applications are discovered in OCR as well as other character recognition systems that are intelligent and advanced. Also, machine learning methods are being implemented by these systems like neural network. Artificial intelligence's branch i.e. machine learning motivated by biology and psychology which deal with learning from data set as well as various spectrum issues are solved by it. In a model of supervised machine learning data instances are provided precise for a problem area as well as a solution that simplifies every instance's problem. After completion of learning, model gives data solutions as per learning as well as with higher precision unseen data is also solved. In machine learning, learning models used are neural networks. They aim in stimulating the learning process which happens in neural system of human or animal. They are utilized in task automation, as they are highly robust learning models, where human decision is imprecise or takes too long. Results are delivered very fast by neural network and data instances' connections are observed that are missed by humans. A neural network is implemented using Hardware description language that recognizes characters from images provided as inputs. After acquiring the knowledge which is described in text, then on a low level, implementation of neural network is done without use of libraries through which process is facilitated. Through this, through this, in a specific problem neural networks' performance is evaluated and for the network source code is provided which is utilized in solving the various classification issues. The resulted system is complex ICR or OCR system's subset.

Neural networks are a type of machine learning algorithm that were created with the intention to mimic the biological function of neurons in the brain [1]. In this biological sense, the primary purpose of neurons is to process and communicate information with each neuron conveying information through "synapses" to other neurons. These are the fundamental units of the nervous system and human brain alone are extensively large with over 100 billion neurons as well as 100 trillion synapses.

Revised Manuscript Received on August 30, 2020.

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These interconnections form networks to accomplish their motor and sensory tasks effectively and efficiently over time as networks and neurons are refined and strengthened [1].

According to what John McCarthy said in the 1950s, Artificial Intelligence (AI) is “the science and engineering of creating intelligent machines that have the ability to achieve goals like humans do” and moreover Neural Networks are a wide part of AI. Also in the 1950s, specifically in 1959, Machine Learning (ML) is described by Arthur Samuel, which is a category included in AI, as “the field of study that gives computers the ability to learn without being explicitly programmed”. This means that a single program can be used for many different ML applications as it will learn how to solve these problems in contrast to purpose-built algorithms, which only perform in a single scenario. It is achieved by the use of training processes instead of customizing the program with a hit-or-miss approach.

a). Floating Point Mac Unit

Generally, comprises of accumulator multiplier and adders. The inputs are fetched from memory location which are given to the MAC and then inputted to MAC block's multiplier that does multiplication as well as provides the adder with result which then adds the results and saves in memory location. Only one cycle is required for achieving the complete process.

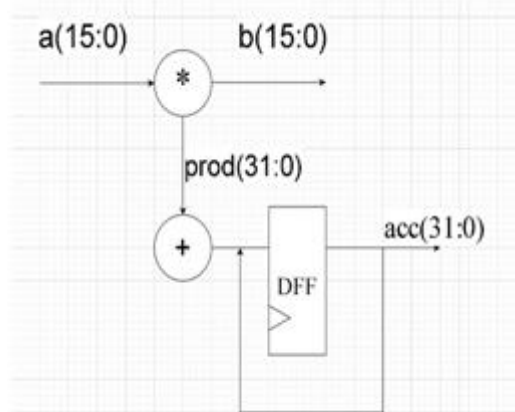


Fig. 1: Block Diagram for Mac Unit

II. LITERATURE SURVEY

In various application areas, particularly, in speech and image recognition, as compared to conventional machine learning techniques, deep learning has outstood [1], [2]. The deep learning's excellence results in various evolving real-world applications' exploration like, drug discovery and toxicology [5], automatic machine translations [4], and self-driving systems [3]. The deep learning depends on the DNN's (deep neural network) structure that comprises of several types' multiple layers and every layer has neurons from hundreds to thousands. It has been revealed by the latest evidence that for the deep learning's success, depth of network has key significance and for the ImageNet dataset, several deep learning models has 16-30 layers [1]. Substantial enhancement were achieved by deep learning in overall accuracy by obtaining high-level and complex features at substantial up-scaling cost in size of model. In the period of big data that worked through embedded systems, semiconductor technology's development

becoming an essential with development in functionalities. Similarly, globally, researcher from industry and academia has given considerable resources and efforts for investigating, improving, and promoting the deep learning applications in embedded system [6]. Memory requirement and computational complexity is increased by DNNs with large model size and deep layered structure, in spite of DNN recognition accuracy advantages.

During the deep learning model deployment on embedded systems below challenges are faced by researchers:

Limited by the embedded systems' communication bandwidth that are generally mobile terminals, downloading of DNN model of large-sized is a challenge that are trained offline in datacenters.

The deep learning model's large size is contributed by N. Liu and S. Lin. They imposed severe requirements on embedded systems' memory size and computing resources. Such issues gives motivation and thus deep learning model with reduced-size is implemented with almost no accuracy loss. In reality, there exists over-parameterization of state-of-the-art DNNs, thus, in the deep learning models redundant parameters are removed and the overall accuracy produces is similar to original models [1]. Furthermore, several there exists investigation on deep learning model compression methods, by encouraging from such finding [6]–[10], it includes weight matrix factorization, network pruning, weight precision reduction, etc.

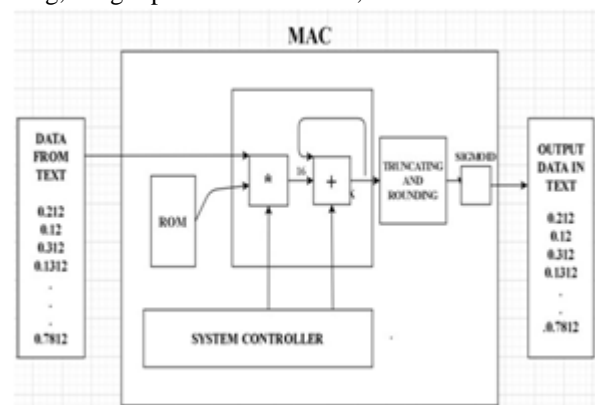


Fig.2: Block diagram of a perception prediction circuit using MAC

Character recognition subordination, pattern recognition regulation's conventional research area is digital recognition. As per various classification standards, digital recognition is characterized into print form and handwriting digital recognition, online and offline recognition, etc. [1]. The handwritten digits recognition is a field that has been studied deeply as there are several aspects to which it can be applied, like bank bills' automated processing, identification of post code, etc. recently, a great development has shown by the offline handwritten digit recognition. But as handwritten digit's writing style differs from human to human, offline handwritten digit recognition hardly recognizes human's digit recognition in fault tolerance, flexibility and accuracy [2].

Each algorithm has its benefits, but each of them concentrates on single number recognition with overall situation's weak control. From artificial intelligence's point of view, studying the people's thought is a good idea when handwritten numbers are identified by them and then existing algorithms can be improved for increasing the handwritten numbers' recognition rate [3]. Thus, in this paper, a research is carried out on handwriting recognition. Various solutions has been given and many achievements are acquired by the various scholars and experts for handwriting image recognition. In the 1920s, OCR's theoretical concept is presented by the Tausheck and in the following years OCR technology is implemented and applied by Handel for intellectual property rights [4]; with the template matching algorithm over 1,000 characters were identified and classified by Casey and Nagy. Also, DBN (Deep Belief Network) is presented in literature by Hinton [5], which has 2.25% error rate after its training. Although, network structure of DBN has poor real time performance, great time complexity and is complicated. In literature a Dropout technology has been proposed by Hinton for reducing algorithm complexity as well as solving the over-fitting issue by enhancing the neural network's hidden unit's participation in the algorithm [6].

In 1980s, digital recognition is initiated in China, and after several development years, there exists various digital identification means and methods that are categorized in 2 categories: structure-based feature analysis and statistical analysis depending on entire condition [7]. The structure-based feature analysis identifies various digits specifically from character and digits shapes outline which includes horizontal length, arc, endpoint, circle, etc.; the statistical analysis depending on entire condition recognizing various digits by mathematical manipulation, feature points, pixel density, and template matching. Recently, world witnessed various systems and theories for digital identification: Lv Rong et al., Wang Yongqian primarily studied the BP neural network based digit recognition method.

Initially, segmentation and refinement of digital characters are performed which results in generation of training samples. Then digital training samples are used to train the neural network. Lastly, untrained digital samples are identified with help of trained BP neural network. After testing, digital recognition's accuracy rate is nearly 95%. A new digit recognition method is presented by FU Yuqing, Wang Maoxiang and Huang Xinye. Depending on structural features analysis, algorithm achieved higher rate of recognition. Depending on algorithm as well as examining by recognition module, the feature extraction module and the image pretreatment module, results in development of a digital identification system. Furthermore, system's recognition ability is tested and good outcomes are obtained [8]. Also, a program for realizing the FPGA-based handwriting image recognition algorithm is designed in this paper.

III. PROPOSED METHODOLOGY

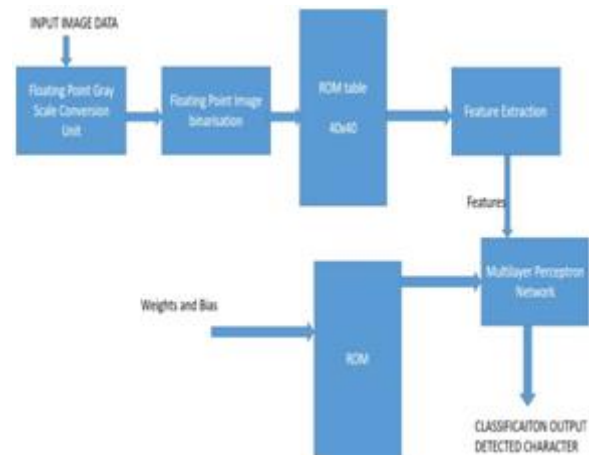


Fig.3. Proposed Architecture

The Above figure shows the overall design of the system, all the modules are designed using Floating point arithmetic which is discussed in the next section. FPU Gray Scale conversion:

Digital camera image is in RGB format. But, image is transformed into gray scale format for post processing. It results in simpler processing.

The need for converting to Grayscale is to reduce the processing time for the Algorithms, RGB Images are not required to Processing,

$$\text{Intensity} = 0.2989 * \text{red} + 0.5870 * \text{green} + 0.1140 * \text{blue}$$

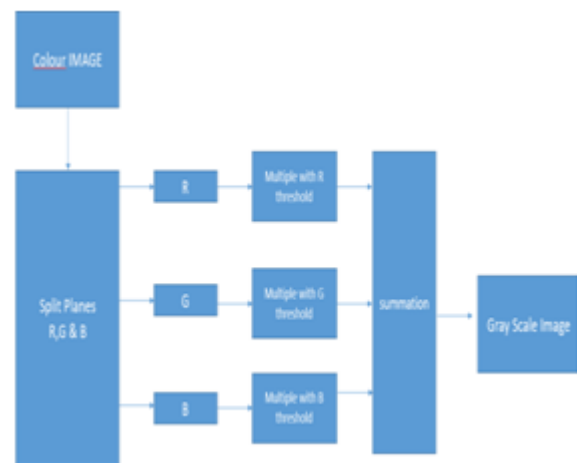


Fig.4. FPU Gray Scale conversion

a.) FPU Image Binarization:

Generally, document image analysis systems has the initial step of Binarization in the preprocessing which resulted in binary image from conversion of gray-scale image. Also, image enhancement stage is also important because the quality of collections of historical document are very low.

b.) Feature Extraction Method:

Two approaches are combined for feature extraction method. These approaches are as: by utilizing this feature extraction method 11 features are extracted.

These are integer features as well as only subtract and add operation can be implemented on FPGA. Furthermore, on FPGA, parallel execution of these approaches are done. This method is implemented with HDL language. For implementation of this method, 10 parallel processes are used.

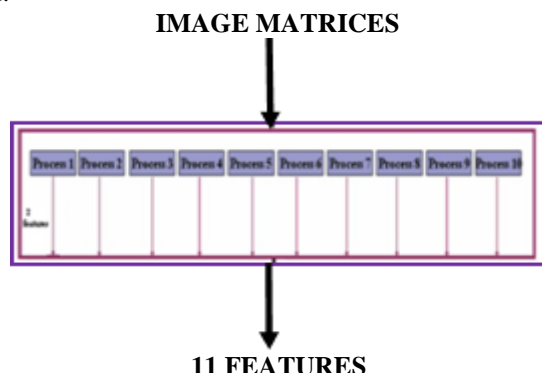


Fig.5.Feature Extraction Block

Binary images' pixel values spatial distribution is represented by using a statistical approach for comparing various white pixels on digit image's right and left halves as well as lower and upper halves. Usually, for digits typing this approach is used. Generally, as compared to right halves, left halves are bigger of some typed digits that has similar size and font. Some digits have lower halves same as upper, some has lower halves greater than upper, some has upper halves greater than lower, some has same right halves and left halves, and some has greater than right halves. For typed digits' pattern recognition, this is a suitable feature but it proved to be useful in handwritten digits when other features are also combined with it. Reason behind this is that digit's middle and picture's middle, in normalized handwritten pictures, are not compatible (represented in Figure 6.). On FPGA implementation, this feature is simple. In image's different areas (left and right of picture's middle, and picture's top and middle), only white pixels must be counted.



Fig.6. Handwritten Text

IV.RESULTS AND DISCUSSION

Each test cases have two 32-bit floating value and it is desired to calculate the product output of the multiplication event carried out on the two operands

No	Din1	Fp.hex	Din2	Fphex	Dout	Hex	Pr.out
1	445.6 5	0x43d e333	745. 8	0x443 a71ec	332356.81 25	0x48a24 89a	0x48 a786 b

2	821.2 3	0x444 d4eb8	345. 32	0x43a ca8f6	283587.093 75	0x488a7 863	0x48 8a786 4
3	1001.11 1	0x447 a471b	1234 45	0x449 a4e66	1235821.3 75	0x4996d b6b	0x49 96db6 b



Fig.7.waveform for test case 1



Fig.8.waveform for test case 2

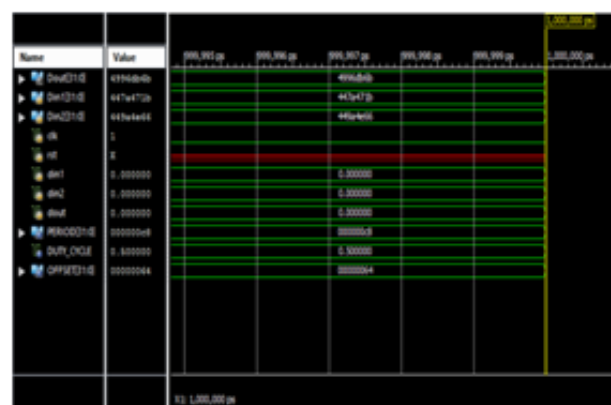


Fig.9.waveform for test case 3

Below application is developed in MATLAB for a single neuron computation

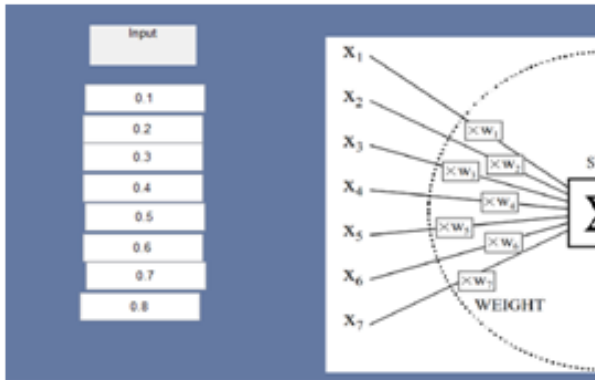


Fig.10. Part of the Matlab model

We can give the random inputs for this computation. Weights are also assumed for the computation purpose and we may also try to generate the weights randomly for this purpose

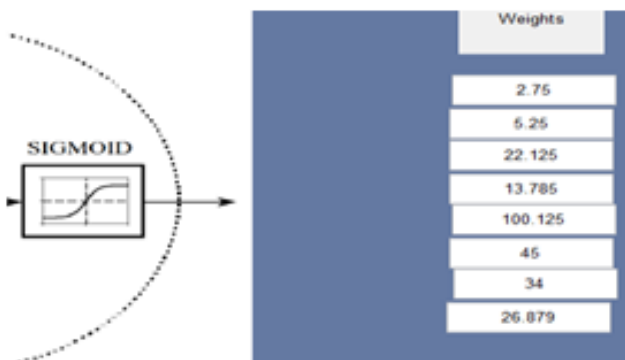


Fig.11. Part of the Matlab model

The complete hidden layer outputs are generated, by utilizing hidden layer biases and weights with all training dataset vectors.

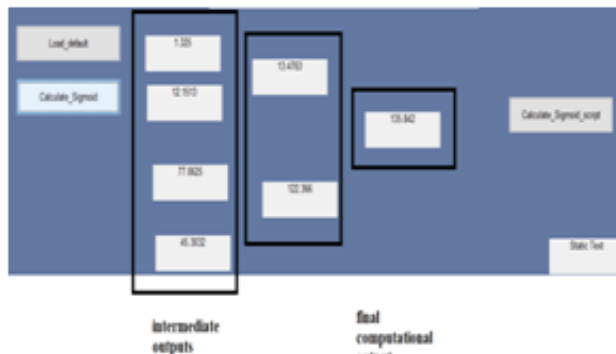


Fig.12. Output of the Matlab Model

The Final Output of 135.842 is obtained for these values of weights and inputs. This value can be used to verify the values or outputs obtained through Verilog coding. Below is an output obtained for the above taken weights and inputs

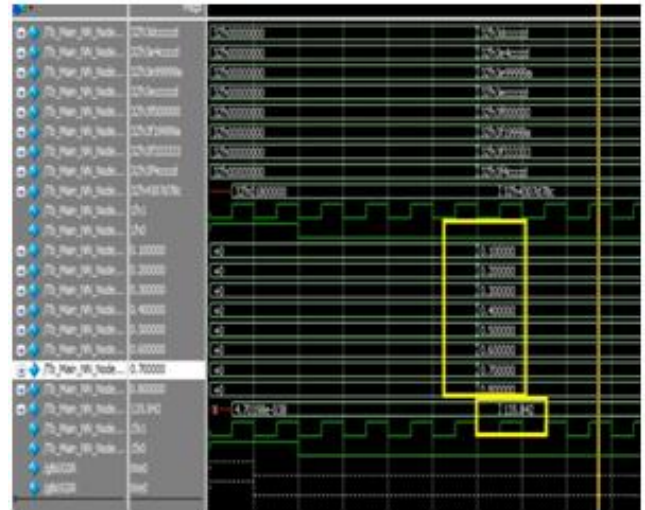


Fig.13. Verilog Simulation Result

Output obtained from simulation is 135.842 for the given set of inputs and weights

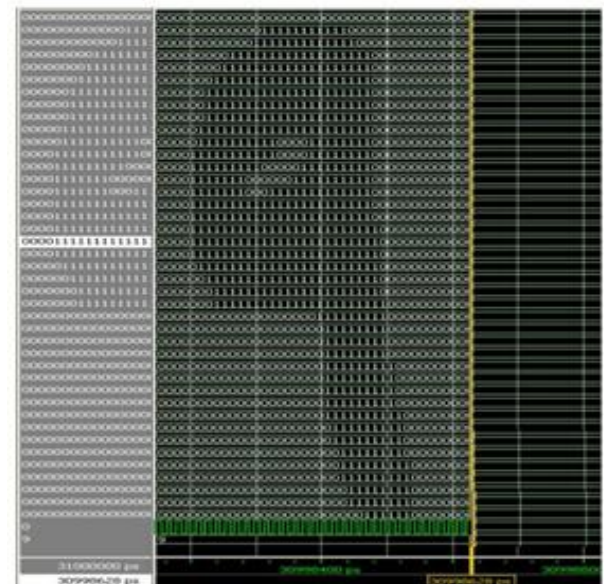


Fig.14. Simulation for ROM array storing handwritten digit

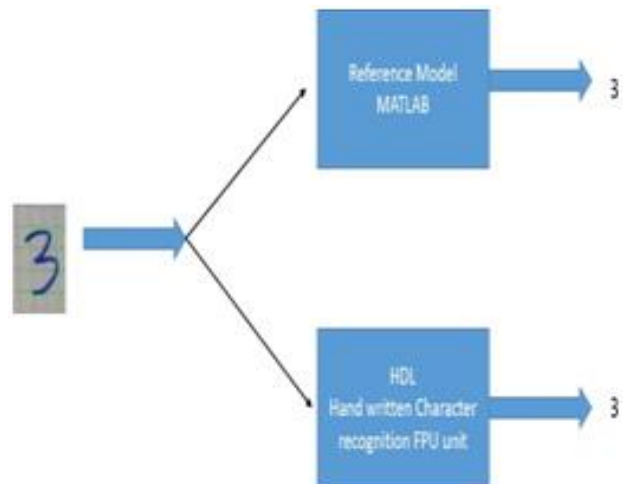


Fig.15. Validation Setup

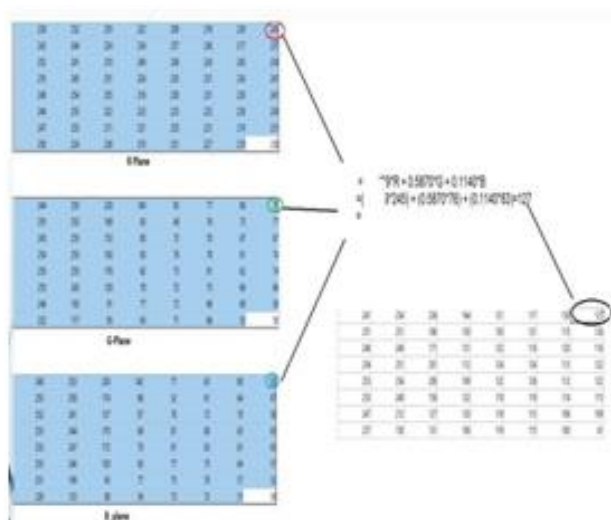


Fig.16. Results Color Conversion (RGB to Gray)

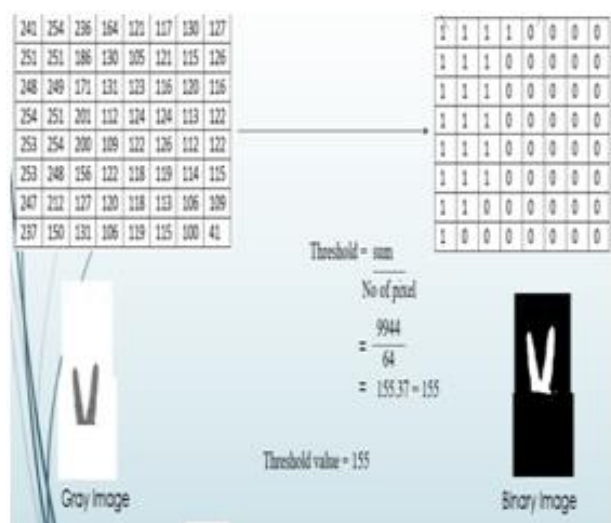


Fig.17.Gray to Binary Conversion

Sl no	Test image	HDL classifier	Result
1		1	pass
2		2	Pass
3		3	Pass

Fig.18.Results Verification

V.CONCLUSION

A FP adder and a FP multiplier, FPU MAC, Neuron and a prediction circuit are presented in this work. In pipeline architectures, they are available and are fully synthesizable and HDL is used for their implementation. After that, floating point adder and multiplier are used for

designing the complete MAC unit as well as perform its FPGA implementation. Furthermore, inputs to a neuron is fed by this MAC Unit in Artificial Neural Networks.

This work presents combined approaches of Image processing feature extraction methods. These methods are executed parallel on FPGA. By implementation of this method, we obtained an appropriate accuracy in HDL-Based handwritten digit recognition system. For classification, a simple MLP classifier was used that in the hidden layer has few neurons. Through this method's implementation, in comparison to hardware handwritten Latin recognition system more accurate system is obtained.

HDL code for FPU color conversion, Binarization, character recognition has been designed in this project work. The project has a wide range of scope in the area of, Machine Learning, Computer vision based applications. This can be targeted onto an FPGA and verified as part of the future scope

REFERENCES

1. K. He, X. Zhang, S. Ren, and J. Sun, "Deep residual learning for image recognition," in Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition, 2016, pp. 770–778.
2. A. Graves, A.-r. Mohamed, and G. Hinton, "Speech recognition with deep recurrent neural networks," in Acoustics, speech and signal processing (icassp), 2013.
3. IEEE International Conference on. IEEE, 2013, pp. 6645–6649.
4. B. Huval, T. Wang, S. Tandon, J. Kiske, W. Song, J. Pazhayampallil, M. Andriluka, P. Rajpurkar, T. Migimatsu, R. Cheng-Yue et al., "An empirical evaluation of deep learning on highway driving," arXiv preprint arXiv:1504.01716, 2015.
5. R. Collobert and J. Weston, "A unified architecture for natural language processing: Deep neural networks with multitask learning," in Proceedings of the 25th international conference on Machine learning, ACM, 2008, pp. 160–167.
6. R. Burbidge, M. Trotter, B. Buxton, and S. Holden, "Drug design by machine learning: support vector machines for pharmaceutical data analysis," Computers & chemistry, vol. 26, no. 1, pp. 5–14, 2001.
7. S. Han, H. Mao, and W. J. Dally, "Deep compression: Compressing deep neural networks with pruning, trained quantization and Huffman coding," arXiv preprint arXiv:1510.00149, 2015.
8. A. Ren, Z. Li, C. Ding, Q. Qiu, Y. Wang, J. Li, X. Qian, and B. Yuan, "Sc-dcn: Highly-scalable deep convolutional neural network using stochastic computing," in Proceedings of the Twenty-Second International Conference on Architectural Support for Programming Languages and Operating Systems. ACM, 2017, pp. 405–418.
9. Y. LeCun, J. S. Denker, S. A. Solla, R. E. Howard, and L. D. Jackel, "Optimal brain damage," in NIPS, vol. 2, 1989, pp. 598–605.
10. L. Y. Pratt, Comparing biases for minimal network construction with back-propagation. Morgan Kaufmann Pub, 1989, vol. 1.
11. Mohamed Al-Ashrafy, Ashraf Salem and Wagdi Anis, "An Efficient Implementation of Floating Point Multiplier," proceeding of 2011 IEEE.
12. Guillermo Marcus, Patricia Hinojosa, Alfonso Avila and Juan Nolasco-Flores, "A Fully Synthesizable Single-Precision, FloatingPoint Adder/Subtractor and Multiplier in VHDL for General and Educational Use", Proceedings of the Fifth IEEE International Caracas Conference on Devices, Circuits and Systems, Dominican Republic.
13. Xilinx Inc, ISE, at <http://www.xilinx.com>.
14. Behrooz Parhami, Computer Arithmetic: Algorithms and Hardware Designs, 1st ed. Oxford: Oxford University Press, 2000
15. John G. Proakis and Dimitris G. Manolakis (1996), "Digital Signal Processing: Principles. Algorithms and Applications", Third Edition.
16. Patterson, D. & Hennessy, J. (2005), Computer Organization and Design: The Hardware/software Interface, Morgan Kaufmann.

17. Mentor Graphics Inc, FPGA Advantage, at <http://www.mentor.com/fpgaadvantage>.
18. IEEE Standards Board, IEEE-754, IEEE Standard for Binary Floating-Point Arithmetic, New York: IEEE, 1985.
19. Lamiaa S.A.Hamid, Khaled A.Sheata, Hassan El-Ghitani, Mohamed Elsaid (2010),“ Design of Generic Floating Point Multiplier and Adder/Subtractor Units”, in proceedings of the 12th IEEE international Conference on computer modeling and Simulation.
20. Design of FPGA based Handwriting Image Recognition System ASME JOURNALS-AMSE IIETA publication-2017-series Lei Wang, Ziheng Yang, Guangqiang Xu, Meili Fu, Yu Wang
21. FPGA based Farsi Handwritten Digit Recognition System Marzieh Moradi , Mohammad Ali Pourmima , Farbod Razzazi.

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