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Constant on Time Controller for Voltage Regulator with and without Adaptive Voltage Positioning

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Abstract*: Advancement in electronics prompted for incremental usage of power supplies in digital circuits. In devices such as Central Processing Unit (CPU), Graphic Processing Unit (GPU) a Voltage regulator (VR) is utilized for microprocessors powering application. During load transients, microprocessor input voltage losses stability. High speed devices need quick response from the converters under transient conditions. Therefore, futuristic electronic devices demand a VR with new control schemes to operate at low operating voltage with improved efficiency thereby improving light load efficiency. In this paper a comparative study about the performance of Constant on Time (COT) controller with and without Adaptive Voltage Positioning (AVP) technique is presented. . The aim of the paper is to present the idea of AVP with COT during transients. Since load transient demands large number of capacitors to maintain stable voltage but increases the cost and volume. Thus, to overcome the transient time frame problem, voltage spikes and to reduce the number of capacitors. The converters need to operate under a new control scheme i.e. COT controller with AVP. Simulation of the voltage regulator is carried out for both Non AVP and AVP compliant schematics in LTSpice software. The simulation results show Non-AVP topology with output voltage spikes for 445uF but the AVP compliant topology with 222uF shows smooth output voltage transition.

Keywords: Adaptive voltage positioning; constant ON-Time control; dc-dc converters.

I. INTRODUCTION

This Almost all the electronic devices require DC power for their functioning e.g. computer, electronic gadgets like mobile phone, tablets, and camera. Thus, a DC power supply unit has to be installed between the power source and the end electronic circuits considered as loads [1]. Power processor module usually called a Voltage Regulator Module (VRM) acts as a buck converter and provides the microprocessor chip a flexible voltage. Normally VRM converts +12V to a lower voltage value required by the CPU and fulfils the processors demand of various voltage levels mounted on the same motherboard [2]. The recent CPU specifications from Intel and AMD demands 50 to 200A/µsec load-current slew rates with peak currents reaching 60Ato nearly 120A. These demands require changes in the existing design of portable power supplies.The quick progression of processor technology has presented severe difficulties for power management and delivery on the board.

One problem that needs to be addressed is the VR's dynamic voltage regulation. Large number of output capacitors have been utilized during the transient time frame to decrease the voltage spikes [3]. Expanding the quantity of capacitors to meet the higher transient is not a practical solution in light of size and cost issues. One approach to mitigate this issue depends on Adaptive Voltage positioning (AVP) control [4].

Light-load efficiency is a clear mandate for most applications. Since, most of the time devices operate under light-loading condition. To address the issues various controllers are implemented for non-isolated converters [5]. Compared to conventional control schemes Constant on-Time (COT) features improved light-load efficiency.

This paper first gives a brief introduction of the work in section I, looks at the previous development in Section II, and discusses the present state of the art in Section III. The design aspects for the work are discussed in Section IV along with the simulation work supporting the study and section V presents the conclusion.

II. HISTORICAL DEVELOPMENTS

In earlier days, Linear Power Supplies (LPS) are the main devices associated with power conversion [1]. The efficiency is poor as the regulating switch acts as variable resistor causing voltage drop which leads to the introduction Switch Mode Power Supply (SMPS). The development of controllers leads to the reduction in size of passive elements and improvement in the regulation of load in transient conditions [5]. In applications with multiple voltage requirements such as processor, it is important to design the converter with reduced size along with smooth regulation as it is the key to the performance of the processor [6]. The capacitors are employed to reduce the voltage ripples during load transients. The conventional methods used for load regulation during variation of load or supply conditions are discussed as follows and as shown in Fig.1.

- Voltage mode control,
- Current mode control and
- Sliding mode control.

In voltage mode control, the transient response is slow due to the delays present in error amplification stage which is essential to get minimum steady state error and to increase the transient response.

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Compared to voltage mode control, current mode control is faster in response to sudden changes in load or supply conditions. This is due to the dependence of inductor ripple current for pulse generation. In sliding mode control, transient response and steady state operation are improved but the variation of switching frequency leads to high speed switching and in turn increase switching losses with inductor core losses and EMI interference losses.

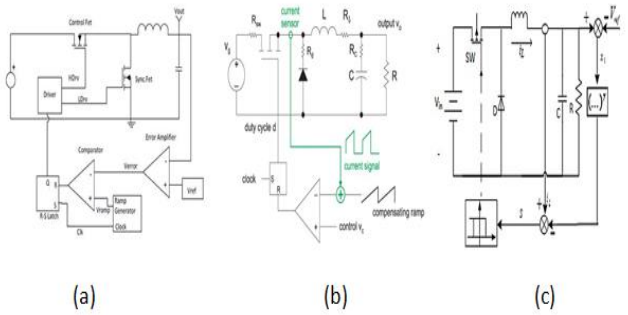

Fig.1. (a) Voltage mode control, (b) Current mode control and (c) sliding mode control of Buck Converter [5]

Therefore, a limit to change in frequency is introduced to make it quasi sliding mode control. Various techniques such as hysteresis, constant sampling frequency, constant ON time, etc., is introduced to limit the switching frequency [7].

With constant-on-time architecture, the control structure is very simple compared to traditional voltage/current mode control**.** Constant on-time control scheme that provides relatively better frequency but slight increase in complexity is adapted [8-9].

III. SYNCHRONOUS BUCK CONVERTER TOPOLOGY WITH COT CONTROL

A. Selected Topology

The synchronous buck voltage regulator is widely used in low voltage, high current applications. The proposed converter consists of two complementary switches with buck inductor and capacitor to reduce the voltage ripples. Synchronous buck converters are high in demand due to the efficient operation under dynamic conditions. The proposed voltage regulator module is provided in the Fig.2.

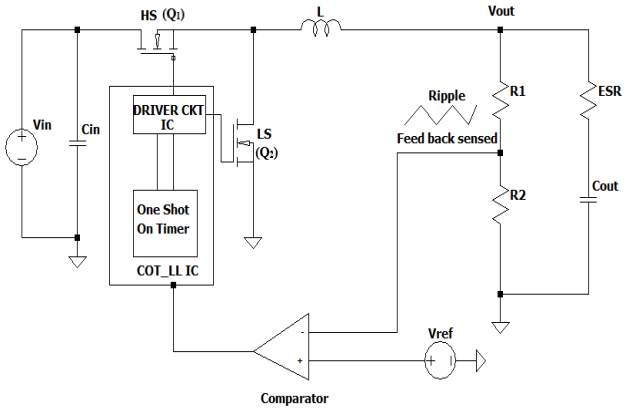

Fig.2. Synchronous buck voltage regulator with COT controller

The operational modes of the proposed voltage regulator shown in Fig.3 and Fig.4 are as follows:

Mode 1: In this, the high side (HS) switch Q_1 is ON and low side (LS) switch Q_2 is OFF. The inductor L gets charged along with the output capacitance C_{out}.

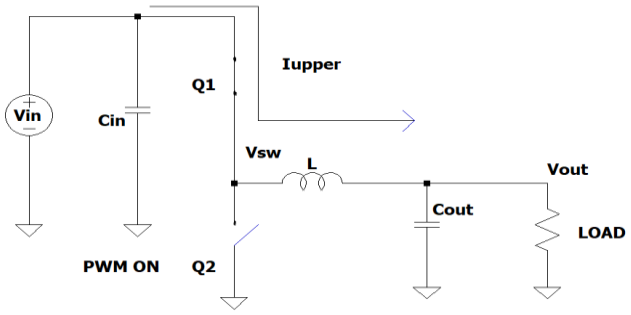

Fig.3. Mode1 operation of proposed voltage regulator

For the interval of DT, the switch Q_1 is ON and the voltage across the inductor is given as

$$V_{L_{ON}} = L\frac{di}{dt} \quad (1)$$

$$\Delta i_{ON} = \frac{V_{L_{ON}} * DT}{L} \quad (2)$$

Mode 2: In this, Q_1 is OFF and Q_2 is ON. The inductor L gets discharged along with the capacitance C_{out}.

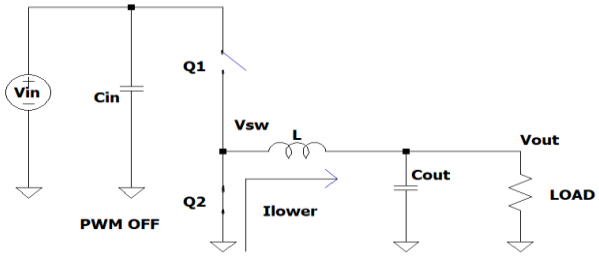

Fig.4. Mode1 operation of proposed voltage regulator

For the interval of 1-DT, the switch Q_2 is ON and the voltage across the inductor is given as

$$V_{L_{OFF}} = L\frac{di}{dt} \quad (3)$$

$$\Delta i_{OFF} = \frac{V_{L_{OFF}} * (1-D)T}{L} \quad (4)$$

For steady state operation the inductor voltage is calculated as

$$V_{L_{ON}} + V_{L_{OFF}} = 0 \quad (5)$$

From implementing equations 1 and 3 in equation 5, we get,

$$D = \frac{V_{out}}{V_{in}} \quad (6)$$

The output voltage ripple is compared with the reference voltage to generate fixed ON time pulse in order to turn ON the upper switch and when the pulse is OFF, the lower switch will be turned ON. The COT control provides pulses to both the switches. The ON time of pulse generated is constant throughout the operation and OFF time varies with the variation of load. During the load transient COT controller will adjust the OFF time and generates multiple pulses to improve the light load efficiency as shown in Fig.5.

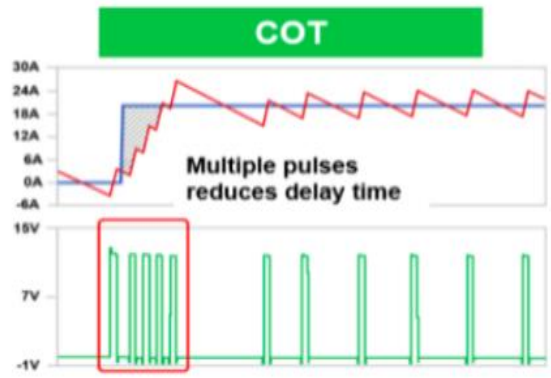

Fig.5. Pulse generation by COT control [4]

The COT architecture is free of compensation network as in voltage mode or current mode control. It makes the control design as simple and also increases the efficiency in light load conditions. The essential function of AVP is to control the voltage level so that it is near to minimum value at full load and at light load, the voltage will be near to maximum limit. The load voltage characteristics with and without AVP is shown in Fig.6.

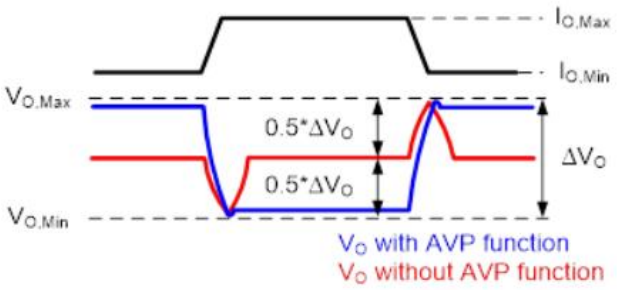

Fig.6. Voltage characteristics with and without AVP during load transients [8]

IV. DESIGN SPECIFICATION AND IMPLEMENATION

A. Parameter Calculation

The calculation of proposed topology starts with the following assumptions listed as below:

- The resistance (R_{ds}) offered by High side switch i.e. upper Mosfet=R_{dsup}=3 mΩ
- The resistance (R_{ds}) offered by Low side switch i.e. down Mosfet=R_{dsdw}=1 mΩ
- Mosfet max current =I_{mos}=60A
- Ripple current =ΔI_o =30% of load current =0.3*I_o
- Output ripple voltage =0.8% of output nominal voltage ΔV_o=(0.008*V_o)
- Input ripple voltage=1% of the input voltage ΔV_i =(0.01*V_i)

The proposed converter specifications are tabulated as follows in the Table.1:

Table.1 Converter Specifications

Input Voltage nominal (V_{in})	12 V
Output Voltage nominal (V_o)	0.75 V
Maximum load current ICCmax (I_o)	40 A
ITDP	32 A
Switching frequency (F_{sw})	600 Khz
Load line impedance (LL)	2.4 mΩ
Minimum output voltage (V_{min})	0.7 V
Maximum output voltage (V_{max})	0.88 V
Load Transient applied	40% to 100% I_o

The practical duty cycle calculation is given by equation (7)

$$D = \frac{V_o + V_{dsq2} + (dcr * I_o)}{V_i - V_{dsq1} + V_{dsq2}} \quad (7)$$

$$= 0.067684564$$

Where V_{dsq1}, V_{dsq2} are voltage drop in upper side switch and Lower side switch respectively and dcr is the DC resistance offered by inductor given in the manufacturer data sheet.

The practical inductor value with the voltage drops consideration is calculated by equation (8):

$$L = \frac{(V_i - V_{dsq1} - V_o) * D}{rippleI_o * F_{sw}} \quad (8)$$

$$= 104.6290548\text{nH}$$

Now the actual inductor ripple current considering the drops and inductor value is calculated back by the equation (9):

$$\Delta Ioc = \frac{(V_i - V_{dsq1} - (dcr * I_o) - V_o) * D}{L_S * F_{sw}} \quad (9)$$

$$= 12.5365349\text{A}$$

The practical output capacitance is calculated by the equation (10):

$$C_o = \frac{\Delta Ioc}{8 * F_{sw} * RippleV_o} \quad (10)$$

$$= 435.2963507\text{uF}$$

Now the actual capacitor ripple voltage with the esr drop is calculated back from the equation (11):

$$\Delta Voc = \frac{rippleI_{oc}}{8 * F_{sw} * C_{so}} + (rippleI_{oc} * E_q C_o E_{sr}) \quad (11)$$

$$=8.99627222\text{mV}$$

B. Simulation Using LTSpice

(i) Non-AVP Topology

The simulation circuit of the voltage regulator without AVP compliant is shown in Fig.7. In the snap, L1 indicates output inductor. The use of multiple capacitors in parallel at the output side leads to the reduction in equivalent series resistance (ESR) and is indicated by C_1, C_2 and so on with R_2, R_4 representing ESR's. The output voltages i.e. overshoot and undershoot voltage waveform of Non-AVP topology is as shown in the Fig.8. The Non AVP topology provides the output voltage with undershoot and overshoot values 726mV and 853mV respectively for given input of 12V.

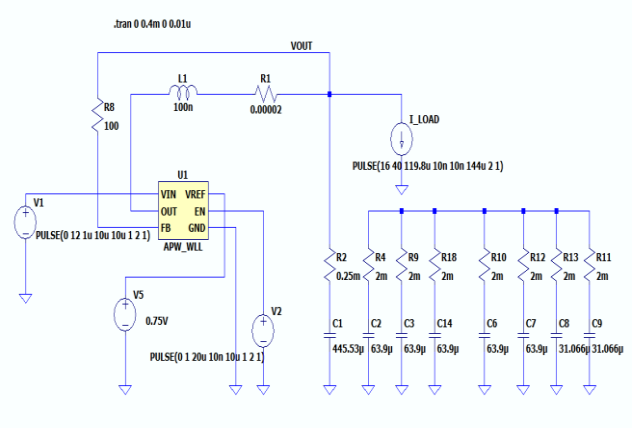

Fig.7. Simulation circuit of proposed converter without AVP

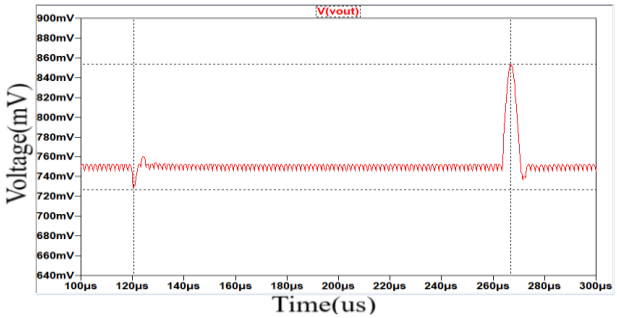

Fig.8 Output Voltage of proposed converter without AVP

The output voltage with a ripple 6.8mV is obtained for the input 12V is shown in Fig.9:

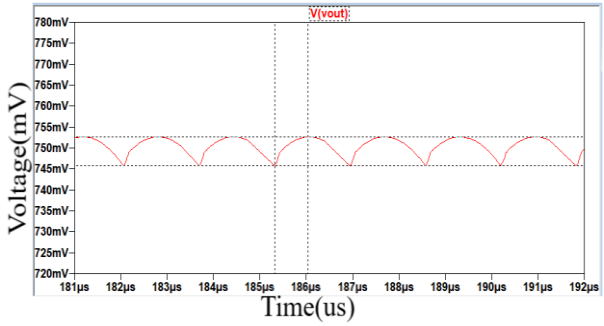

Fig.9. Output ripple voltage of proposed converter without AVP

The Inductor ripple current same as the output ripple current is shown in the Fig.10:

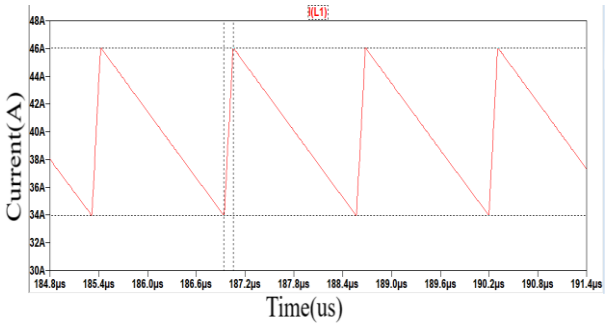

Fig.10. Inductor ripple current of proposed converter without AVP

For the given specification peak ripple current value corresponds to 12.05A.

The duty ratio i.e. on time of the controller for the given inputs corresponds to 112ns that is around 6.7% and the waveform is shown in Fig.11:

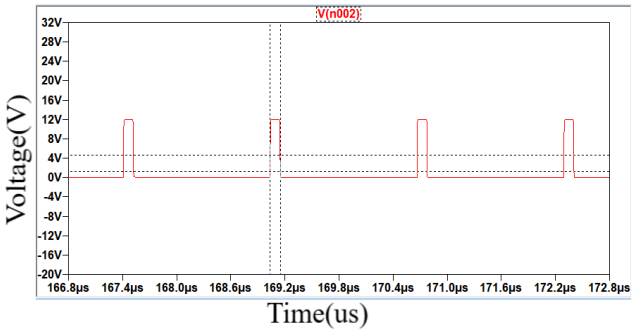

Fig.11. Duty ratio waveform of Non-AVP topology

(ii) AVP topology

The simulation circuit of AVP compliant voltage regulator with reduced number of capacitors as shown in Fig.12:

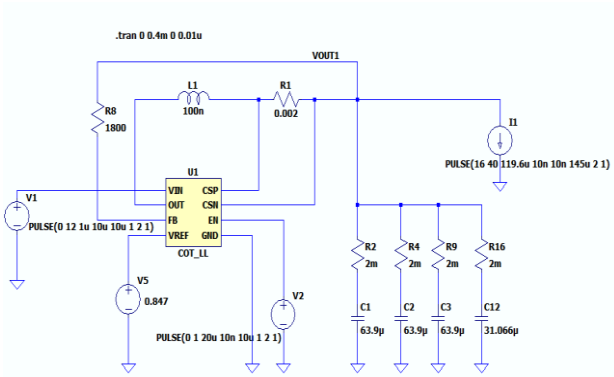

Fig.12 Simulation circuit of proposed converter with AVP and reduced capacitors

COT_LL indicates the constant on time controller IC package with internal MOSFET's and driver circuitry. The reference voltage provided is 847mV and R_8 value is 1800ohms.

The output voltages i.e. minimum and maximum voltage snap of AVP topology is shown in Fig.13:

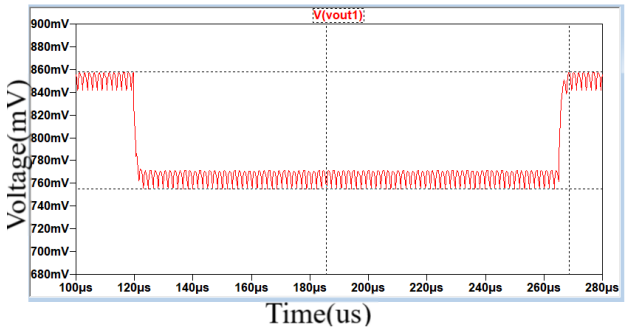

Fig.13 Output Voltage of proposed converter with AVP

The snap shows load line implementation and the prevention of sudden spikes which leads smooth transition. The AVP compliant output voltage for the input 12V corresponds to 755mV and 850mV. The use of COT controller leads to the reduction in capacitors (i.e. half compared to Non-AVP) for achieving the specified requirements.

AVP compliant voltage regulator with reduced number of capacitors and fine tuning is simulated and shown in Fig.14:

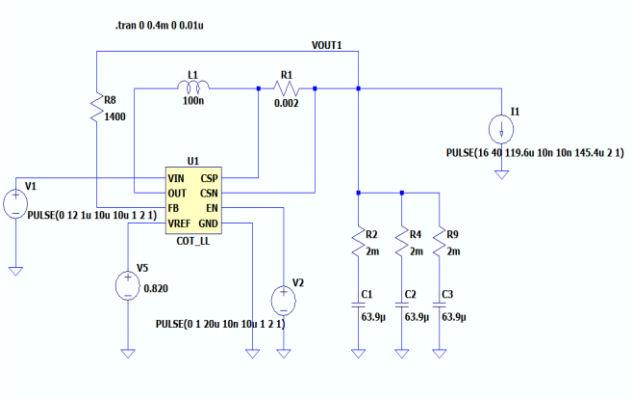

Fig.14 Simulation Circuit of AVP compliant voltage regulator with Fine Tuning

To reduce the voltage window and achieve Minimum and Maximum values accurately load line adjustment with fine tuning is done. The reference voltage and R_8 resistor are adjusted resulting 726mV as minimum voltage and 837mV as maximum voltage.

The tuning in the circuit sets the undershoot voltage to minimal value and causes the overall reduction of voltage window usage as shown in Fig.15. Load line is set such that it prevents the sharp spikes to occur and protects the circuit from transients. Also the light load efficiency is increased with the proposed controller.

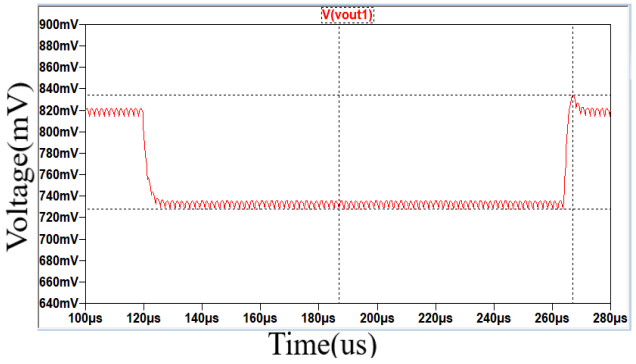

Fig.15 Minimum and Maximum voltage waveform of AVP topology with reduced capacitance fine tuning

Due to the reduction in capacitance value there is a tradeoff between ripple voltage i.e. the ripple voltage tends to increase. For input of 12V the output voltage with a ripple of 16mV is obtained and shown in Fig.16:

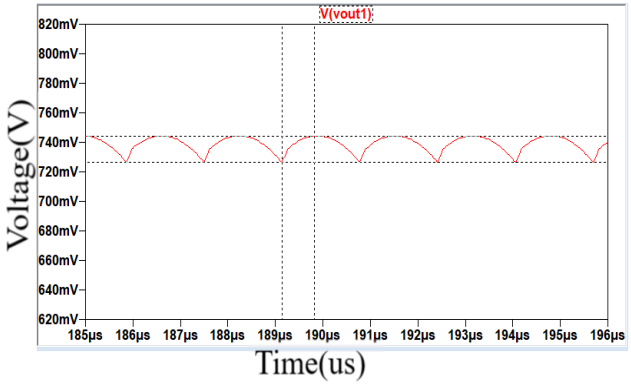

Fig.16 Output Ripple Voltage waveform of AVP topology

The change in inductor current ripple for AVP topology is more or less the same as Non-AVP and is shown in Fig.17:

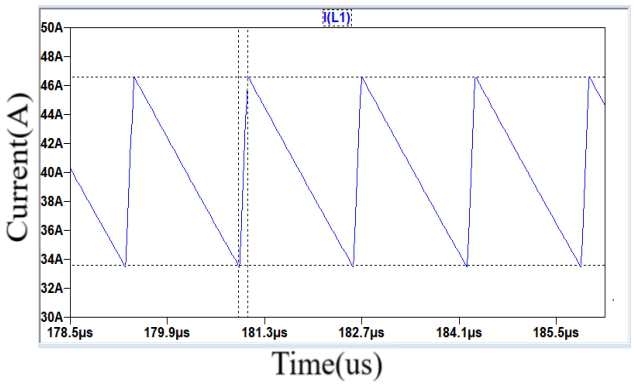

Fig.17 Inductor Ripple current waveform of AVP topology

For the given specification peak ripple current value corresponds to 13A.In AVP topology the duty ratio i.e. on time of the controller for the given inputs corresponds to 118ns that is around 6.8% and is shown in Fig.18:

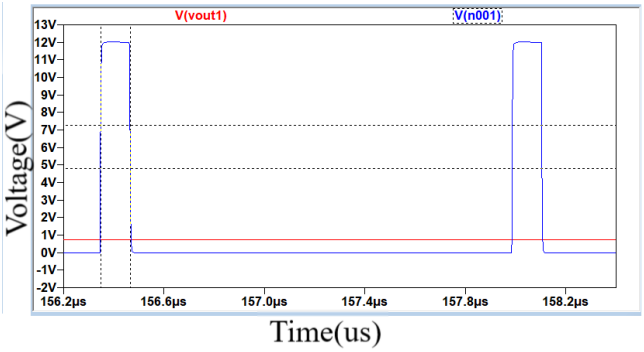

Fig.18 Duty ratio waveform of AVP topology

The application of sudden transient and corresponding inductor ripple current waveform is shown in Fig.19:

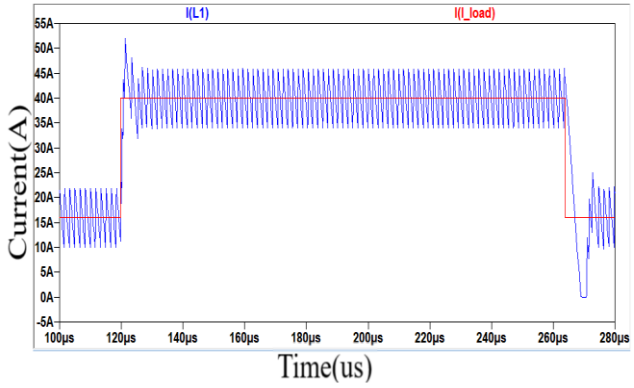

Fig.19 Load current and inductor ripple current waveforms in transient conditions

According to the specifications the load is applied from 16A to 40A and the changes in inductor current is observed as shown in Fig.20.

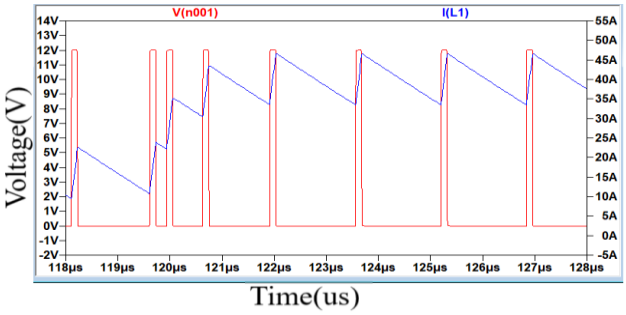

Fig.20 Pulses generated during load transients in AVP topology

During the transient period or light load period the COT controller changes the off time and maintains the same on time. Thus, during the transient period or light load condition the controller adopts nearly constant frequency mode. From the simulation results the comparison of Non-AVP and AVP considering the output voltages, ripple voltage and current values with capacitance required is tabulated in the Table.2:

Table.2-Comparison results of Non-AVP and AVP

Parameters	Calculated values	Non-AVP	AVP
Undershoot Voltage	725mV	726mV	726mV
Overshoot Voltage	847mV	853mV	837mV
Output Ripple Voltage	8.99mV	8.6mV	16mV
Inductor Ripple current	12.5A	12.05A	13A
Capacitance required	445.53uF	445.53uF	222uF
Duty ratio	6.7%	6.6%	6.8%

C. Hardware Verification

The implementation of discussed topologies are first reviewed with the schematic layout then the actual testing begins. The verification of voltage regulator with and without AVP compliant behavior is done in Intel IOTG labs, Bengaluru. The waveforms of output voltages are captured using DSO and shown in Fig.21 and Fig 22 respectively.

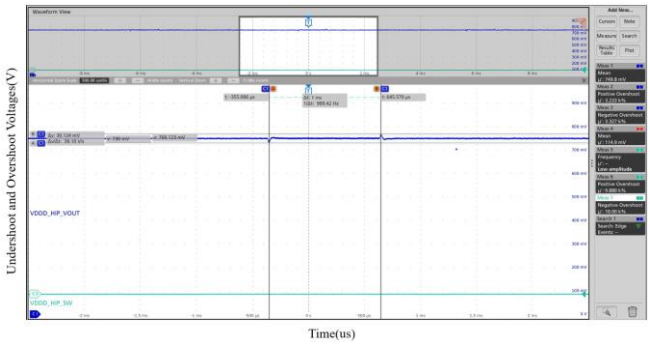

Fig.21 Output voltage validation waveforms of Non-AVP topology

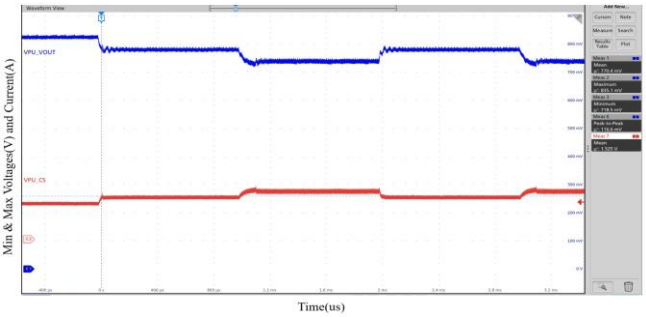

Fig.21 Output voltage validation waveforms of AVP topology

IV. CONCLUSION

In this paper, the principle of synchronous buck topology and adaptive voltage positioning is adopted. Advanced COT controller with internal built MOSFET and driver circuit IC is implemented for providing switching pulses of Voltage regulator. The Voltage regulator module is implemented with both Non-AVP and AVP compliant using LTSpice simulation software. Conventional topology generating voltages spikes is simulated with APW_WLL controller and the reduction in spikes with minimum and maximum voltage levels with improved light load efficiency is simulated using COT_LL controller. In Non-AVP topology with input 12V and 445uF capacitance the output i.e.726mV undershoot and overshoot being at 853mV is observed. In AVP compliant topology with input 12V and 222uF capacitance the output i.e. minimum and maximum voltage levels are 726mV and 837mV respectively. Thus the reduction of capacitance and improved light load efficiency is achieved with AVP topology.

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REFERENCES

1. Van Wyk J. D and Lee F.C, “On a Future for Power Electronics”, *IEEE Journal Of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 2, pp. 59-72, June2013.
2. Intel document "Voltage Regulator-Down (VRD)"http://www.intel.com/assets/pdf/designguide/313214.pdf dated November 2006.
3. P. K. Sim and Z. Salam, "Some issues on the design of a voltage regulator module (VRM) for microprocessor power supply," *Proceedings. National Power Engineering Conference, 2003. PECon 2003.*, Bangi, Malaysia, 2003, pp. 110-116.
4. K. Yao *et al.*, "Adaptive voltage position design for voltage regulators", *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC '04.*, Anaheim, CA, USA, 2004.
5. Himanshu and R. Khanna, "Various control methods for DC-DC buck converter", *2012 IEEE Fifth Power India Conference*, Murthal, 2012, pp. 1-4
6. R. Panguloori, D. Kastha, A. Patra and G. Capodivacca, "High performance voltage regulator for high step-down DC-DC conversion", *2008 34th Annual Conference of IEEE Industrial Electronics*, Orlando, FL, 2008.
7. J. Sun, M. Xu, Y. Ren and F. C. Lee, "Light-Load Efficiency Improvement for Buck Voltage Regulators", in *IEEE Transactions on Power Electronics*, vol. 24, no. 3, pp. 742-751, March 2009.

8. K. Hu, B. Chen and C. Tsai, "A digitally controlled buck converter with current sensor-less adaptive voltage positioning (AVP) mechanism", *2017 International Symposium on VLSI Design, Automation and Test (VLSI-DAT)*, Hsinchu, 2017.
9. C. Chen, S. Lu, S. Hsiao, Y. Chen and J. Huang, "A Current-Mode Buck Converter With Reconfigurable On-Chip Compensation and Adaptive Voltage Positioning", in *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 485-494, Jan. 2019.

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