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CMOS-NAND Based Gate Driver Card of IGBT for Fault Diagnosis in VSI

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Abstract*: In industrial application, over loading condition, short circuit is the dominant fault in the motor drives. There are many reasons for the fault but due to this insulated gate bipolar transistor (IGBT) gets damaged which affect the whole system. Protecting IGBT and hence protecting motor drive system at fault condition is the crucial and insistent part of the protection. The short circuit and open circuit fault in an IGBT can be detected by several techniques. The paper presents an idea to deals with the short circuit fault such as fault under over load condition in the typical applications like winder machine. In this paper both the fault diagnosis and clearance of the fault are done. Fault diagnosis is based on the voltage between the collector and the emitter (VCE) of the IGBT which can be done by actual short circuit between these points in the simulation. Voltages of healthy and faulty condition are analyzed. In the fault clearance, CMOS-NAND based circuitry is used called EH10 card for inverter. It shows that this card has ability to detect the fault across the switch and give the signal to microcontroller for its clearance by making GATE signal of the IGBTs zero. This protection of Inverter using realization of CMOS-NAND based GATE driver card is verified using MATLAB simulation results.

Keywords: Voltage Source Inverter, Short Circuit Fault, IGBT fault Diagnosis, EH10 card.

I. INTRODUCTION

As the technology grows there is a notable advancement in the world of power semiconductor switches. The IGBT (Insulated Gate Bipolar Transistor) has several advantages over other semiconductor switches. It is commonly used in high power application in the industrial drives. There are many conditions when short circuit fault is occurred in the industrial motor drive. However, one of the main causes of the damage is the IGBT switch in the inverter circuitry. Hence, the fault occurred in the IGBT can be in two cases: Hard Switching Fault (HSF) and Fault under Load (FUL). In HSF, the short condition occurred when the device is shorted with the DC limb, whereas in FUL, the device is shorted in on - condition. The behavior of the FUL fault is more severe than the HSF [7]. For example, in a single leg of a three phase inverter, when FUL short circuit condition is incident on the upper side then the lower IGBT will be defined as having HSF condition.[6].The gate driver circuits are designed to protect the IGBTs. This gate driver circuit gives power amplification at the time of switching the devices. The driver circuits are also designed to generate the turn-off signals for the controller which intended to stop the healthy PWM pulses, once the fault has occurred. This paper presents the realization of such gate driver card (EH10) which operates in a same fashion. The decision of the fault condition is taken on the basis of the voltage across the collector and the emitter of the individual IGBT within the inverter circuitry. However, the decision to continue the Load or not can be taken on the basis of the change in voltage due to short circuit in each switch of the inverter [9]. The basic scheme of the overall gate driver circuit is based on receiving the SPWM pulses from the main controller of the motor driver unit. The electrical isolation is provided to the gate driver circuit using opto-couplers. Further, the SPWM pulses are given to the gate of IGBT through the EH10 card. If short circuit fault is occurred then the circuit designed to detect the fault in the inverter. The fault signal is feedback to the Micro-controller to interrupt the healthy SPWM pulses. This sensed fault signal is again isolated by another opto-coupler and hence, the gate pulses are stopped for all the switches of the inverter. Thus, the outputs of the inverter become zero and fault condition is resolved.

II. METHODOLOGY

The presented algorithm is based on the circuit having two CMOS-NAND ICs to process the pulses coming from the first opto-coupler. The card itself has ability to detect the fault within the inverter circuit by analyzing the voltage across each switch. If the fault occurs at any switch at any instance, the detection circuit senses the fault and gives feedback to the controller to stop the healthy pulses through second opto-coupler. The controller then blocks the healthy pulses for all switches. The fault detection logic is the decision-making logic whether SPWM pulses have to be continued or not. On the basis of the schematic diagram as shown in fig.1, starting from the controller, the pulses of 1 V is given at the cathode pin of first opto-coupler. Further, the pulses are process through the CMOS NAND ICs. The NAND ICs are used to generate the pulses for two different purposes i.e. to drive the MOSFET driver circuit and to keep the fault detection circuit continuously on till the motor drive system is in operation.

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The MOSFET driver circuit is used to give the higher switching frequency and power amplification for the gate switching. At the terminal of the gate pulses, basic protection is given to deal with heavy current spikes with help of resistors. Now, if the short circuit fault occurs on any of the IGBT of the inverter, the voltage across the switch is sensed. Depending on the voltage VCE, fault signal is generated and given to the opto-coupler-2. This signal is transferred to the controller as a fault signal by the opto-coupler-2 and the pulses for all the switches are stopped. The CMOS NAND ICs are used to operate on higher voltage range so this circuit is used for higher voltage range.

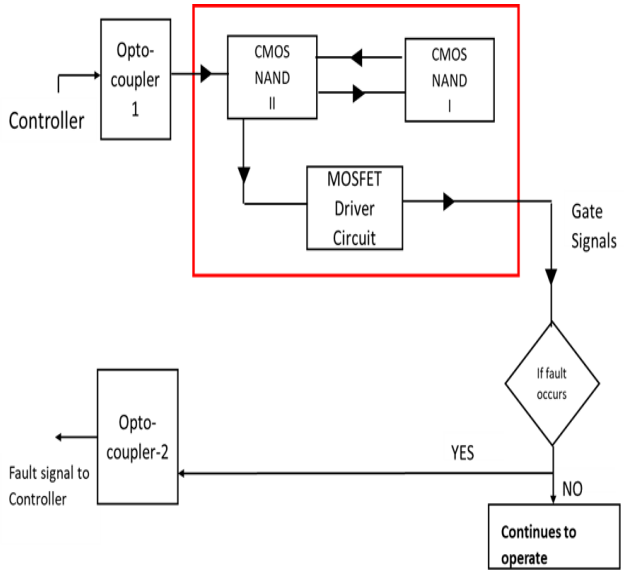

Fig. 1. Schematic diagram of the gate driver circuit

To realise the defined algorithm, it can be implemented in the inverter circuit. Referring to the fig. 2, gate pulses are given to the IGBT through switch s1 from the driver circuit. To create the fault switch s2 is closed. The voltage across collector and emitter of the IGBT is sense by the fault detector circuit. The fault detector circuit has NPN transistor and RC circuit to judge the fault situation. In driver circuit,NAND ICs are implemented in such a way that it give always high pulse to the base of the transistor and the voltage across the switch is applied to the collector the transistor while emitter of the transistor is grounded. Thus, the voltage across the transistor is given to the RC circuit to filter out the pulsed voltage across the switch. The capacitor voltage is kept on charging and discharging till the switch is healthy.If s2 then the switch get short and voltage across the switch is zero. This led to discharge the capacitor to zero volts. Here the fact comes into the picture that, every switch has its ON state transition voltage which keeps it on: if the capacitor voltage falls below that on state voltage then the octo-coupler gives the high signal at fault pin of the Micro-controller.

The fault detection circuit involves the RC circuit, hence for fault detection requires some time.The time constant for the RC circuit for higher voltages will be more as it depends on the supply voltage of the Inverter. Here the inverter is supplied by the 100 V supply and the load is considered as the RL load, where R= 10Ω and L=23 mH. The on- state transition voltage for the IGBT is considered as 4 V, that means whenever the fault is there, the voltage across the IGBT becomes zero and the voltage across capacitor falls below 4 V, as soon as the voltage falls below the 4 V comparator gives high pulse to the octo-coupler-2. And the controller receives fault signal. As the current capacity of the IGBT increases, the on- state transition voltage for the IGBT will also increase. Hence, this logic for the fault detection can be applied for different value of on-state transition voltage provided that the RC time constant has to be designed for that value to detect the fault. And stop the system as early as possible. The RC circuit will increase components of circuitry and cost too.

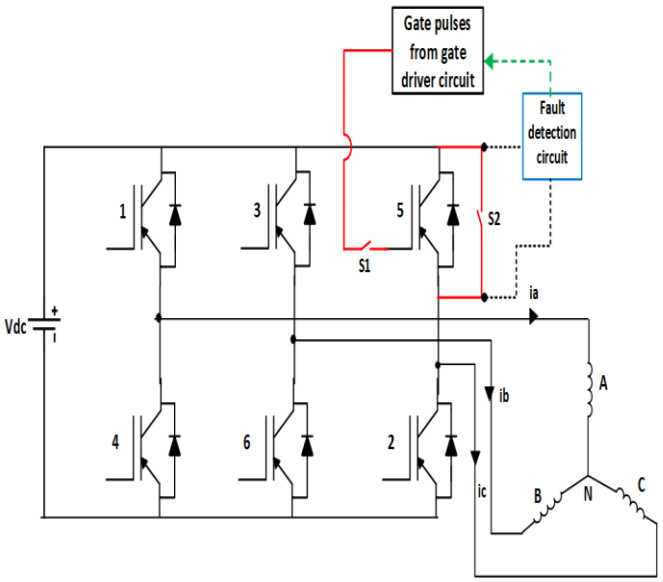

Fig. 2. Schematic diagram of the implemented circuit in thr inverter system.

Usually, in healthy condition, the gate pulses for the switches are derived by the comparing the sine wave and the triangular carrier wave. But during fault condition, the gate pulses for the IGBTs should be stopped i.e if s2 is closed then s1 should be open (refer Fig.2). This scheme is applied to all switches of the inverter so that the output of the inverter becomes zero. To do so, one method can be implemented that making no comparison of sine wave and the triangular carrier wave.

III. SIMULATION RESULTS

Now, by creating the fault on the switch 5 of the inverter following results are obtained. The Fig. 3 (a) shows the result of input voltage of the inverter Vdc, and output of inverter such as phase voltage Van, line voltage Vab, and phase currents of the inverter. Fig.3 (b) gate pulses of switch 5, voltage across the switch 5, fault status of switch 5. And Fig.3(c) shows the Voltage across the capacitor of fault detector circuit. Fig.3 shows the results before and after the fault situation. The fault occurred on switch 5 at the instance of 0.06 sec, it can be observed from the Fig. 3 (b) the gate pulses of the switch 5 becomes zero after 14 msec after the fault occurrence. Therefore, we can conclude that the fault condition can be detected by the controller after 14 msec of the occurrence. This fault detection time depends upon the capacitor value and the time constant of the RC circuit used for the filtration of the pulsating voltage across the switch as shown in Fig 3(c).

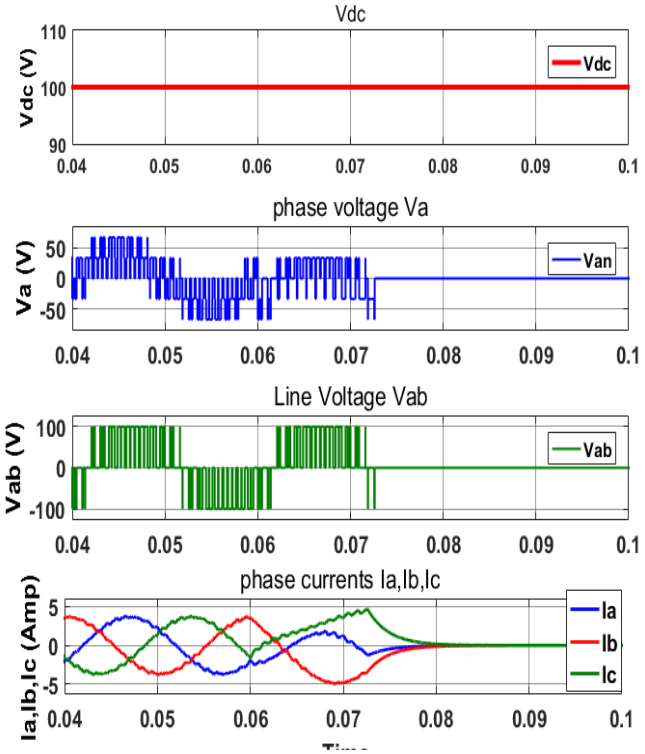

Fig. 3(a). Inverter output (Phase voltage Va, Line voltage Vab, current of three phases Ia,Ib,Ic)

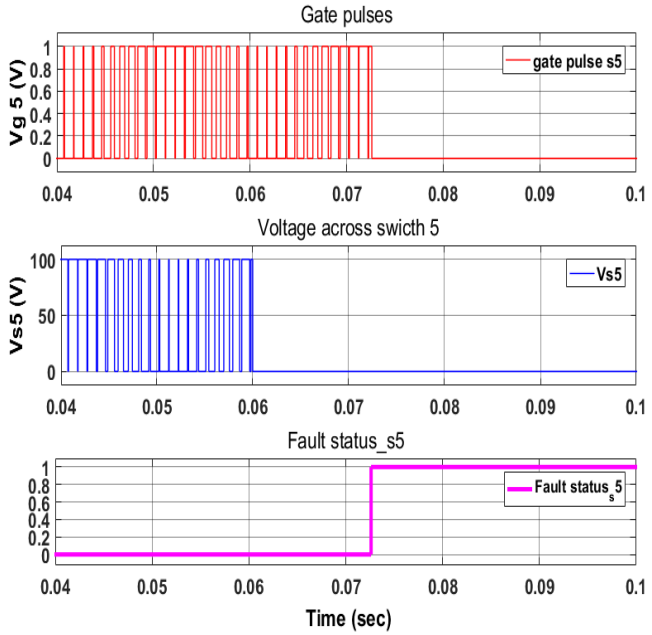

Fig. 3(b). Gate pulses, voltage across switch, fault status of switch 5

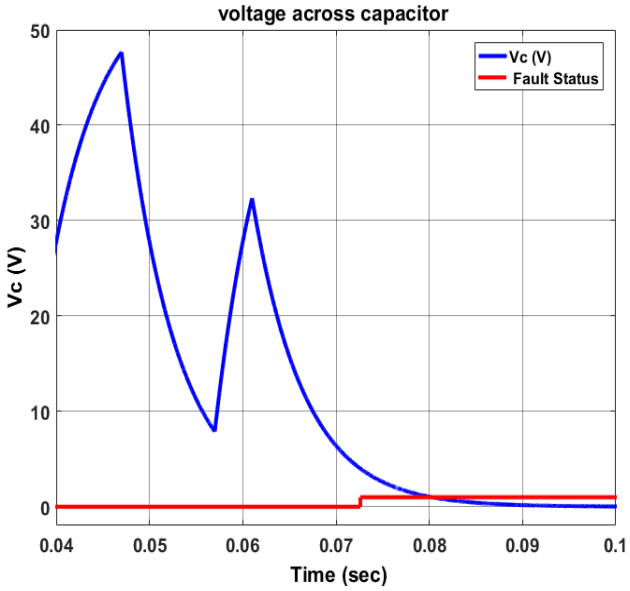

Fig. 3(c). Voltage across Capacitor of fault detection circuit and fault status

The modulation for the upper switch and the lower switch is designed in such a way that if fault occurs on any of the switch then carrier wave for the upper switch will become constant at greater value than the amplitude of the sine wave here it is taken as 2. Hence, there is no comparison and resulting pulses becomes zero as shown in Fig 4(a). Similarly, the carrier wave for the lower switch will become constant at lower value say -1 than the negative amplitude of the sine wave. And there is no comparison between sine wave and triangular carrier wave.

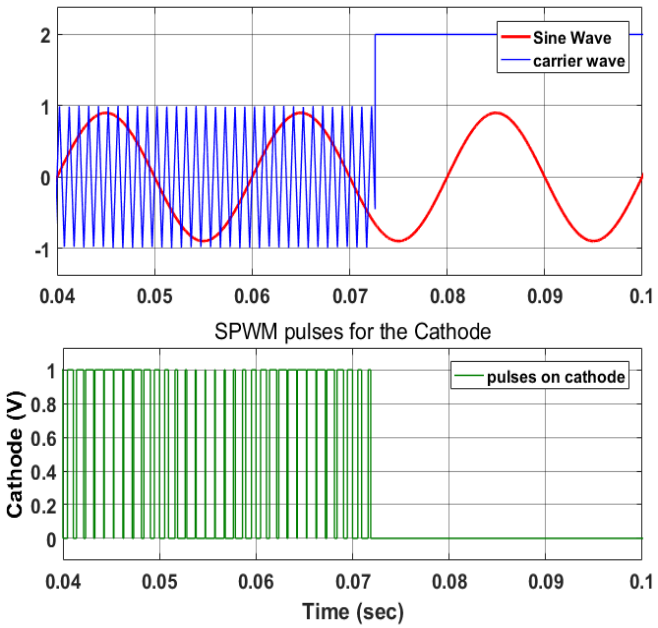

Fig. 4(a). SPWM pulses for the upper switches of the inverter

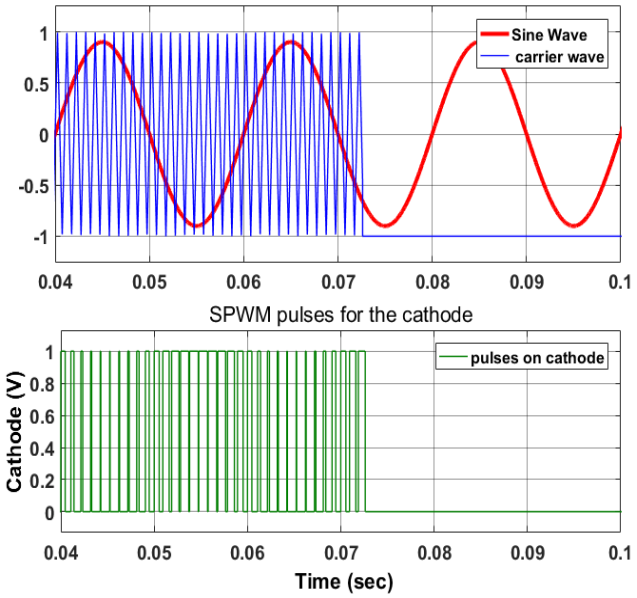

Fig. 4(b). SPWM pulses for the lower switches of the inverter

IV. CONCLUSION

Simulation result shows that CMOS-NAND Based EH10 card is very effectively diagnosed the fault and gives the signal to Microcontroller. As the Microcontroller sense the fault, it stops the pulses to the IGBT. Hence, the VSI isolates the load from the supply. With this further damage to the other system can be secure. With the removal of VSI, damaged IGBT can be replaced & hence the whole system can be restored for the further task.

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