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DVR Control System for Voltage Sag/Swell Compensation for Sensitive Loads Protection

Zeinab Elkady, Naser Abdel-Rahim, Ahmed A. Mansour, Fahmy M. Bendary

Abstract*: This paper introduces an enhanced control system to improve the transient response of the dynamic voltage restorer (DVR). The control strategy achieves superior response against voltage disturbance approximately within 400 µs. The control system comprises three terms: closed-loop feedback control signal, upstream disturbance detection error, and voltage drop over DVR term. The actual load voltage is compared with its reference value and is adapted by a PI controller. The upstream disturbance detection significantly enhances the transient time of the control system performance and improves its steady-state operation. In addition, the voltage drop over the DVR term represents the voltage drop caused by the DVR circuit component. Incorporating these effects in the control loop, fast and accurate response of the system are achieved. An L filter is used instead of the LC filter to overcome the inherent LC filter damping delay and resonance problem mentioned in previous studies. The system is simulated using MATLAB/ Simulink. The simulation results show excellent response in transient and steady-state operation for various operating conditions.

Keywords: Dynamic voltage restorer, power quality, voltage sag, voltage swell, voltage source inverter

I. INTRODUCTION

Recently, power quality (PQ) attracted much attention especially by industrial and commercial consumers due to the huge economic losses caused by poor PQ. In addition, there is a steady increase in using sensitive electronic equipment in the industrial, residential, and commercial sectors. Voltage disturbances such as voltage sag (dip), voltage swell, flickers, interruptions, and voltage harmonics, are among the most significant PQ problems 1. According to some statistical studies, voltage sag has been identified as the most frequent and repeated voltage disturbance which has a negative impact on production costs 2, 3. Investigation of equipment sensitivity and malfunction due to voltage dip has been reported in the literature [9].

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***** Correspondence Author
Zeinab Elkady*, Department of Power Electronics and Energy Conversion, Electronics Research Institute, Cairo, Egypt. E-mail: zaianb.elkady@eri.sci.eg
Naser M. B. Abdel-Rahim, Department of Electrical Engineering, Future University, Egypt, Cairo, Egypt. E-mail: naser.abdelrahim@fue.edu.eg
Ahmed Aly Mansour, power electronics and energy conversion department, Electronics Research Institute, Cairo, Egypt. E-mail: mansour@eri.sci.eg
Fahmy Bendary, Electrical Power System, Benha University Faculty of Engineering, Shoubra. E-mail: fbendary45@gmail.com

Various examples of problems associated with different voltage sags have been discussed in 7-[9].
The causes of voltage sag/swell may be due to the starting of large motors or transformers energizing, switching operations, faults (short circuit), and sudden load changes 3, 4. Such causes are impossible to prevent but can be dealt with in a way to mitigate their negative impact on equipment. According to the IEEE standards 1346 and IEEE 519-2014 5, 6, a voltage sag/swell is defined as a decrease/increase in the RMS ac voltage (10–90% of the nominal voltage /110–190% of the nominal voltage), respectively, at the power frequency of duration from 10.0 milliseconds to 1.0 minute. From the definition, one of the most necessary requirements in the voltage sag/swell compensation device is to detect and compensate the sag/swell within a time of fewer than 10 milliseconds. Hence, the transient response and good overall performance of the DVR system are essential for providing a good quality of the power system. In order to mitigate the problems associated with voltage sag, various studies reported in the literature have dealt with the DVR control system to improve its transient and steady-state response 10 , 11. Open-loop control is the most reported control strategy because of the fast voltage compensation requirement, but it has poor performance such as steady-state error and delay time in its response 1213. Single-feedback closed-loop 14 and multi-loop control 15 methods are applied on DVR in a different study aimed to improve the control system response. Ref. 16 analyzes the physical limitations of DVR systems bandwidth control by using LC output filters that lead to time delays and compensation voltage resonance issues. A combination of feedforward and state feedback control system has been created for DVR compensation voltages. In 17, a closed-loop state variable control strategy removing the inner current control loop in a multi-control structure has been presented. The derivative of the output current is used to increase the dynamic response of the control system. This study compares its proposed technique with open feed-forward and multi-loop structure and achieved a better response in both transient and steady-state conditions. However, in this method, the load side is compensated to the nominal amplitude within 4 milliseconds. In 18, the transient behavior of DVR from a perspective including the LC resonance source and resonance factors has been investigated. An effective damping method was subsequently proposed using a multi-loop controller with the Posicast 16 and P+Resonant controllers. The results indicated that the DVR has succeeded in restoring the load voltage in half a cycle.

In 19, a repetitive control scheme for a three-phase series compensator was introduced. The controller response delayed one PWM switching cycle. A repetitive controller with one feed-forward and two feedback loops has been proposed in 20. The first feedback loop is used to increase system damping while the feed-forward loop compensates for the voltage drops.

The second feedback loop applies the repeated time controller to compensate for periodic distortions of voltage. The simulation results show good dynamic performance. In 21, hybrid energy storage (HES) with superconducting magnetic energy storage (SMES), high temperature superconducting (HTS) magnets can store a mass of magnetic energy. The integration of the SMES quick response feature in HES-based DVR has been introduced.

This paper proposes an enhanced control structure of the DVR system. The proposed control structure employs two feed-forward control loops and one feedback control loop. The first feedforward control term incorporates the difference between the actual voltage at the PCC and its reference waveform. This has the effect of continuously calculating the upstream voltage disturbance. The second feed-forward control term combines the voltage drop across the DVR itself. Finally, the feed-back control loop incorporates the difference between the actual load voltage and its reference waveform. The proposed control scheme has a very fast dynamic response and excellent steady-state performance. The system is simulated using MATLAB/Simulink and the simulation results show an excellent response in transient and steady-state operation for different conditions.

II. SYSTEM MODELLING

Figure 1 shows the power circuit of the DVR as a series compensation device in the distribution line. Neglecting higher-order harmonics, the voltage source inverter (VSI) can be represented by an ideal AC (Vinv, a, Vinv, b, and Vinv, c) as depicted in Figure 2.

In this paper, a first-order low pass "L" filter is used to interface between the inverter and the power grid. This has the effect of reducing harmonic injection into the power grid. An "L" filter is used rather than an LC filter to avoid the transients of the LC filter oscillations initiated at the start and at the recovery instant from a voltage sag 18. Also, resonance problems and time delay caused by LC filter with DVR are avoided 16, 22. As shown in Figure 1, a series injection transformer is used to provide the required amount of power compensation. The injection transformer is a three-phase transformer designed as three single-phase transformers connecting each phase to the three legs of the inverter. The injection transformer in the DVR systems guarantees galvanic isolation and filtration for the pulsated inverter output voltage. Careful design of the injection transformer is a very essential element in DVR as it may face saturation, overrating, and/or overheating 23. In this study, it is assumed that the load is R-L with rated power 15.0 kVA and the DVR is designed to compensate the voltage dip/swell within ± 30% of the total kVA, i.e. DVR is designed to compensate within ±5.0 kVA. Considering that the primary side of the transformer is the inverter side, the transformer is a step-down transformer with a turns ratio of 3:1 in order to decrease the current stress on the inverter switching devices. Table I illustrates the system parameters per phase.

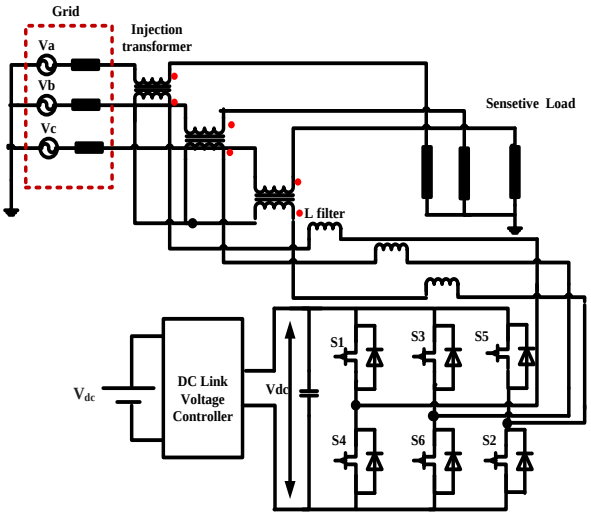

Figure 1. The power circuit of the DVR

Table I: System parameters per phase

Fs (switching frequency	5.0 kHz
R (load)	10.0 Ω
L (load)	10.0 mH
Load power rating	4620.0 VA
Transformer rated power	3.0 kVA
Inverter rated power	2.5 kVA
L(filter)	100.0 mH
Transformer turns ratio	3:1
Vprimary(inverter side)	350 V
Vsecondary(grid side)	117 V
Vdc	750.0 V
V_PCC (RMS phase value)	220.0 V

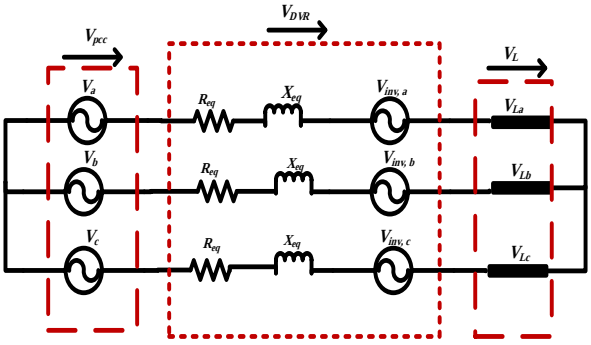

Figure 2. Simplified circuit model for the proposed system

The equivalent circuit of the system model is shown in Figure 2. Applying KVL yields

$$\vec{V}_{L(a,b,c)} = \vec{V}_{PCC(a,b,c)} - \vec{V}_{DVR(a,b,c)} \quad (1),$$

$$\vec{V}_{DVR} = \vec{V}_{inv(a,b,c)} + \vec{I}_{a,b,c}(R_{eq} + jX_{eq}) = \vec{V}_{PCC(a,b,c)} - \vec{V}_{L(a,b,c)} \quad (2).$$

Where,

$V_{PCC(a,b,c)}$ are the voltages of phases "a", "b", and "c" at the PCC, respectively,

$I_{a,b,c}(R_{eq}+jX_{eq})$ are the voltage drops over the DVR internal impedance (including the filter series inductance) for phases "a", "b", and "c", respectively.

$V_{inv(a,b,c)}$ are the controlled output voltage for phases "a", "b", and "c" of the VSI, respectively.

Equation (1) shows that the load voltage is dependent on the value of the voltage at the PCC (Vpcc) and the controlled DVR voltage. Equation (2) indicates that the compensation process should include the compensation of the voltage drop over DVR internal impedance.

III. CONTROL SYSTEM STRUCTURE

Figure 3 shows the block diagram of the enhanced control structure. Referring to (2), it can be seen that for good and fast dynamic responses, the voltage drops across the DVR, as well as the disturbances in the voltage at PCC, must be incorporated in the control loop. The principle of operation of the control system is as follows. The upstream voltage is compared with its disturbance-free value (V^*_{PCC}) to produce e_{PCC}. At the same time, the load voltage (V_L) is compared with its reference value (V^*_L) to produce *e*. *e* is conditioned using the PI controller to produce e_{pi}. e_{pi} is summed up with e_{PCC} and the voltage drop across the DVR to produce the e_c. e_c is then employed to produce the proper space vector PWM signal. This PWM signal is used to control the switching devices of the voltage-source inverter (VSI) which is then transformed using the series injection transformer to the power grid voltage level to produce the compensating voltage (v_{cmp}). v_{cmp} is summed up with V_{PCC} to produce the regulated load voltage.

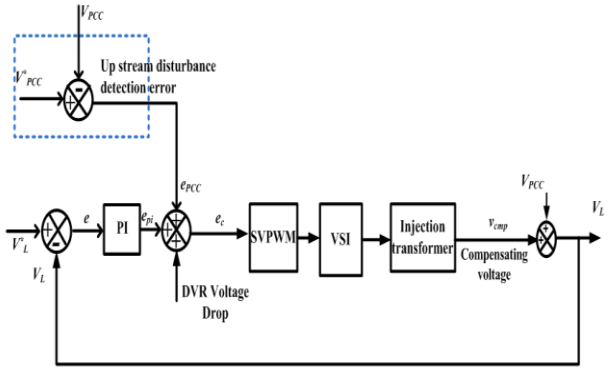

Figure 3. Block diagram of the proposed control algorithm

Figure **4** shows the detailed control circuit of the DVR system which is required to perform the following tasks:

1. Detect the grid angle (for grid synchronization)
2. Detect the load and/or grid voltage
3. Calculate the reference voltage and the compensating voltage values.
4. Generate appropriate pulses to control the switching devices of the VSI.

The detailed operation of the control block is as follows. The three-phase voltages V_{abc} at the PCC are transformed from a three-phase abc system to a two-phase stationary frame (αβ) system using Clark transformation in (3). The transformation is based on two conditions. The first is that the α-axis is aligned with the axis of phase "a"-axis. The second condition is that the β-axis leads the α-axis with 90 degrees. Then, using Park transformation in (4), the system voltages are obtained in the rotating frame of reference. The grid angle (θ), used in (4), is obtained using the phase-locked loop (PLL) circuit shown in Figure 5.

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_o \end{bmatrix} = C \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix} \times \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (3)$$

Where,

C= 2/3 stands for constant voltage and current transformation, and

θ represents the transformation angle representing the vector position.

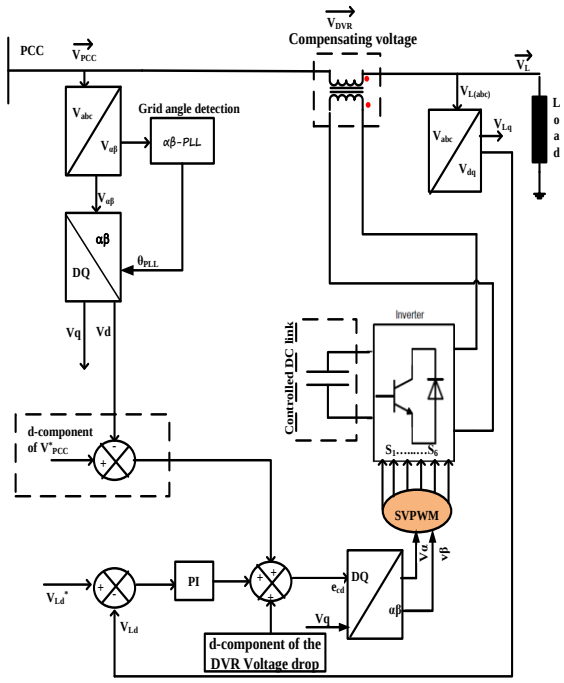

Figure 4. Structure of the DVR control circuit

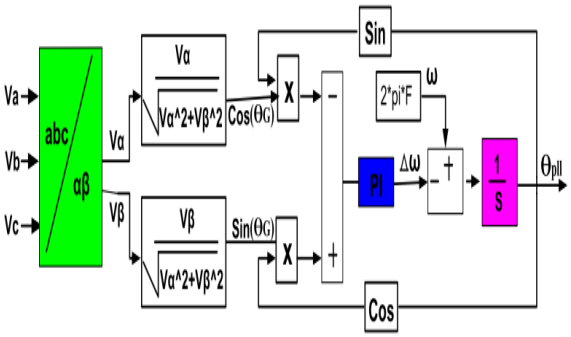

Figure 5. The control structure of αβ PLL

$$\begin{pmatrix} V_d \\ V_q \end{pmatrix} = \begin{pmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{pmatrix} \times \begin{pmatrix} V_\alpha \\ V_\beta \end{pmatrix} \quad (4)$$

The α-β stationary frame PLL (αβ-PLL) technique is widely used in three-phase grid-connected power converters because of its simple implementation and accurate estimation of the phase angle of the grid 24. Figure 5 illustrates the control structure of αβ-PLL implemented on Matlab/Simulink platform.

IV. SIMULATION RESULTS

A three-phase DVR closed-loop control algorithm based on synchronous reference frame theory is designed and simulated using Matlab /Simulink. The conditions of operation are mentioned in Table I. Applying disturbance at the PCC voltage (sag with ratio -30%) from t = 0.1 s to t= 0.2 s, resulted in a change from 311 Volts to 217.7 Volts (peak phase value).At t=0.25 s, disturbance (swell with ratio +30%) resulted in a change from 311 Volts to 379 Volts (peak phase value). Figure 6. (a) presents the voltage at the PCC (V_{PCC}) for both swell and sag disturbances. Figure 6. (b) shows the voltage in the stationary αβ frame where the voltage appears as two-phase sinusoidal quantities. Figure 6. (c) shows the voltage at the PCC in the rotating dq frame of reference. The figure shows that the time-varying quantities appear as DC quantities. It should be noted that as the d-axis is aligned with the axis of phase "a", V_q =0. Figure 7 shows the three-phase voltages both during normal operation and during disturbances (sag and swell). During normal operation, from t=0 to t=0.1 s, the DVR compensates only for the voltage drop across it (please refer to Figure 7.(a) and Figure 7. (b)). At t=0.1 s, to t=0.2 s, V_{PCC} undergoes a voltage sag of ≅30% of its nominal voltage to reach as low as 217.7 Volts. For the same time interval, the DVR produces an aiding voltage that counteracts this voltage sag to produce a load voltage that is disturbance-free (Figure 7.(b)). From t=0.2 to t=0.25 s, the system regains its nominal operating conditions. At t=0.25 s, to t=0.35 s, the voltage at the PCC undergoes a voltage swell of ≅30% of its nominal voltage to reach as high as 404 Volts. For the same time interval, the DVR produces an opposing voltage that counteracts this voltage swell to produce a load voltage that is disturbance-free.

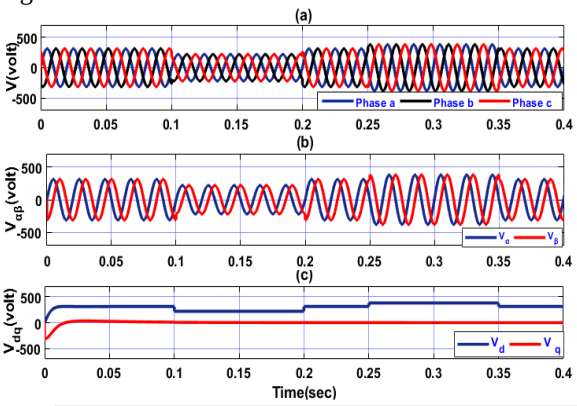

Figure 6. Voltage waveforms at the PCC in abc, αβ and dq frames

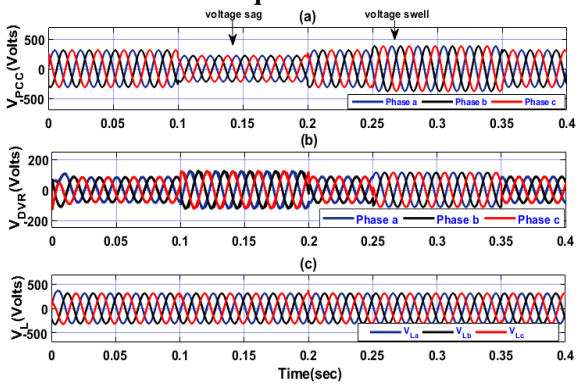

Figure 7. Three-phase sinusoidal voltages during sag and swell at the PCC

Figure 8 depicts the control action during sag within one cycle based on the power system frequency from t=0.1 s, to t=0.102 s. Figure 8.(b) provides a zoomed-in view of the disturbance interval shown in Figure 8.(a). It is shown that the proposed system takes less than 400 µs to reach a steady-state and counteract the disturbance.

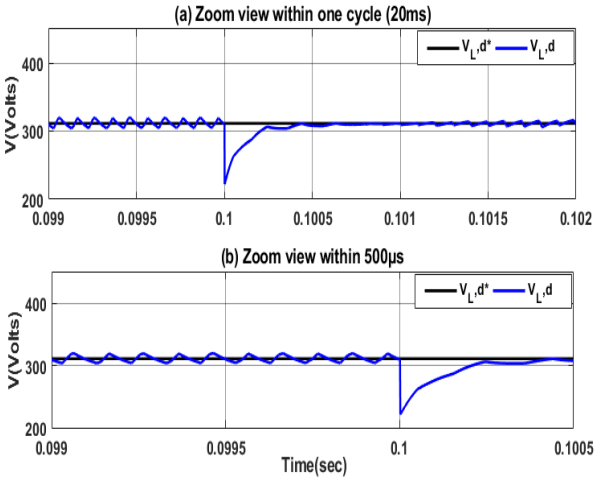

Figure 8. Zoomed-in view indicates the transient response of the control system during voltage sag

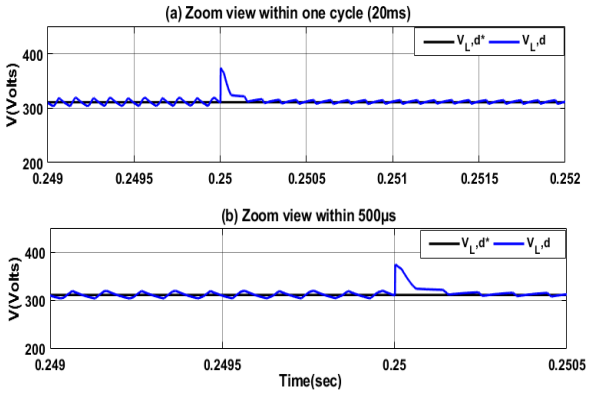

Figure 9. Zoomed in view indicates the transient response of the proposed controller during voltage swell

Figure 9.(a) shows the system behavior during swell disturbance which takes place from t=0.25 to t=0.35 s, Figure 9.(b) shows a zoomed-in view of the transient response at the start of swell within one cycle based on the power system frequency. The figure shows that the system takes approximately 400 µs to recover from the swell disturbance with zero steady-state error in both sag and swell cases. These results indicate that the controller is capable of coping with the disturbance which occurs at the source side with both excellent dynamic and steady-state responses.

Figure 10 presents the active and reactive power during sag and swell at the PCC. The figure shows that there is a reduction in active and reactive power delivered by the PCC during the sag and increase active and reactive power during the swell.

Figure 11 indicates the DVR active and reactive power compensation during sag and swell. The figure shows that DVR injects power during sag and absorbs it during voltage swell.

Figure 12 shows that the load does not suffer any disturbance in the power delivered to it throughout the whole period of operation. This indicates that DVR effectively mitigates sag and swell occurrence. illustrates the power flow in the proposed system. According to the values indicated in the Table II, the DVR can inject or absorb active and reactive power which compensates the load power in an excellent manner.

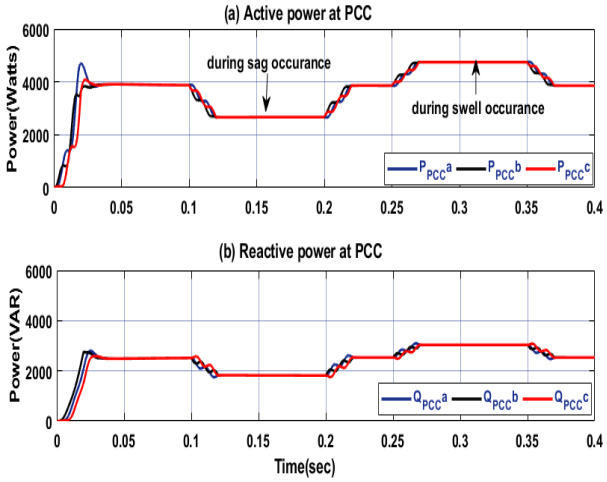

Figure 10. Active and reactive power at the grid side

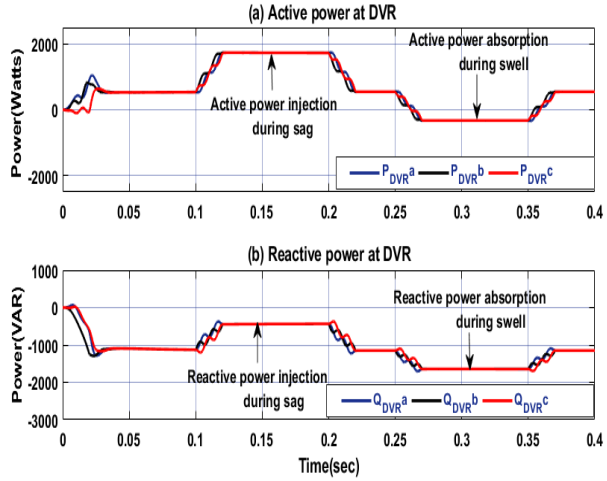

Figure 11. Active and reactive power injected by the DVR

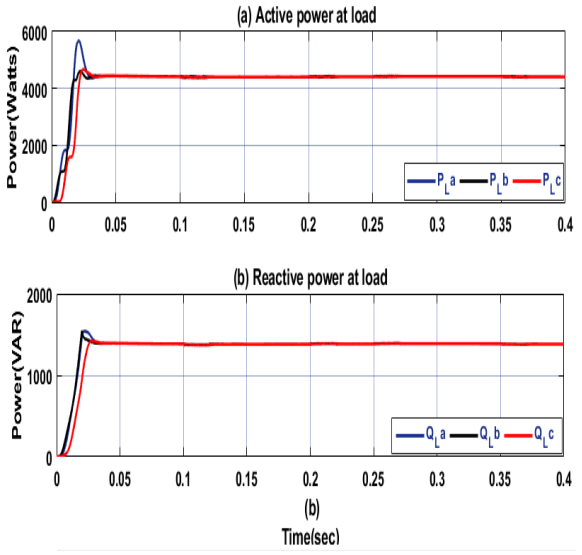

Figure 12. Active and reactive power at the load side

Table II: Power flow in the proposed system

Power / Status	Power at the grid side	Power injected by DVR	Load power
Without sag/swell	P≈3900 watt Q≈2500 var	P≈500 watt Q≈-1100 var	P≈4400 watt Q≈1390 var
During sag	P≈2660 watt Q≈1800var	P≈1740 watt Q≈-420var	P≈4400 watt Q≈1380 var
During swell	P≈5000 watt Q≈3200 var	P≈-600 watt Q≈-1800 var	P≈4400 watt Q≈1400 var

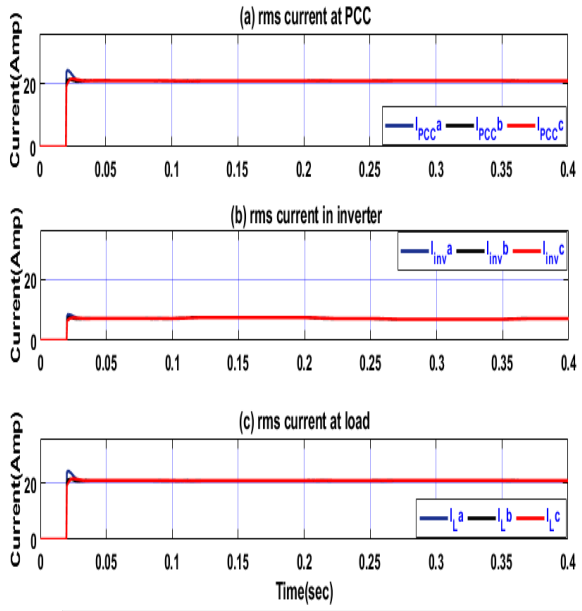

Figure 13. RMS currents in the proposed system.

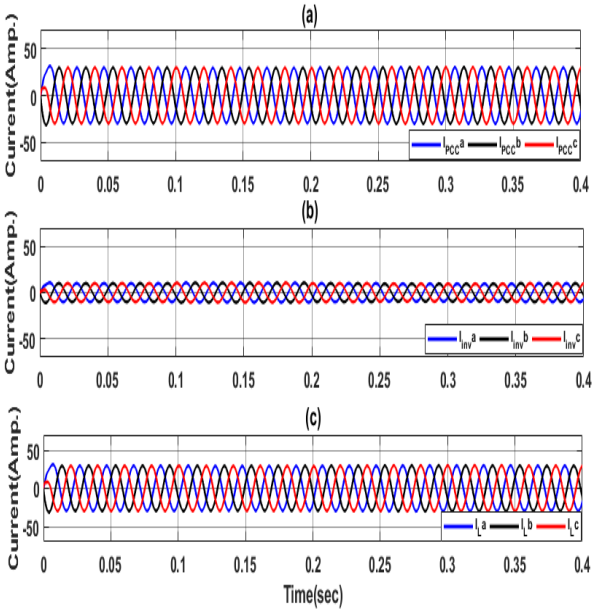

Figure 14. Three-phase sinusoidal currents in the proposed system.

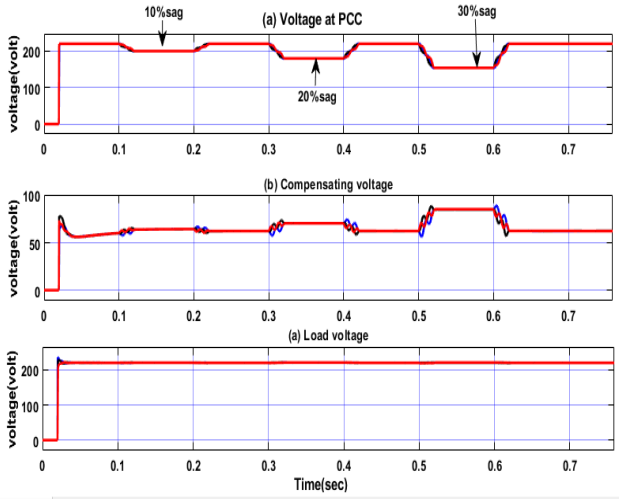

Figure 15. Different ratios of sag values and corresponding compensation

Figure 13 and Figure 14 depict the RMS and the three-phase sinusoidal currents in all systems. Since the transformer ratio is 3:1, the current in the inverter circuit is 1/3 the value of the current in the grid and load circuits. Figure 15 shows different ratios of sag values and the corresponding compensation. As depicted, the DVR can isolate the load from any disturbance (swell/sag) that might occur at the PCC by providing the proper voltage compensation.

V. CONCLUSION

This paper proposed an enhanced DVR control algorithm that achieved superior dynamic response against voltage sag and swell. The results indicate that the controller takes around 400 µs to reach a steady state. This rapid response is very essential in the case of a DVR device used as a protection device for sensitive loads. Incorporating the upstream disturbance detection term and compensating for the drop across the DVR itself help in achieving the necessary fast and accurate responses to mitigate the problems associated with voltage sag and swell.

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AUTHOR PROFILE

Zeinab Elkady was born in Qalubia–Egypt on August 31, 1985. She graduated from the Electrical Power and Machines Department of the Faculty of Engineering, Benha University in May 2007 with overall grade Very Good with honor degree. Graduation project was "Standalone photovoltaic system design and implementation using FPGA" using sparten3-E which supplied to the project by XLINIX as a sponsor. Participated in ROBOCON competition and achieved two prizes in two years. Worked as Researcher Assistant in Electronic Research Institute (ERI). Zeinab received her M.Sc. of Electrical Engineering (power system), 2014-2016, Benha University. Her specific fields of interest include power system Control, power quality, and Renewable Energy. Currently, she is an Assistant researcher at Electronic Research Institute-Egypt.

Naser Abdel-Rahim, Ph.D. Dr. Naser Abdel-Rahim currently holds the position of Professor in the Department of Electrical Engineering of Future University in Egypt. From 2013 to 2017 has been a Professor with the Faculty of Engineering at Shoubra, Benha University, Egypt. He received both his M. Eng. and Ph.D. degrees from the Memorial University of Newfoundland in Canada, in 1989 and 1995, respectively. As an Assistant Professor at the United Arab Emirates University (UAEU) from 2000 till 2005,

he obtained several research projects funding from the UAEU as well as from Asea Brown Boveri (ABB). Prof. Abdel-Rahim has numerous publications in international journals and refereed conferences, where he also served as a reviewer.

Ahmed A. Mansour was born in Qalubia - EGYPT on December 28, 1967. He graduated from the Electrical Power and Machines Department of the Faculty of Engineering - Zagzig University in May 1990. His specific fields of interest include Power Electronics and Power Quality systems. His experience on advanced power factor correction techniques based on both Static Var Compensators "SVC's", STATCOM systems and Active Power Filters (APF's) systems dedicated to harmonics compensation of the electrical non-linear loads. Mansour received his M.Sc. and Ph.D. from the faculty of Engineering of Cairo University in 1997 and 2004 respectively. Mansour is currently working as an associate professor researcher at the Power Electronics and Energy Conversion Systems Dept., Electronics Research Institute – Egypt.

Fahmy.M.Bendary received his B.Sc. degree from Ain Shams University, Egypt and his M.Sc. from Cairo University, Egypt in 1966 and 1979, respectively, and earned his Ph.D. degree from Paris, Sud university, France, in 1983. From 1984-1995, he was an associate professor at Zagazig University. Dr.Fahmy was promoted full professor of automatic control and its applications to power system in 1995. He is currently a professor of electric power systems and automatic control at the faculty of engineering (Shoubra), Benha University. He is a coauthor of more than one hundred research papers, and a reviewer for many local and international journals as well as conferences in the field of power system optimization, operation, planning, control, and renewable energy systems.