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Multi level Transformer less PV Inverter with Reduced Switching Losses and Elimination of CM leakage Current

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Abstract*: In order to have efficient operation of grid connected Photovoltaic (PV) inverter, the issue of leakage current must be completely eliminated. For this new transformerless multilevel inverter is proposed in this paper with (k-1) levels in which k denotes the number of switches. The inverter provides zero common mode leakage current and also capable of operating under half of rated PV voltage, hence make this proposed inverter topology as LVRT (low voltage ride through) capable. Different modes are employed for the stable operation of the proposed inverter with varying input PV voltage. Simulation work is carried out for three, five and seven level proposed inverter topologies in MATLAB/Simulink software which determines its maximum power point tracking performance. Here the THD (Total Harmonic Distortions) of 3, 5 and 7 levels are compared.

Keywords* : multilevel inverter, Transformerless PV inverter, common mode current, LVRT, Leakage Current.

I. INTRODUCTION

Conventional grid connected PV inverters consists of isolation transformer which are huge in size and also leads to more losses which results in reduction of efficiency. Hence, nowadays transformerless inverters are more popular in grid connected pv applications. But as there is no isolation provided, results in common mode (CM) leakage current flow due to variation in common mode voltages which leads to panel degrading, reduction in power quality, electromagnetic interference, Safety problems for operating personnel, etc., (1-4).The equivalent circuit for the general transformerless inverter is provided below in Fig 1.

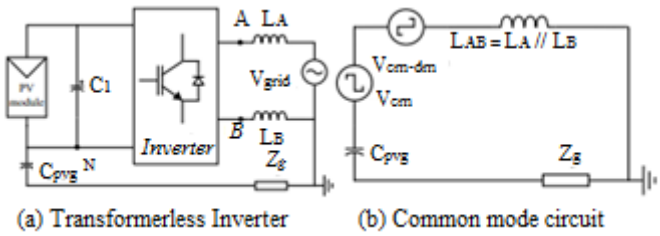

Fig 1. Conventional transformerless inverter with equivalent circuit

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In this,

$$V_{cm} = \frac{V_{AN}+V_{BN}}{2} \quad (1)$$

$$V_{dm} = V_{AN} - V_{BN} \quad (2)$$

The equivalent voltage, $V_{cm\text{-}dm}$ is given by

$$V_{cm-dm} = \frac{(V_{AN}-V_{BN})}{2}\left(\frac{L_2-L_1}{L_1+L_2}\right) \quad (3)$$

There are two methods to get zero leakage current which is given below:

1) To get zero equivalent voltage $V_{cm\text{-}dm}$and constant V_{cm}, i.e V_{AN}=V_{BN}
2) Designing circuit elements in such a way that sum of V_{cm} and $V_{cm\text{-}dm}$is zero.

The NPC inverters can be used as transformerless grid connected inverters (7-9) but the output voltage will be half of the input voltage and we have to add dc-dc converters for maintaining the output voltage of inverter as constant with varying PV voltage.
Additional switches can be added in order to avoid the common mode current path during freewheeling mode, on ac or dc side of the inverter.
But, the switches consist of varying junction capacitance, results in common mode leakage current flow (6,10).
The CM current can be reduced by active clamping but the cost gets increased due to additional capacitors and switches (12,13).
The PV negative terminal and grid neutral point are directly connected to eliminate the CM current and 3 level voltage is generated by the inverter with unipolar sinusoidal pulse width modulation (SPWM) technique (15,16). The filter size can be reduced by increasing the voltage levels with the help of multilevel inverters (18).
In this paper, a new multilevel inverter topology is provided as grid connected PV inverter and different operational modes are analyzed.
The control strategy for 3 level inverters is discussed and simulation is done with incremental conductance algorithm implemented as MPPT and verified of LVRT capability. The switching sequences for five and seven level inverters are discussed with simulation results.
The THD is measured for proposed multilevel inverter topology and compared for voltage levels of three, five and seven.

II. PROPOSED THREE LEVEL TRANSFORMERLESS INVERTER TOPOLOGY

The 3 level proposed inverter is provided below in Fig 2:

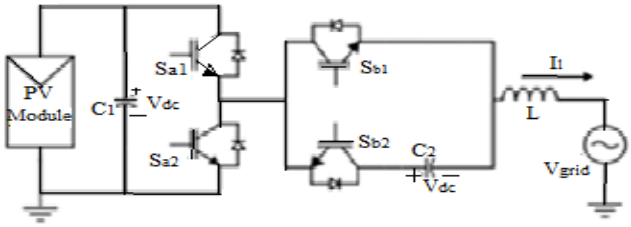

Fig.2. Proposed three level inverter

The proposed converter consist of two half bridges with capacitors C_1 and C_2 respectively. The negative terminal of the PV panel and grid neutral point is grounded. Hence $V_{BN}=0$ and $L_b=0$.

Therefore,

$$V_{CM} = \frac{V_{AN}}{2} \text{and} V_{CM-DM} = \frac{-V_{AN}}{2} \quad (4)$$

Hence the sum of above mentioned voltages V_{cm} and $V_{cm\text{-}dm}$ is zero, thereby making leakage currents also get zero. The proposed inverter eliminates the CM leakage current with less number of switches. It operates under two modes. When PV provides rated power, then the capacitor voltage will be $V_{dc}/2$ and when it operates below rated power, then the mode changes and the capacitor voltage will be forced to maintain as V_{dc}. The operational modes are provided below:

Mode 1:

Switching state 1:

The equivalent circuit of three level transformerless inverter for mode1 switching state 1 is shown in Fig 3.a.In this, S_{a1} and S_{b2} will operate and the load voltage will be $V_{dc}/2$. The capacitor C_2 gets charged and the voltage across it is maintained at $V_{dc}/2$.

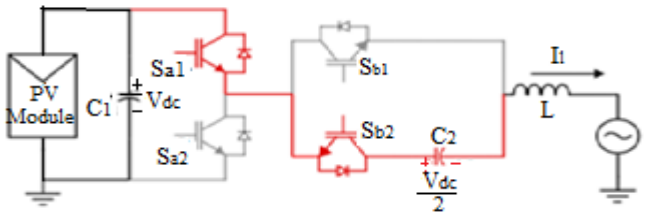

Fig. 3.a Mode1.1, Vo=$V_{dc}/2$

Switching state 2:

The equivalent circuit of three level transformerless inverter for mode1 switching state 2 is shown in Fig 3.b. In this, the switches S_{a2} and S_{b1} will be ON, the output voltage will be zero. The capacitor will be disconnected, neither charged nor discharged and the voltage across the capacitor will remains as $V_{dc}/2$.

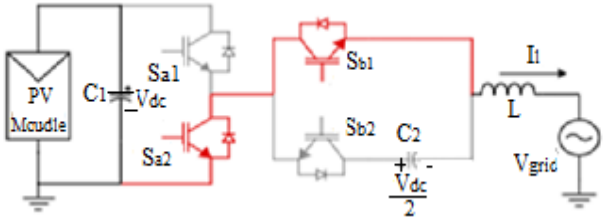

Fig. 3.b Mode1.2, Vo=0

Switching state 3:

The equivalent circuit of three level transformerless inverter for mode1 switching state 3 is shown in Fig 3.cIn this, the switches S_{a2} and S_{b2} will be ON, the load voltage is $-V_{dc}/2$. The capacitor C_2 will start discharging in this condition.

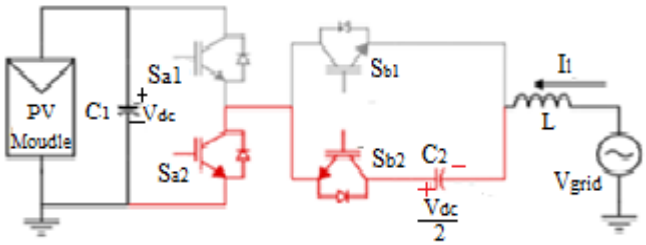

Fig. 3.c. Mode1.3, $V_o=-V_{dc}/2$

In this mode the voltage across the capacitor C_2 will be balanced naturally and maintained at $V_{dc}/2$. In this, the dc link voltage V_{dc} is provided as 600V. The switching table for different modes (Table I for mode 1 and Table II for mode 2) is provided below:

Table - I: Mode-1 Switching operation of Three level Inverter

V_o level	S_1	S_2	S_3	S_4	V_{c2}	Mode
$V_{dc}/2$	ON	OFF	OFF	ON	▲	Mode 1
Zero	OFF	ON	ON	OFF	NC	Mode 1
$-V_{dc}/2$	OFF	ON	OFF	ON	▼	Mode 1

Table - II: Mode-2 Switching operation of Three level Inverter

V_o level	S_1	S_2	S_3	S_4	V_{c2}	Mode
V_{dc}	ON	OFF	ON	OFF	NC	Mode 2
Zero	ON	OFF	OFF	ON	▲	Mode 2
$-V_{dc}$	OFF	ON	OFF	ON	▼	Mode 2

The inverter voltage and current along with capacitor voltage is provided in the following graphs in Fig 4:

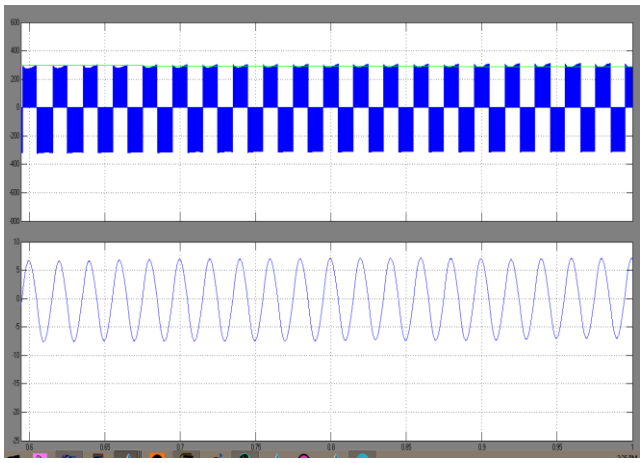

Fig 4 Three level Inverter voltage and current

III. CLOSED LOOP CONROL

The proposed current mode controller block diagram is shown below in Fig 5:

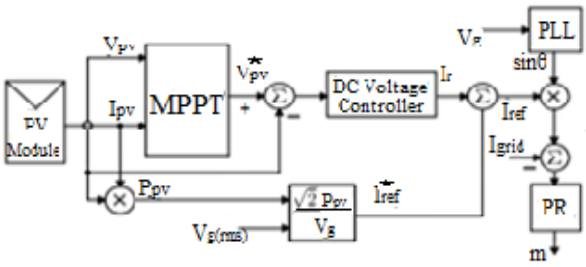

Fig. 5. Control circuit for proposed inverter

The reference voltage for PV is derived from incremental conductance (IC) algorithm based MPPT. The fundamental concept of the IC algorithm based MPPT is that the Voltage-Power (PV) curve have zero slope at MPP, so that with P=VI, ΔP/ΔV=0.The flowchart for IC algorithm is provided below in Fig 6:

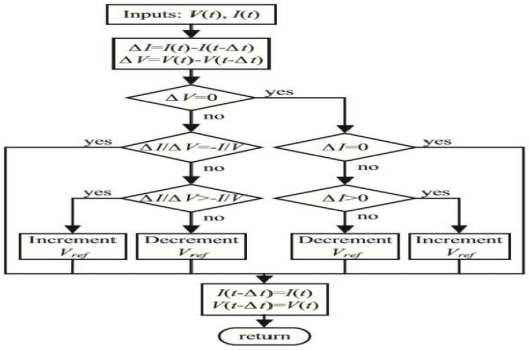

Fig 6 Algorithm for Incremental Conductance Method

The PI controller (Kp=0.8 and Ki =0.42) is employed for controlling the DC voltage. The PI controller acts as DC voltage controller which generates reference current from dc voltage error which is compared with grid current and the compensation current is provided to PR controller. The PR control transfer function is provided below:

$$G_c(s) = K_p + K_i \frac{s}{s^2+\omega^2} \quad (5)$$

The modulation index is generated by PR controller which is provided to SPWM for pulse generation. In mode 1, the capacitor voltage gets balanced without any control but in mode 2, the voltage balance is to be maintained by using the following algorithm as shown in Fig 7,

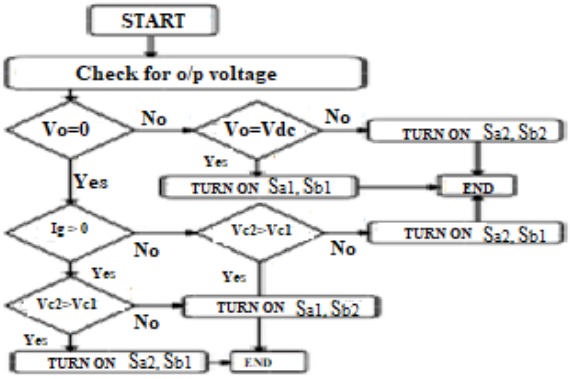

Fig. 7. Switching Algorithm for mode 2 operation of proposed inverter

The simulation circuit parameters are provided in Table III as follows:

Table - III Simulation Parameters

Parameters	Values
PV Voltage	600V
PV Power	2000W
Grid Voltage	220V
Switching Frequency	5KHZ
Filter Inductor	L_f= 0.1mH
Capacitors	$C_1=C_2=C_3$=1mF and C_{in}=10μF

Then the grid voltage is reduced to 110V, and the voltage and current of grid and inverter is measured as shown in Fig 8.

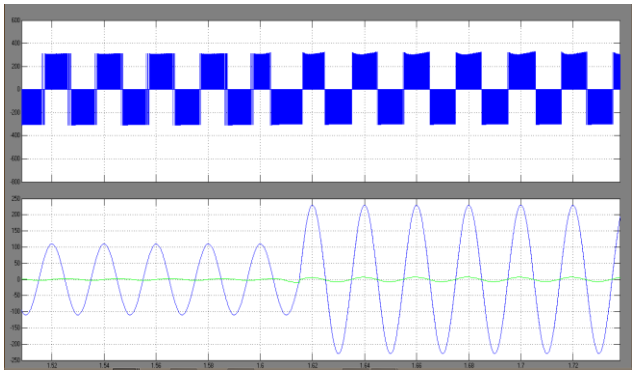

Fig. 8. Reactive power injection in LVRT condition

From the shift in phase angle of current waveform, we can get that the reactive power is generated from the proposed PV inverter and fed to the grid. This demonstration provides the LVRT capability of the proposed inverter. The harmonics present in the inverter current can be measured in terms of THD which is provided in Fig 9:

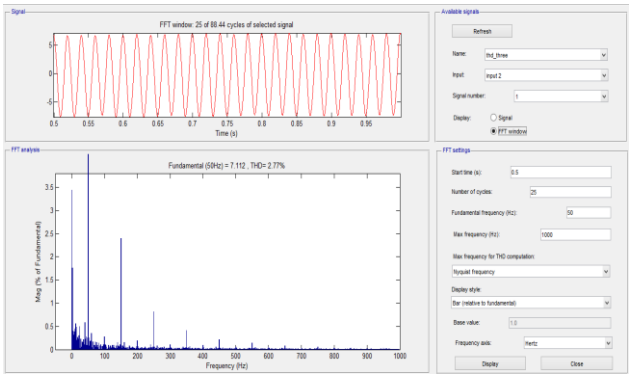

Fig. 9. THD of Three level Inverter current

The THD value is coming as 2.77% for three level proposed inverter.

IV. FIVE LEVEL TRANSFORMERLESS INVERTER TOPOLOGY

The proposed inverter topology is similar to modular multilevel inverter, as the levels can be increased by adding the modules of half bridge to the inverter.

The five level proposed inverter is provided below in Fig 10:

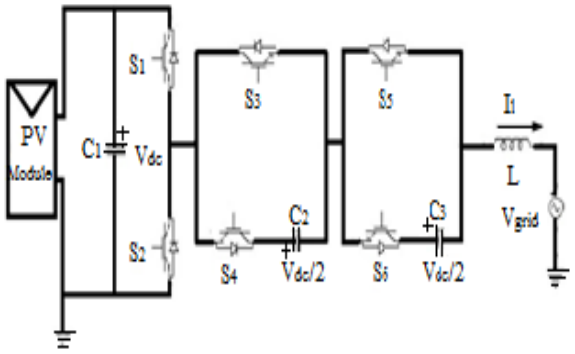

Fig.10. Five level proposed Inverter

It consists of three half bridges with six switches and capacitors C_1, C_2 and C_3. The voltage across C_1 is V_{dc} and across C_2 and C_3 is $V_{dc}/2$. When the inverter output is V_{dc}, C_1 is directly connected to grid while when it is $V_{dc}/2$, C_2 or C_3 will be connected along with C_1. During positive cycle, the capacitors C_2 and C_3 will be charged while during negative cycle it is discharged. The control strategy is same as for 3 level inverter topology. The switching sequence of the 5L proposed inverter topolgy is provided in the following Table IV:

Table - IV.Switching sequence of 5L Inverter

V_oLevels	S_1	S_2	S_3	S_4	S_5	S_6	V_{c2}	V_{c3}
V_{dc}	1	0	1	0	1	0	NC	NC
$\frac{V_{dc}}{2}$	1	0	1	0	0	1	NC	▲
$\frac{V_{dc}}{2}$	1	0	0	1	1	0	▲	NC
Zero	0	1	1	0	1	0	NC	NC
$\frac{-V_{dc}}{2}$	0	1	1	0	0	1	NC	▼
$\frac{-V_{dc}}{2}$	0	1	0	1	1	0	▼	NC
$-V_{dc}$	0	1	0	1	0	1	▼	▼

The current and voltage waveforms of 5L inverter along with capacitor voltages are provided below Fig 11:

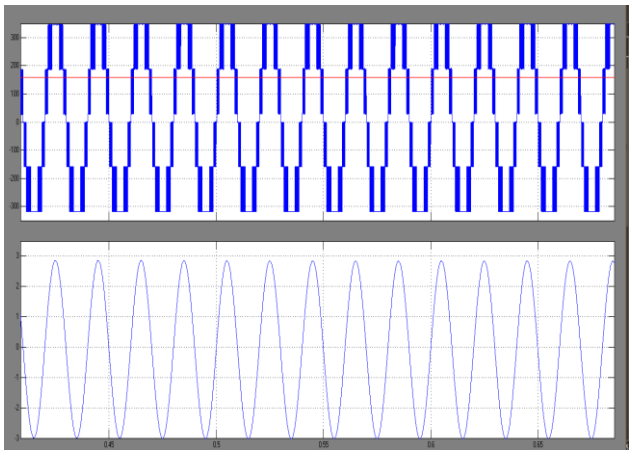

Fig.11. 5L Inverter voltage and current

In this, the voltage across the capacitors C_2 and C_3 are maintained as $V_{dc}/2$ i.e 150V where the voltage across C_1 is 300V (V_{dc}).

The THD of the five level inverter current is provided in Fig 12:

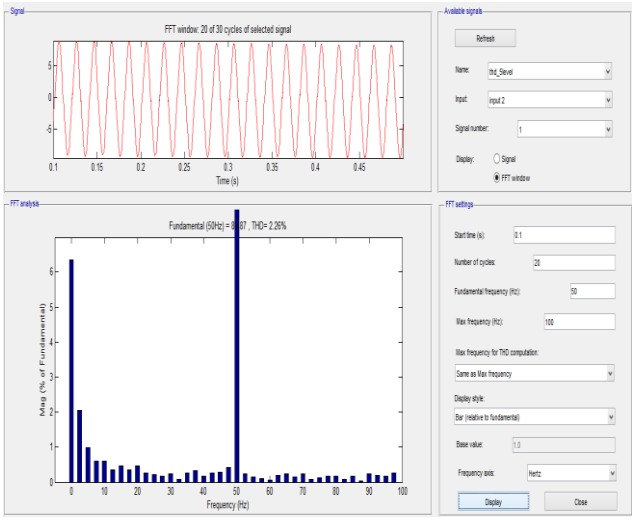

Fig. 12. THD for five level Inverter current

The THD value is 2.26% for five level proposed transformerless PV inverter.

V. SEVEN LEVEL TRANSFORMERLESS INVERTER TOPOLOGY

The proposed 7L inverter is provided below in Fig 13:

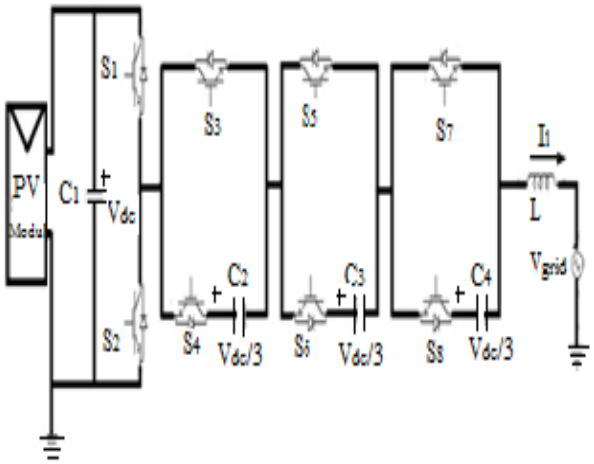

Fig. 13. Seven level proposed Inverter

It consists of four half bridges with eight switches and four capacitors. The voltage across C_1 is V_{dc} and across C_2, C_3 and C_4 is $V_{dc}/3$.

When the inverter output is V_{dc}, C_1 is directly connected to grid while when it is $V_{dc}/3$, any two of the three capacitors C_2, C_3 or C_4 will be connected along with C_1.

For $2V_{dc}/3$ level, any one of the three capacitors will be connected along with C_1.

During positive cycle, the sub module capacitors will be charged while during negative cycle it is discharged.

The switching sequence for the 7L proposed inverter topolgy is provided below in Table V:

Table – V: Switching sequence of 7L Inverter

V_o	S_{a1}	S_{a2}	S_{b1}	S_{b2}	S_{c1}	S_{c2}	S_{d1}	S_{d2}	V_{c1}	V_{c2}	V_{c3}
V_{dc}	1	-	1	-	1	-	1	-	NC	NC	NC
$\frac{2V_{dc}}{3}$	1	-	-	-	1	-	1	-	▲	NC	NC
$\frac{2V_{dc}}{3}$	1	-	-	-		1	1	-	NC	▲	NC
$\frac{2V_{dc}}{3}$	1	-	-	-	1			1	NC	NC	▲
$\frac{V_{dc}}{3}$	1	-	-	1		1	1	-	▲	▲	NC
Zero	-	1		1	1	-	1	-	NC	NC	NC
$\frac{-V_{dc}}{3}$	-	1		1	1	-	1	-	▼	NC	NC
$\frac{-2V_{dc}}{3}$	-	1		1		1	1	-	▼	▼	NC
$-V_{dc}$	-	1		1		1		1	▼	▼	▼

The voltage and current waveforms of proposed seven level inverter along with capacitor voltages are provided below in Fig 14:

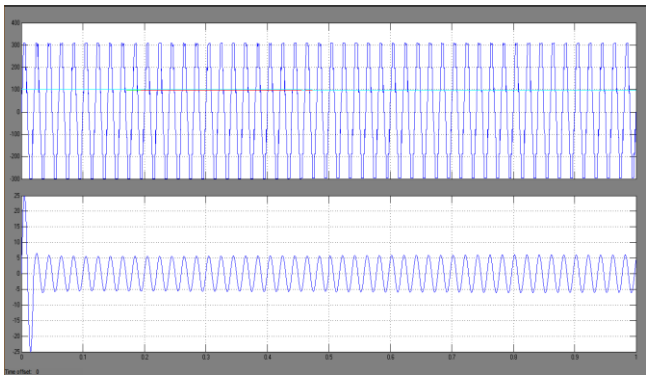

Fig. 14. 7L inverter voltage and current waveforms

In this, the capacitor voltages$V_{C2}V_{C3}$ and V_{C4} are maintained as $V_{dc}/3$ i.e 100V where V_{c1} is 300V (V_{dc}).

The size of the filter inductors will be reduced by adding the number of levels. Also as the voltage gets distributed across the half bridges, when adding the voltage levels, the number of half bridges will also increased and the voltage for each half bridge will reduce accordingly and hence the stress across

the switches in each half bridge will be reduced. The switching losses and %THD for 3, 5 and 7 level inverters are provided in Table VI.

The THD of the 7L inverter current is provided in Fig 15:

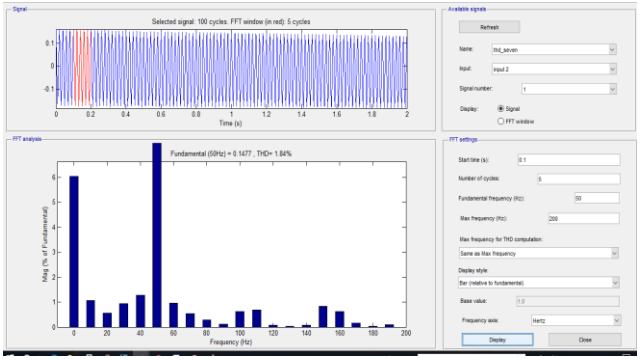

Fig. 15. THD for Seven level Inverter current

The THD value is 1.84% for seven level proposed transformerless PV inverter.

Table – VI: Comparison of proposed Three, Five and Seven Level Inverters

No of levels	No of switches	Switching losses(W)	THD	Capacitors/Voltage
Three level	4	16.29	2.77%	10mF/300V[1] 10mF/150V[1]
Five level	6	7.2	2.26%	10mF/300V[1] 10mF/150V[2]
Seven level	8	4.6	1.84%	10mF/300V[1] 10mF/100V[3]

VI. CONCLUSION

A new transformerless multilevel inverter topology was proposed in this paper and performance of three, five and seven level inverters are compared.

The proposed inverter was tested under half of rated pv voltage and grid voltage, thusthe proposed inverter topology is proved as LVRT capable and here maximum power is maintained through incremental conductance method which is more efficient in pv system.

Different modes was employed for the stable operation of the proposed multilevel inverter with varying input PV voltage and the performance of the proposed inverter is analysed with the help of a table for different levels.

The voltage levels can be still increased by adding the half bridge modules with same proposed control technique.

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