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Novel Design of Low-Power High-Speed Hybrid Full Adder Design using Gate Diffusion Input (GDI) Technique

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Abstract: ***VLSI technology become one of the most significant and demandable because of the characteristics like device portability, device size, large amount of features, expenditure, consistency, rapidity and many others. Multipliers and Adders place an important role in various digital systems such as computers, process controllers and signal processors in order to achieve high speed and low power. Two input XOR/XNOR gate and 2:1 multiplexer modules are used to design the Hybrid Full adders. The XOR/XNOR gate is the key punter of power included in the Full adder cell. However this circuit increases the delay, area and critical path delay. Hence, the optimum design of the XOR/XNOR is required to reduce the power consumption of the Full adder Cell. So a 6 New Hybrid Full adder circuits are proposed based on the Novel Full-Swing XOR/XNOR gates and a New Gate Diffusion Input (GDI) design of Full adder with high-swing outputs. The speed, power consumption, power delay product and driving capability are the merits of the each proposed circuits. This circuit simulation was carried used cadence virtuoso EDA tool. The simulation results based on the 90nm CMOS process technology model.***

Keywords: Full adder(FA), GDI, VLSI, Full-Swing, CMOS.

I. INTRODUCTION

In the present world everyone was busy with the electronic devices which must available for the long working hours and taking it as serious consideration regarding power saving. As the population is growing rapidly the usage of battery operate devices are also increased, so that the designing of the electronic devices with more number of chips, complexity and number of transistors in a chip and power consumption is also growing.The most commonly unit in the circuits is full adder which used for performing arithmetic operations such as multipliers, compressors, large adders. So to reduce the power consumption problem in all the electronic devices one can reduce it by the reduction of power in the full adders because it is available in all the electronic devices so which reduce the power consumption of whole system. The basic structure of the full adder consists of the XOR/XNOR gates which are the main cause for power consumption.In this paper the basic gates for the design of full adders are of novel full swing category and the design is of a New Gate Diffusion Input (GDI) with high swing output and less area.

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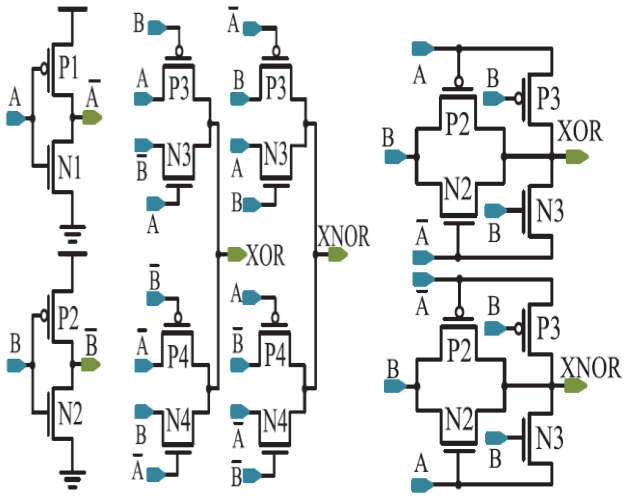
The simulation is carried by the software tool cadence virtuoso EDA tool. The evaluation is carried out several times to verify the proposed method is better than the previous existing methods. The repose of the paper is as follows. In section II analysis of the XOR and XNOR gates with different circuits and section III consisting of the novel full swing XOR and XNOR gates are proposed. Section IV provides the advantages of proposed methods over the other investigated methods and comparing the results in the section V and finally concluding the results in section VI.

II. ANALYSIS OF CIRCUITS

A. XOR-XNOR Gates

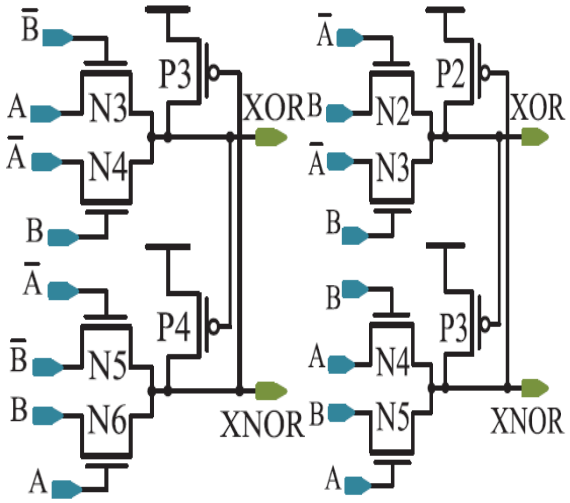
XOR/XNOR and 2 to 1 multiplexer are the two modules included in the design of Hybrid FAs.In the FA cell, the most power consumer is XOR/XNOR gate.The optimum design of the XOR/XNOR gate will reduce the power consumption of the FA cell.In the design of digital circuits, the XOR/XNOR gate has also many applications. Fig. 1 shows few examples of the most efficient of the many proposed circuits to implement XOR/XNOR gate. This structure has eight transistors. The critical path of the circuit includes two high power consumption NOT gates which is the main problem of this circuit as the output capacitance must be driven by the NOT gates. The lower critical path delay can be obtained by the incrementing the size of the transistors in the NOT gates. In addition, the intermediate node with large capacitance is created which means the NOT gates drives the output of circuit i.e. pass transistor or TG. Consequently the short circuit power and the total power dissipation of the circuit are extensively increased. The critical path delay will increased in the optimum PDP situation slightly.

six new FA circuits are existing in this work used for various applications. The proposed XOR/XNOR or Simultaneous XOR-XNOR circuits are used to design the six types of hybrid full adder circuits with different types of logic styles. The Four-transitor 2-1 multilplexer is also used in the designing of hybrid full adder structure. These 2-1 MUX does not have stactic and short -circuit power dissipation because this circuit is designed by using TG (tansmission gate logic style).The power consumption and delay of HFA-20T and HFA-19T are greater than that of HFA-22T and HFA-19T.

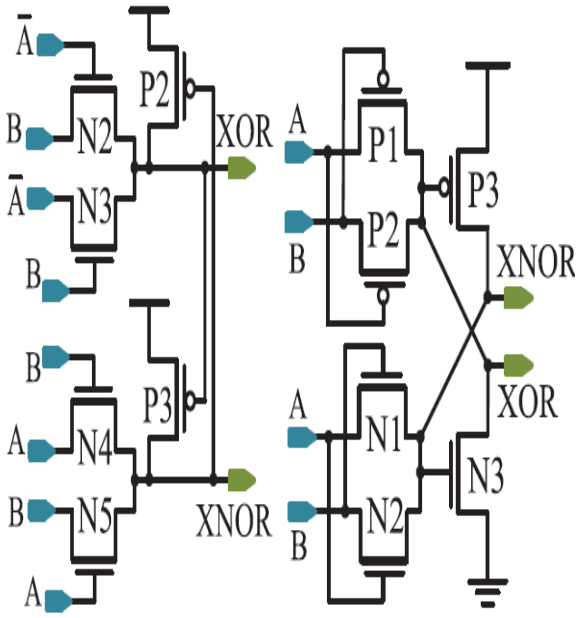


(a) (b)

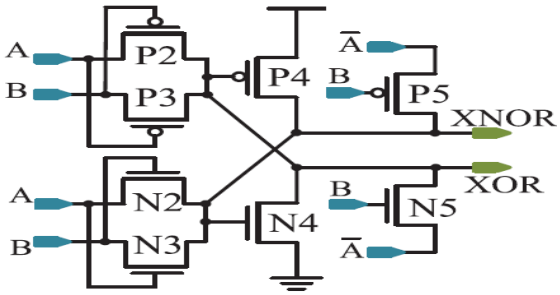
Fig.1.(a) and (b)The Full swing XOR/XNOR gate circuits



(c) (d)



(e) (f)



(g)

Fig.2.(c)-(g)The Full swing XOR-XNOR gate circuits

The full-swing XOR/XNOR gate in which each made of six transistors is the another example as shown in Fig. 1(b). Compared to the circuit shown in Fig. 1(a), this circuit is designed on the basis of PTL logic style and the power consumption and delay are best. The usage of NOT gate on the critical path of the circuit is the only problem of this structure. The XNOR circuit has more delay than XOR gate as shown in Fig. 1(b). NOT gates with NMOS transistor (N3) are included in the critical path of the XOR circuit, but the NOT gates with PMOS transistor are included in the critical path of XNOR (NMOS transistor is faster than PMOS). Therefore, the size of NOT gates and PMOS transistor (P5) should not be increased to improve the speed of the XNOR circuit.

B. Simultaneous XOR-XNOR Circuits

The simultaneous XOR/XNOR circuit is widely used in the recent years for the hybrid FA structures where the XOR-XNOR signals are connected as select lines to the inputs of 2-1 MUX so that the FA output nodes glitches must be avoid by using the two simultaneous signals with the same delay. The simultaneous XOR-XNOR circuit as an example depicted in Fig. 1(C). The circuit has been designed by using ten transistors which is based on the CPL logic style. To recover the output-level voltages two PMOS transistors are connected to as cross coupled and the outputs are driven by only NMOS transistors. The size of the transistors should be increased so as to mitigate the imposed delay and this further reduces the problem of having feedback increasing the delay and short circuit power of the XOR/XNOR structure.

Existence of two NOT gates in the critical path is considered as another disadvantage of the structure. The logic '0' is passed via N2 transistor to XOR output and the transistors N3, N4 and N5 are turned OFF when the inputs are AB = 00 in the Fig. 1(d). the transistor P3 helps to charge the XNOR output to VDD because of the logic ''0" on XOR. So that this circuit is having larger critical path than that of the circuit in Fig. 1(c). When the input is changed from AB = 01 to AB = 00 then the short-circuit current will be passed through it. Logic ''0'' is passed through the transistor N4 to XNOR output and logic ''1'' is passed via transistors N2, N3 and P2 to XOR output when the inputs are AB = 01 and when changed to AB = 00 except transistors N2 and P2 all transistors will be turned OFF.

Hence from the transistors P2 and N2, the short circuit current will pass to the remaining transistors. The outputs of XOR and XNOR does not changes and also the short circuit current will continue to be drawn from VDD if the amount of current sinking from the transistor is less than the amount of current being sourced from the transistor P2. The proper functioning of the circuit is impacted by the change of inputs AB = 11 to AB = 10 and the same situation occurs. The ON-state resistance of the transistors Pw and P3 must be greater than the transistors N2 and N5 (RP2 > RN2, RP3 > RN5) correspondingly to ensure the proper operation of the circuit. The circuit operation is altered if the transistor is changed and also this structure is very sensitive to process variation. Fig. 1(e) depicts the proposed full swing XOR-XNOR gate with only six transistors as in [7] and [13]

When the input is AB = 00, 11 then the two complementary feedback transistors N3 and P3 retains the weak logic in XOR and XNOR output nodes. The output reaches its final voltage value in two steps when the inputs changes from AB = 01, 10 to AB = 11, 00 and in addition to this the circuit suffers from the high worst case delay. The logic ‘‘1’’ is passed through the XOR output transistor N2 and the logic ‘‘0’’ is passed through the XNOR output transistor P2 to clarify the issue when the inputs equal to AB = 10. XOR node is initially at high impedance indicates the transistors P1 and P2 are in OFF state when the input mode is change to AB = 11, this further passes weak logic ‘‘1’’ (VDD-Vthn) to the XNOR output through the transistors N1 and N2. The feedback transistor N3 is turned because of the weak logic ‘1’ on the XNOR which further pull down the XOR output to weak logic ‘0’ yields the feedback transistor P3 to be turn ON. To overcome the issues in the negative feedback, positive feedback is made which finally make the XOR and XNOR outputs to have strong logic ‘1’ and logic ‘0’ correspondingly and slow reaction predicament is inferior in the low voltage operation.

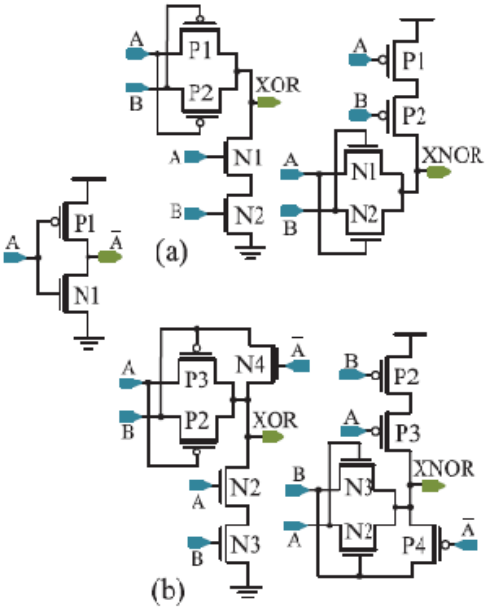


Fig.2. (a) Non full-swing XOR/XNOR gate (b) Modified full-swing XOR/XNOR gate.

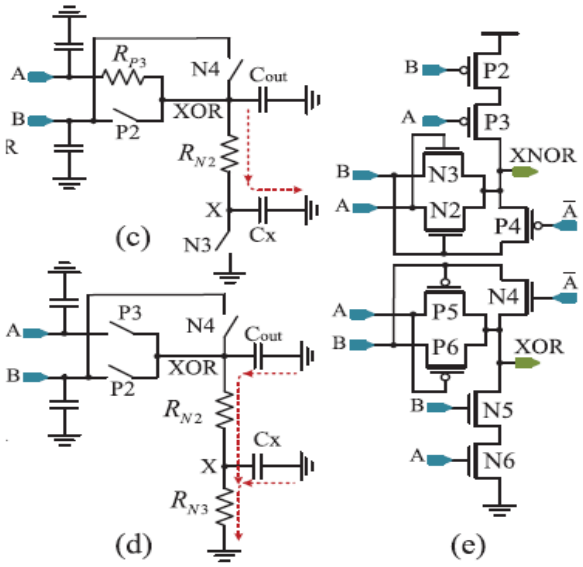


Fig.2. (c) *RC* model of proposed XOR for *AB* = 10. (d) *RC* model of proposed XOR for *AB* = 11. (e) Modified XOR–XNOR gate.

The short circuit current increases [the short circuit current passes through the circuit when one of the outputs of XOR or XNOR has high impedance and the feedback not acted properly]. The operation of the circuit may vary if the transistor size in the circuit is not selected properly. Thus process-voltage-temperature (PVT) variations made the structure most sensitive. A new structure of the simultaneous XOR-XNOR gate have been proposed by Chang et al in [18] shown in the Fig. 1(f) by improving the 6T XOR-XNOR circuit in Fig. 1(e). To solve the problems like slow response and low voltage supply operation as in the Fig. 1(f), two NMOS transistors for AB = 11 and two PMOS transistors for AB = 0 are included to the outputs of XOR and XNOR respectively. Good driving capability, full swing output, and robustness against transistor sizing and supply voltage scaling, all these parameters made the structure more advantageous. The structure of feedback is the main problem in this circuit which changes the XOR and XNOR output nodes with extra parasitic capacitance. Hence there is significant increase in the delay and the power consumption of the circuit. The structure in the Fig. 1(e) is improved as shown in Fig. 1(g) in which, the circuit speed is increased by inclusion of a NOT gate so that it is having better speed than the circuit in Fig. 1(e). Because of this the transistors N5 and P5 have the path from GND or VDD to the output nodes in two states of inputs AB = X1 for N5 transistor and AB = X0 for P5 transistor. There is only one same path for only one state of inputs AB = 11 for transistor N4 and AB = 00 for transistor P5 in the circuit of Fig. 1(e). The power consumption of the circuit increased due to the creation of the intermediate node with a large capacitance because of the addition of a NOT gate. Consequently, the circuit in Fig. 1(g) has more power consumption than the circuit in Fig. 1(e). Two simultaneous XOR-XNOR gates are formed by the combination of two XOR and XNOR circuits depicted in Fig. 1(a) and Fig. 1(b). The advantages and disadvantages of these new structures are similar to their XOR/XNOR circuits.

III. PROPOSED METHOD

This section gives the details regarding the proposed low power full adder with a new logic approach and then illustrated the proposed full adder

A. Proposed Full Adder Cell Circuit (Ss10t):

The proposed Gate Diffusion Input (GDI) cell is as shown in Fig. 3 and this intellect design is more flexible for digital circuits. The power dissipation is optimized by this method and also the transistor count is reduced. The unique advantages of the GDI technique are tow transistor implementation of complex logic functions and under certain conditions in cell swing restoration within existing low power design techniques. The figure shows the XOR gate using GDI technique. Using small number of devices, most logic functions can be implemented.

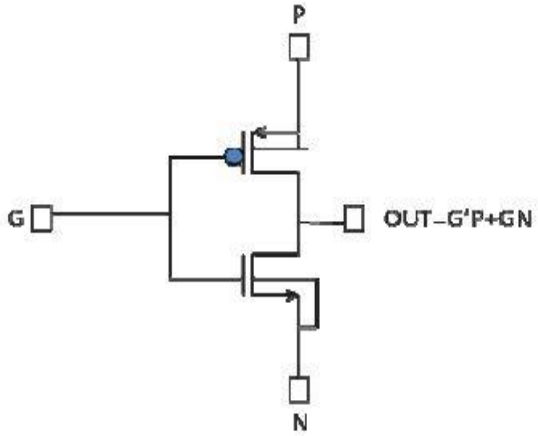


Fig.3.GDI Circuit

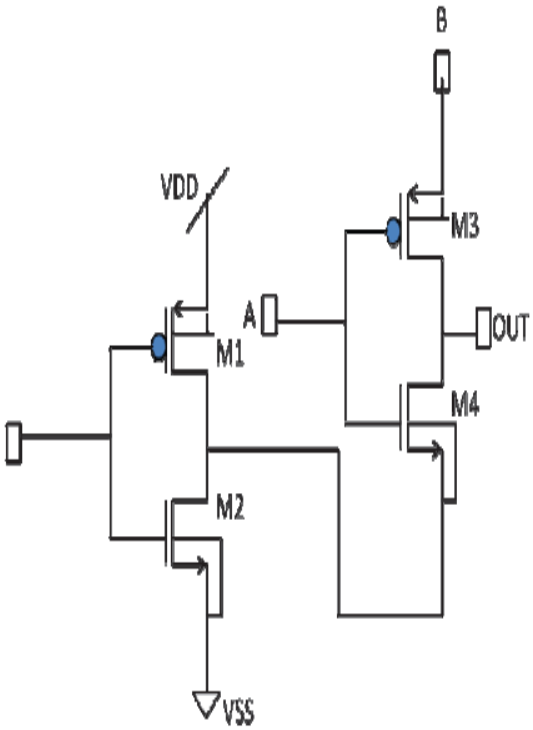


Fig.4.GDI Based XOR Circuit

Table- I :Truth table for GDI XOR gate

A	B	Out
0	0	Vtp
0	1	V_{dd}
1	0	V_{dd}-V_{tn}
1	1	0

From the Table 1 it can be observed that there is loss in GDI based XOR output when B ='0' .i.e., which is the threshold loss, when M1 and M3 transistors turns ON for A = '0' and B = '0' or M1 and M4 turns ON for A = '1' and B = '0'. To restore the sustainable and acceptable logic levels for solving the issues, one can manipulate the aspect ratios i.e. width to length (W/L) ratio of PMOS and NMOS transistors. The circuit diagram of GDI XOR based 10T full adder is as shown in Fig. 4 and the W/L ratios are represented in the circuit itself for the transistors. The threshold voltages of PMOS and NMOS circuits are Vtp and Vtn repectively can be observed suppose the circuit is working with highest supply VDD and the input vector is ABCin = '001'.

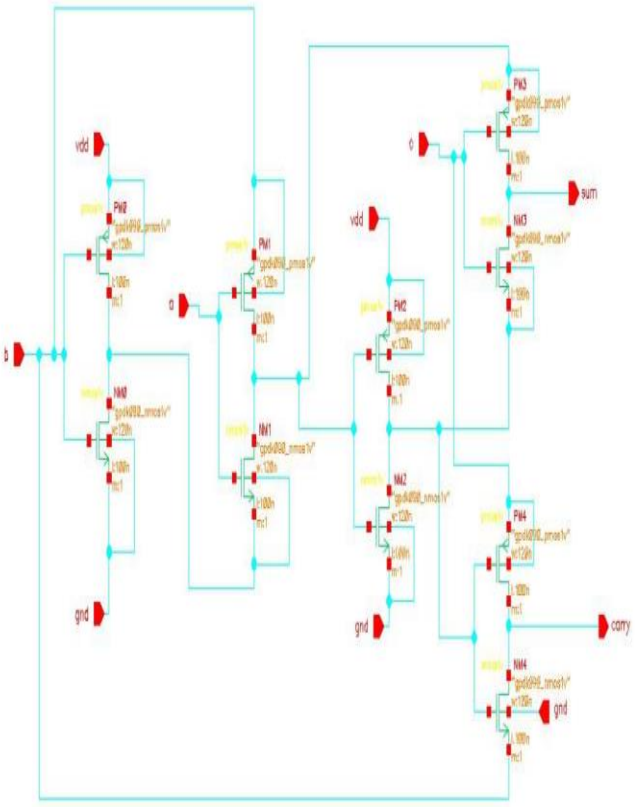


Fig.5.GDI Based 10T Full Adder

IV. SIMULATION SETUP

The test circuits as shown in Fig. 4 are added with output loads and input buffers. The whole circuit power and delay calculation involved the inverters power and delay so that the complexity id increased in the computations. 1-bit cells are used to implement the 4-bit adder, to study the properties of the compared circuits in cascaded fashion.

The size of the cells in the adder is same as the size of each cell in transistor. Propagation delay is used to find the performance of the circuits under test and it is calculated 50% of voltage level of input to 50% of voltage level of output. In all the simulations, 5% of the pulse width will gives the rise time and fall time of the input signals. Total average power consumption will gives the power in this study and the calculation of the power delay product is the convolution of the worst case delay and average power consumption.

V. RESULTS

The average power, delay and power delay product (PDP) are the parameters used to compare the hybrid full adders with the GDI full adders. Cadence virtuoso 90nm CMOS technology is used to simulate all the results. The product of delay and average power is defined as the PDP which determines the performance of the digital circuits. Simulation results are obtained using Cadence virtuoso 90nm CMOS technology.

Table- II: Simulation Results for XOR/XNOR Circuits

DESIGNS	TYPE	DELAY(ns)	POWER(µW)	PDP(fJ)
Full swing XOR/XNOR Gate (fig 1a)	XOR	50.10	1.87	93.6
	XNOR	40.05	1.85	74.09
Full swing XOR/XNOR Gate (fig 1b)	XOR	40.02	**1.23**	49.22
	XNOR	50.05	1.25	62.56
Modified Full swing XOR/XNOR Circuit(fig 2b)	XOR	30.09	1.28	**38.51**
	XNOR	**30.03**	1.72	51.65

Table-III: Simulation Results for Simultaneous XOR-XNOR Circuits

DESIGN	DELAY(ns)	POWER(µW)	PDP(Fj)
Simultaneous XOR-XNOR(fig 1c)	50.06	5.39	269.82
Simultaneous XOR-XNOR(fig 1d)	60.04	4.11	246.70
Simultaneous XOR-XNOR(fig 1e)	90.13	2.63	237.04
Simultaneous XOR-XNOR(fig 1f)	40.02	2.99	119.65
Simultaneous XOR-XNOR(fig 1g)	30.03	3.09	92.79
Modified XOR-XNOR Gate(fig 2e)	**20.03**	**2.07**	**41.46**

Table IV: Simulation Results for Hybrid full adder Circuits and GDI full adder

DESIGN	DELAY(ns)	POWER(µW)	PDP(Fj)
HFA-20T	70.09	5.62	393.9
HFA-17T	70.23	5.56	390.47
HFA-B-26T	60.04	9.08	581.78
HFA-NB-26T	70.00	7.21	506.1
HFA-22T	50.06	6.76	331.39
HFA-19T	70.13	6.86	476.88
GDI Full adder(10T)	**34.89**	**1.202**	**41.93**

VI. CONCLUSION

In this paper, we proposed an efficient and low power design for full adder circuit. By using GDI technology 10T full adders are designed with reduced transistor count, low power dissipation and high performance. The proposed design is compared with six types of hybrid full adders, achieved 43% reduction in delay, 83% power consumption and 87% of PDP with GDI technology compared with Hybrid Full adder of 22T and the simulation results were performed in Cadence Virtuoso 90nm CMOS technology.

The applications of these types of full adders are with minimum area and low power requirement. It is used in the design of ALU, Multipliers and Multiplexers which are the most important circuits in the Digital Signal Processing and Digital Circuits Implementation. In the design process of Application Specific Integrated Circuits (ASIC), high performance adder is most important circuit in such type of designs our proposed adder can be used and it is also suitable for low power and high speed VLSI circuit applications.

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