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DesignandSimulation of High-Efficiency High Gain non Isolated Interleaved DC-DC Converter with Reduced Voltage Stress on the Devices

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***Abstract:** In this paper, a non-isolated two interleaved modified step up KY Converter is analyzed and designed, whose efficiency,the voltage conversion ratio is high. There are various types of non -isolated converters such as buck-boost, Cuk, SEPIC, ZETA converters, etc but the voltage gain of these converters is less compare to the proposed interleaved KY converters. The voltage gain, efficiency of the proposed converter is enhanced compared to the previous converters. The voltage stress on semi-conductor devices and the ripple in the input current is reduced because of this interleaving technique. Switches with low on-state resistance are used due to which the conduction losses are reduced. Steady-state analysis and the operating principle are studied in continuous conduction mode (CCM) at ideal conditions. Simulation is also carried out in MATLAB/Simulink for the proposed interleaved KY converter.*

***Keywords:** dc-dc converter, High voltage gain, Interleaved KY converter, Voltage stress.*

I.INTRODUCTION

As we all know that fossil fuels are being depleted day by day and they are also affecting the environment. So the renewable sources are being considered as an attractive feature by research scholars. Renewable resources like photovoltaic (PV), fuel cell, wind are commonly used but the output obtained by this is low dc voltage, to enhance this low dc voltage to higher value dc-dc converters are been used. In the case of PV there exist a shadow effect that cannot be neglected. In the present scenario, dc-dc converters are being widely used for various purposes, Such as battery power systems, uninterrupted power supply, etc. In SEPIC dc-dc converter efficiency-voltage gain is high where the output may be greater, equal, or less than the input voltage[1]. To have continuous input current for dc-dc convertor with low ripple double input source are used. Various conventional dc-dc converters have high voltage gain but due to their operating conditions and the parasitic element the voltage gain of the buck-boost, Cuk, SEPIC, ZETA converters have been restricted. Also, the stress on the semiconductor device is equal to the output voltage [2]. The voltage gain of the converters can also be increased by using a couple of inductors in a dc-dc converter. Thus a proper number of turns ratios must be chosen to increase the voltage gain[3].

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But higher the turns ration reduces the efficiency and causes higher EMI noise and power loss which can be overcome by using non-isolated converters which indeed have lower size, cost, and losses[4].The newly developed converter is proposed named as KY converters. In this converter, the voltage on the switches is less than the output voltage [5]. Also, the KY converters are very useful in supplying the power to the devices which will operate at low noise conditions they provide a very fast transient response which is similar to the buck converter [6]. The output current is non-pulsating of this KY converter. But still, the voltage gain of this converter can be enhanced [7]. In this paper a novel high step-up interleaved dc-dc converter is presented, This converter is proposed by interleaving two modified KY converters. The voltage conversion ratio of this converter is higher than the previously developed dc-dc converter like buck-boost, Cuk, SEPIC, ZETA convertors. The overall aim of this converter is to obtain high voltage gain, high efficiency, low voltage stress on the switches, and the other semiconductor devices.The low ripple in the input current and low switching and conduction losses.

II. PROPOSED INTERLEVED KY CONVERTER TOPOLOGY

Fig1 represents a step up non-isolated interleaved dc-dc converter. In this paper, the voltage gain of the switches is less than the output voltage, and also the ripple at the output voltage is reduced and the output current is non-pulsating. As they have previously developed various converters but the voltage gain of the proposed converter is larger i.e

$$M=1+3D/1-D \quad (1)$$

The interleaved modified KY converter consists of two IGBTswitches, four inductors L1, L2, L3, L4 four diode D1, D2, D3, D4 four capacitors C1, C2, C3, C4 and two output capacitor C_o1, C_o2 and the load. This converter is operated in CCM. To ease the steady-state analysis few assumptions are made:

1. All the parasitic parameters of the semiconductor devices are neglected.
2. All the semiconductor devices are in ideal condition.
3. The voltage of the capacitors is assumed to be constant as the size of the capacitors is considered to be large enough.

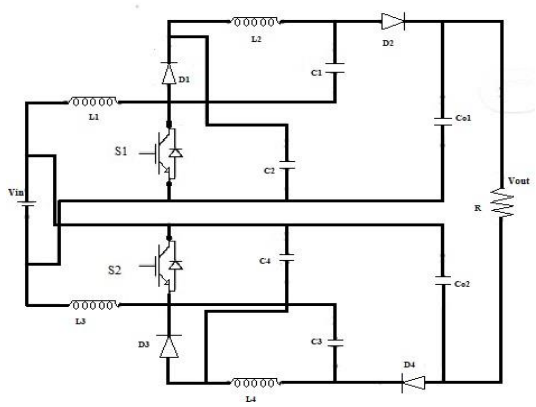


Fig 1. Equivalent circuit of interleaved KY converter

The interleaved KY converter operates in two modes:

A.Mode 1: The time interval for this mode is (t_o-t_1).In this mode the switches S_1, S_2 are in on state and all the four diodes D_1-D_4 are in off state. As the inductors are charged from the input source, the current through the inductors rises linearly. The capacitors C_1 and C_3 are charged and the capacitors C_2, C_4 C_{O1}, C_{O2} are discharged which were charged from the previous mode. The output capacitors also charge the load. Figure 2.(a) represents the current flow directions of mode 1. The voltage across the inductors are

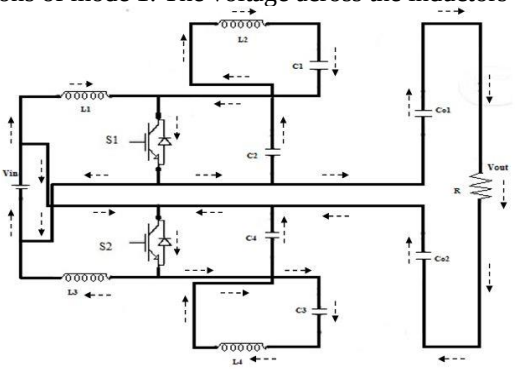


Fig 2(a). Mode 1 current directions

$V_{L1}= V_{in}$ (2)

$V_{L2}= V_{C2}- V_{C1}$ (3)

$V_{L3}= V_{in}$ (4)

$V_{L4}= V_{C4}- V_{C3}$ (5)

B.Mode 2: The time interval for this mode is (t_1-t_2). In this mode, both the switches are in off state and all the four diodes are in on state. The current through the inductors decreases to its minimum value, now the capacitors C_1 and C_3 are discharged and the capacitors C_2, C_4, C_{O1}, C_{O2}, Ro are charged through the diodes D_2 and D_4. For the next time-period the switches S_1 and S_2 have turned on again which ends mode 2.Figure 2 (b) represents the current flow direction of mode 2. The voltage across the inductors are:

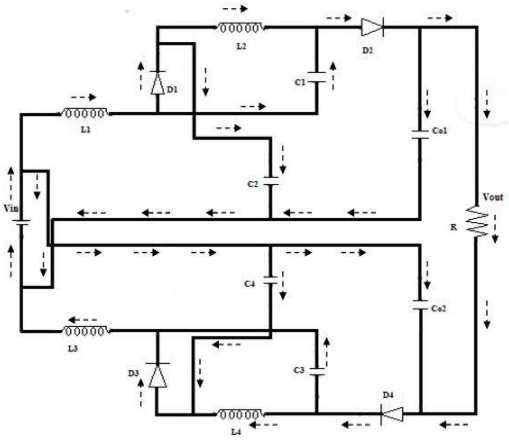


Fig 2(b). Mode 2 current directions

$V_{L1}= V_{in}-V_{C2}$ (6)

$V_{L2}= - V_{C1}$ (7)

$V_{L3}= V_{in}-V_{C4}$ (8)

$V_{L4}= - V_{C3}$ (9)

III. STEADY STATE ANALYSIS OF PROPOSED CONVERTER

To ease the analysis volt second balanced law of inductor is applied for the inductors L_1, L_2, L_3, L_4:

$V_{Li}= \int_0^{Ts}(VLi\ )dt$ (10)

$V_{L1}= \int_0^{DTs} Vindt + \int_{DTs}^{Ts}(Vin - Vc2)dt$ (11)

$V_{L2}= \int_0^{DTs}(Vc2 - Vc1)\ dt + \int_{DTs}^{TS}(-Vc2)dt$ (12)

$V_{L3}= \int_0^{DTs}(Vin)\ dt + \int_{DTs}^{TS}(Vin - Vc4)dt$ (13)

$V_{L4}== \int_0^{DTs}(Vc4 - Vc3)\ dt + \int_{DTs}^{TS}(-Vc3)dt$ (14)

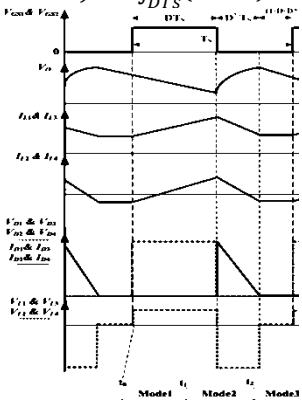


Fig 3.Key waveforms of interleaved ky converter in CCM

When KVL is applied in mode 1,the output voltage is

$Vo=V_{co1} -V_{in}+V_{co2}$ (15)

Similarly in mode 2

$V_{co1}=V_{c1}+V_{c2}$ (16)

$V_{co2}=V_{c3}+V_{c4}$ (17)

By equating equation 11 ,12 ,13 & 14 to zero ,we get

$V_{c1}= V_{c3}=\frac{D}{1-D}\ V_{in}$ (18)

$V_{c2}=V_{c4}=\frac{1}{1-D}V_{in}$ (19)

From The above equation 18 & 19

$V_{co1}=V_{co2}=\frac{D+1}{1-D}\ V_{in}$ (20)

From equation 15 & 20 the voltage gain of the converter is

$M=\frac{Vo}{Vin}=\frac{Vco1-Vin+Vco2}{\frac{Vin}{}}$ (21)

Where $M=\frac{3D+1}{1-D}$

Design equations of the proposed converter

Inductor

As we are analyzing in CCM,so the inductor values are obtained as

$I_L \geq \frac{\Delta Il}{2}$

$\Delta I_{L1}=\Delta I_{L2}=\Delta I_{L3}=\Delta I_{L4}=\frac{0.2VoIo}{Vin}=1.5A$

$L_1= L_2= L_3= L_4= \frac{Vin*D}{\Delta IL*Fs}=464\mu H$

Capacitor

As from the voltage equations of the capacitor V_{C1} –Vc4 (18 & 19) the capacitor equations are obtained.Since the charges observed by all the capacitors is equal :

$\Delta Q=\frac{Io*D}{\Delta Vc*Fs}$

$\Delta Vc=\frac{\Delta Q}{C}$

Based on ΔVc the capacitor value here we use 1% but in the base,the paper may vary upto 5%

$C_1= C_3=\frac{0.72*0.68}{0.75*30*10^3}=16\mu F$

$C_2= C_4=\frac{0.72*0.68}{1.04*30*10^3}=16\ \mu F$

$C_{01}= C_{02}=\frac{0.72*0.68}{1.68*30*10^3}=10\ \mu F$

IV.VOLTAGE STRESS

To select the proper ratings of the semiconductor devices the voltage stress of the converter is to be considered. Based on the operating principle of the proposed converter, the voltage stress on the switches and the diodes is :

$V_{ss}1=V_{ss}2=1/1\text{-}D\ V_{in}=29/1\text{-}0.72=103.5V$

$V_{SD(1\text{-}4)}= -1/1\text{-}D\ V_{in}=-29/1\text{-}0.72 =-103.5V$

V.COMPARISON STUDY

The proposed converter is compared with some previously developed converters in terms of voltage gain, the voltage stress on power switches, efficiency, cost, and size. The voltage stress of the proposed converter is less than the other previously developed converters for different values of the duty cycle which indeed increases the converter efficiency and hence cost of the converter is reduced. Also, the voltage conversion ration and the voltage gain of the converter are more than the previously developed converters due to the interleaving technique of two modified step-up KY converter which is proposed in this project. The numbers of switches used here are less compared to previously developed converters.

Table 1:Comparsion of the proposed converter with present converters

Parameters	Proposed Converter	Reference [1]	Reference [6]
Voltage gain	1+3D/1-D	n+1+(n+1)D/1-D	2(KN+1)/1-D
The voltage stress on switches	1/1-D V_{in}	M+n+1/2n+1	M+1/2M
Number of modes	2	4	8
Number of switches	2	1	2
Size	Small	complex	More complex
Efficiency	96.6	90.4	92.8

VI.SIMULATION RESULTS

Simulation is carried out in Matlab/Simulink software. The parameter value used in this simulation is given in the below table 1. The graphical representation of voltage, current for different components of the proposed converter is shown in fig 4& 5. The switch voltage is less than the output voltage which reduces the stress on the switches, so the switches with low on-state resistance can be used. The efficiency of the proposed converter is 96.6% fig 4(c). The input power is 231W with an input voltage and current 29V and 9A represented in fig 4and the output power obtained is 225W the output voltage and current are represented in fig 4.The gate pulses are of 1V and the switch voltage V_{sw} and current I_{sw} is 100V and 9A represented in fig 5. The inductor voltage and current are represented in fig 6. The capacitor voltage V_{C4} and V_{C2} are represented in fig 7.

Table II: Parameter Values Used in Simulation

Specifications	Values
Input voltage	29 V
Output voltage	329 V
Output power	225.5 Watt
Switching frequency	30 kHz
Load Resistance	480 Ω
Inductors	464μH(4)
Capacitors	22μF(2), 16μF(2), 100μF(2)

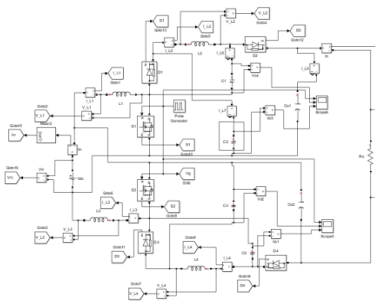
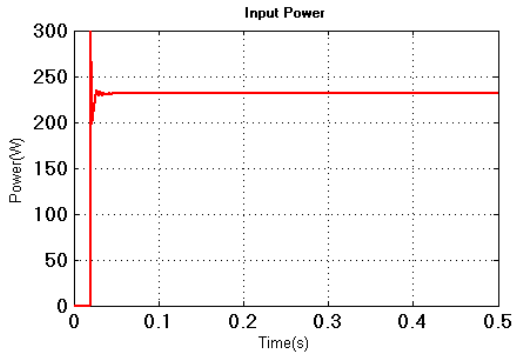


Fig 4: Simulation Diagram



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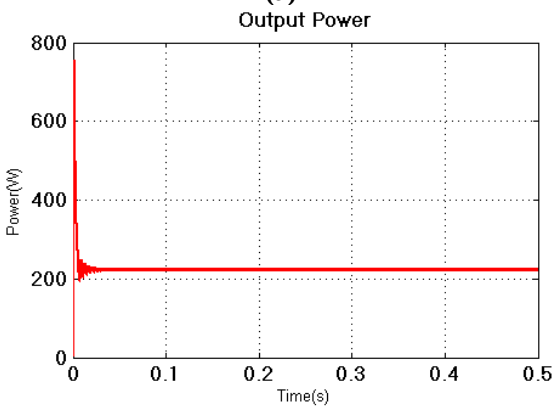

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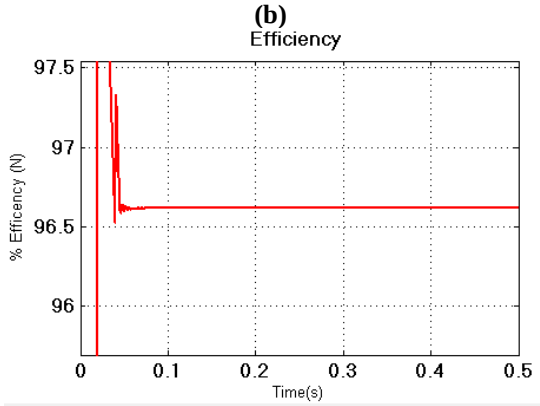

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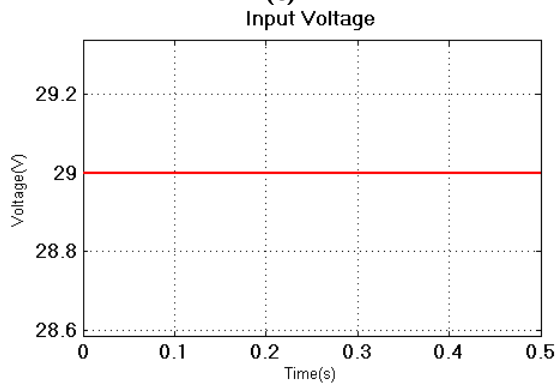

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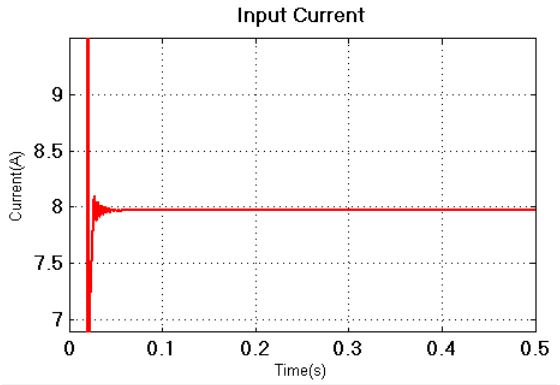

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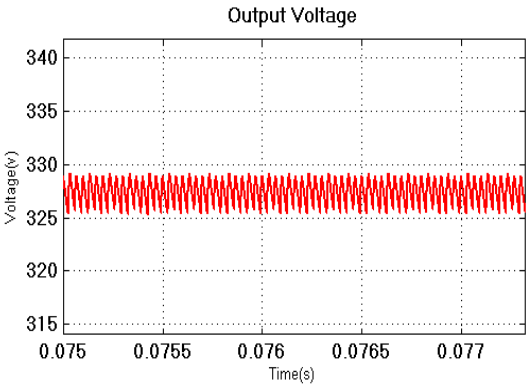
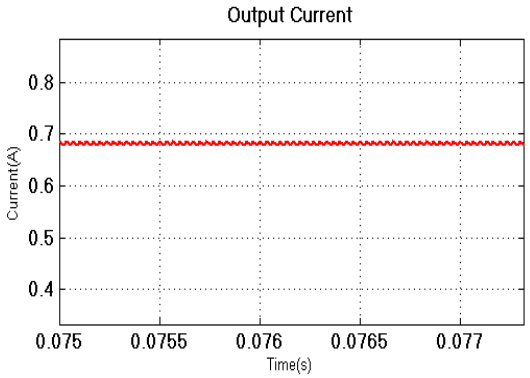
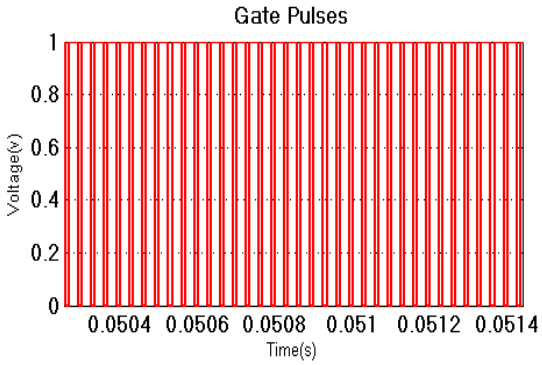


(f)



(g)

Fig 4. (a) Input power. (b) Output power. (c) Efficiency (d) input voltage. (e) input current (f) output voltage of the conveter (g) output current of the conveter



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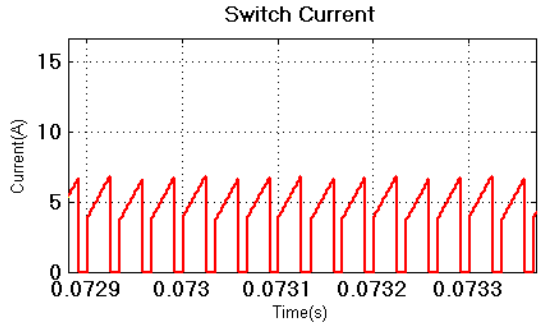

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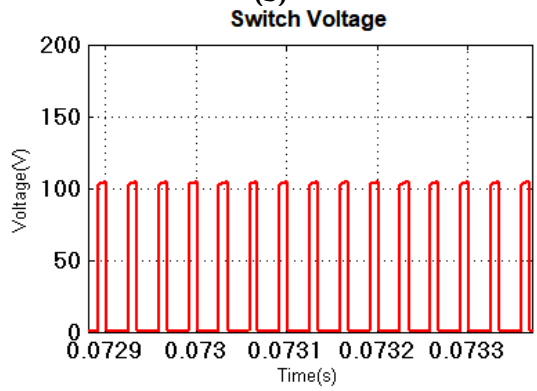

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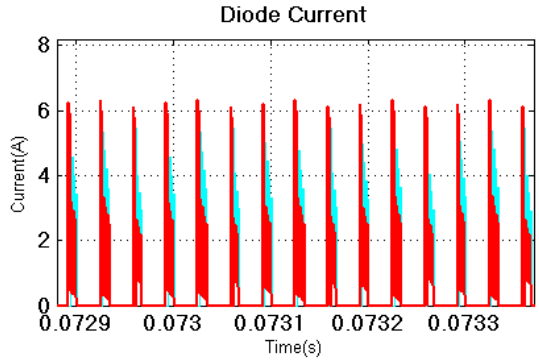

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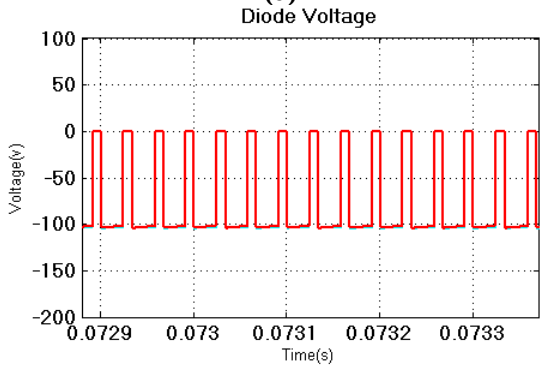
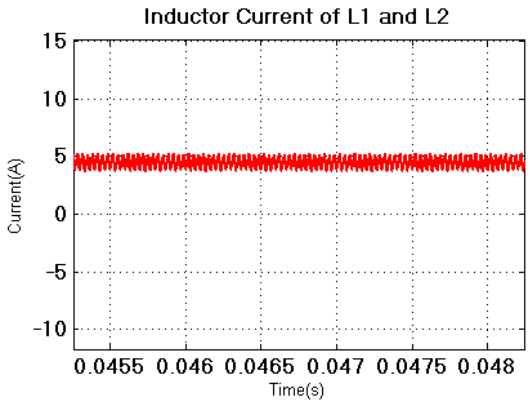


(e)

Fig 5. (a) gate pulses. (b) switch current. (c) switch voltage. (d) diode current.(e) diode voltage



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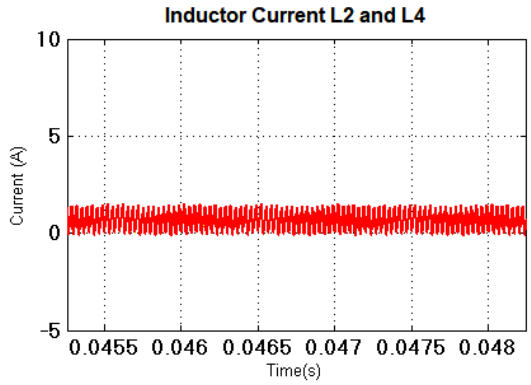

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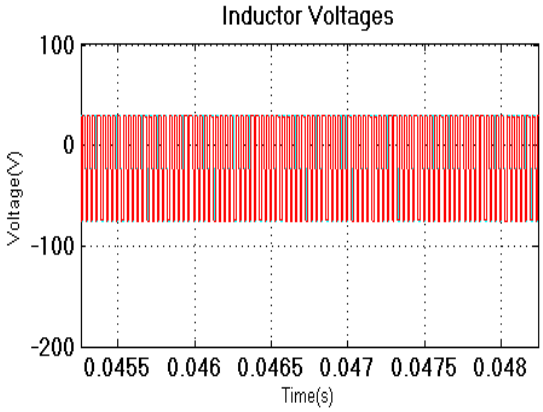

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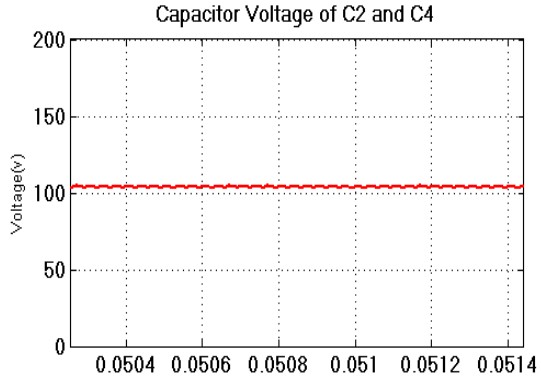

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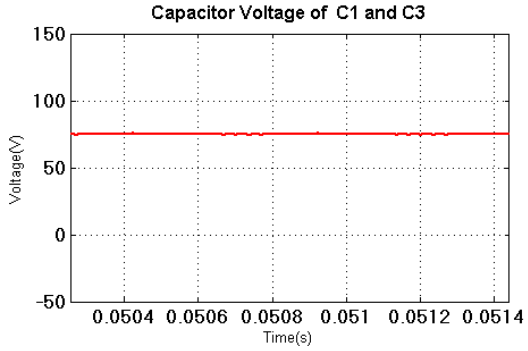

(e)

Fig 6. (a) inductor current of L_1 and L_3. (b) inductor current L_2 and L_4.(c) voltage of inductors.(d)Capacitor voltage of C2 and C4.(e)Capacitor voltage of C1 and C3

VII.CONCLUSION

This paper proposes a new step-up non-isolated interleaved KY dc-dc converter. The proposed converter consist of two switches with low on-state resistances as the voltage stress on the switches is less. The modified interleaved KY converter has high voltage gain compared to the previously developed/conventional converters and due to low ripple in the input current, this is suitable for the PV system also. There can be further enhanced by using a PV array. The converter was operated in CCM and all the semiconductor devices were analyzed in steady-state The accuracy of the proposed converter is estimated in MATLAB/SIMULINK software. The voltage conversion ratio and the voltage gain of the converter are 11.34 for the duty cycle of 72%, which is more than that of input voltage due to the interleaving technique of two modified step-up KY converter. The voltage stress of the interleaved KY converter is less.The input voltage given to the converter is 29V and the boosted output voltage obtained is 329V. The interleaved KY converter output power obtained is 225W for an input power of 230W. The efficiency of the proposed converter is 96.6%. The gate pulses are of 1V which are obtained from the pulse generator given to the switch, diode voltage is 100V which is 3.25 times less than that of load voltage. The performance of the interleaved KY converter was studied.

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