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Design and Analysis of Hybrid full adder Topology using Regular and Triplet Logic Design

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Abstract*: *In the recent era, voltage reduction procedure is gaining most attention for achieving minimum energy consumption. Full adder is the primary computational arithmetic block in numerous of the computing executions and hence is the critical component of ALU.Various existing full adders proposed in literature fail to accomplish low power delay product (PDP) and lacks driving strength when used in chainsstructure.In this paper two new hybrid full adders have been proposedwith an aim to achieve low PDP.Further the paper proposesripple carry adder (RCA) in chainstructure using triplet design approach to improve the driving strength. Fivedifferent hybrid full adders topologies have been implementedto build 4-bit RCA adder in regular and triplet logic design and PDP improvement is obtained in triplet design approach. All the simulations are done on 45nm technology and performance analysis done over the voltage range 0.6 V to 1.2V in Cadence Virtuoso simulation software. Simulation results are obtained to show that delay and PDP has improved in triplet designing and the proposed hybrid adders represents least PDP among other implemented reference circuits.

Keywords: hybrid full adder, power delay product, ripple carry adder, triplet design

I. INTRODUCTION

In VLSI chip design, power dissipation is an important performance parameter. As the device density increases, more transistors are being integrated onto a chip, which further prompt increment in power dissipation of the device [1]. Static Power dissipation is caused by the device internal leakage, when it is in OFF state [2]. Dynamic power dissipation is caused when charging and discharging of the output node capacitance of transistor takes place during the time of switching and results in high energy loss. Therefore, both the power dissipation has been the most important concern for the designers [3]. Since battery innovation has offered a restricted change, low power design procedures are basic for improved portable gadgets and devices [4]. The electronic devices demand for more speed and longest battery life. For arithmetic operations, ALU is used as processing element inside the device. Full adder is the primary architecture of ALU and hence improving the performance of full adder is an important point of concern [5-8]. High speed and low power full adder are essential in achieving high performance battery operated electronic devices. Many logic styles are used in designing full adders using GDI techniques previously [25]. In the dynamic logic style clock signals are given to the NMOS and PMOS transistor. This clock signal provides large loading and unnecessary switching in idle mode, which results in high leakage current [20]. Therefore, dynamic logic style designed full adder is not suitable for devices demanding longer battery life. In static logic style the output is strongly driven to either supply voltage or ground. Hence, they consume less power and suitable for battery conducted devices. The main aim of the hybrid design is to reduce the number of transistors in the adder cell thereby reducing the number of power dissipating nodes. PTL transistors XOR-XNOR techniques have been realize high-speed and high-performance hybrid XOR-XNOR full adders. The full adder circuits based on 4T XOR-XNOR functions have a simple structure and reduced power consumption. The N14T FA designs have overcome non swing problem prevailing in the reported designs at low voltage and subsequently improved the performance of the circuit. This design reduces propagation delay and area of digital circuits while maintaining low complexity.

A. Review on existing static full adders

The conventional full adder is the static complementary metal oxide semiconductor (C-CMOS) in which two networks is there of PMOS and NMOS that accounts for total 28 transistors [9]. The advantage of this adder is its toughness against voltage scaling. The drawback is due to large number transistors and high input capacitance which affects the circuit's performance when it is used in the chain structure. Pass transistor logic (PTL) based full adder uses a less number of transistor counts i.e. 6 [10]. This type of full adders dissipates low power, but the major drawback is threshold voltage drop and poor driving capability. Complementary pass transistor logic (CPL) style is another type of full adder that uses two mutually exclusive NMOS network. This logic style achieves high speed, full swing and good driving capability due to use of an inverter in the output. But the disadvantage with this style is a large number of transistors are used, i.e. 32 transistors, which results in high capacitance and large area [8]. The Transmission gate (TG) based full adder has proved to be better than conventional, PTL and CPL in terms of power consumption and speed.

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It removes the drawback of threshold voltage drop in PTL by using NMOS and PMOS transistors parallel to each other [27].They are more suitable for chain structure [11-12].

Hybrid full adders use the benefits of various logic styles and are designed to reduce the transistor count while maintaining the high performance of the circuit. Hence, the most suitable adder to be used in the chain structure for designing ALU architecture is a hybrid CMOS full adder which is used in the electronic devices to achieve high speed, low power and long battery lifespan [13-16]. When it comesto battery operated devices, then speed and power dissipation both are important concerns [21-23]. So, requirement in a full adder is high speed, low power dissipation, good driving strength and full voltage swing[24]. From the survey on existing full adders, TG and hybrid CMOS FA design styles are more suitable for battery operated devices in terms of low PDP.

This paper is organized in 5 sections. Section Idepict about the introduction to static full adders, their functioning and issues. Section II talks about the proposed hybrid full adders and selection of referencefull adderstopologies for comparison with the proposed full adders in terms of power,delay and PDP. Simulation results and comparative analysis of proposed hybrid adders with other reference adders topologies is shown in this section. Section III describes the regular and triplet logic designapproach used to design 4-bit RCA. This section also deals with issues in conventional RCA design and how it is resolved in triplet design. Section IV describes about the simulation results and comparative graphical representation of 4-bit RCA and section V is the final conclusion of the proposed work.

II. HYBRID FULL ADDER CIRCUITS TOPOLOGIES

In this section hybrid full adder architecture N17T and N14T are proposed. 4T XOR logic function is designed using four transistors as shown in Fig. 1 and subsequently, XNOR function can also be implemented using CMOS inverter.

Following Boolean equations are employed to generate XOR and XNOR signals are:

$$XOR = A\bar{B} + \bar{A}B \quad (2.1)$$

$$XOR = \overline{XNOR} \quad (2.2)$$

XOR and MUX logic circuits implemented have shown correct logic at all input logic conditions and schematic diagram as shown in Fig. 2 & Fig 3 respectively.

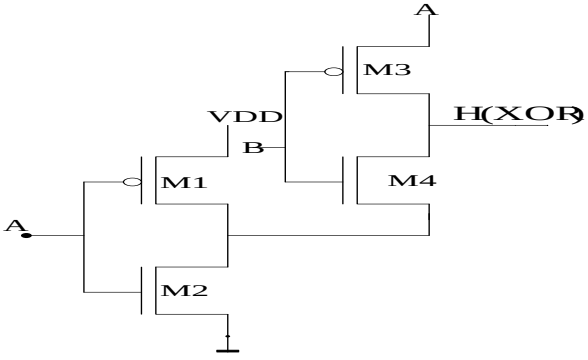

Fig.14T XOR logic circuit

The functionality of the full adder topology is based on the following Boolean equation:

$$Sum = \overline{Cin}(A \oplus B) + Cin(A \odot B) \quad (2.3)$$

$$Carry = \overline{(A \odot B)}Cin + (A \odot B)\,B \quad (2.4)$$

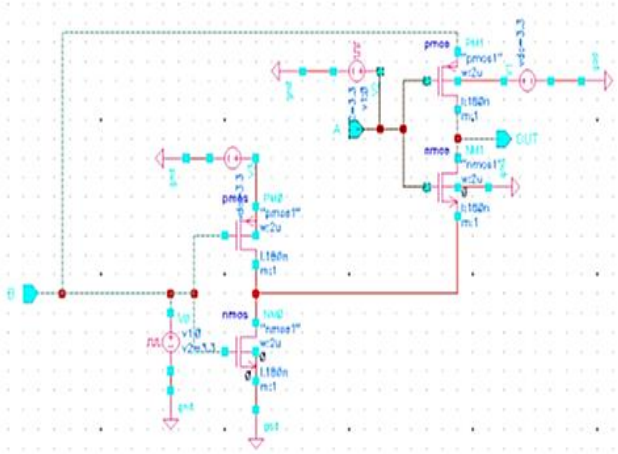

Fig. 2 Schematic diagram of4T XOR logic circuit

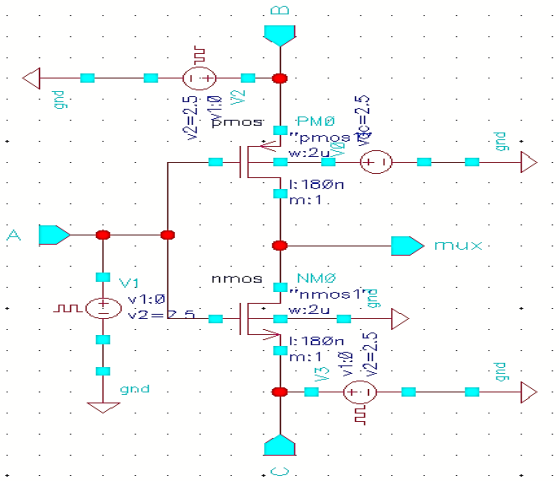

Fig. 3 Schematic diagram of 2T MUX logic circuit

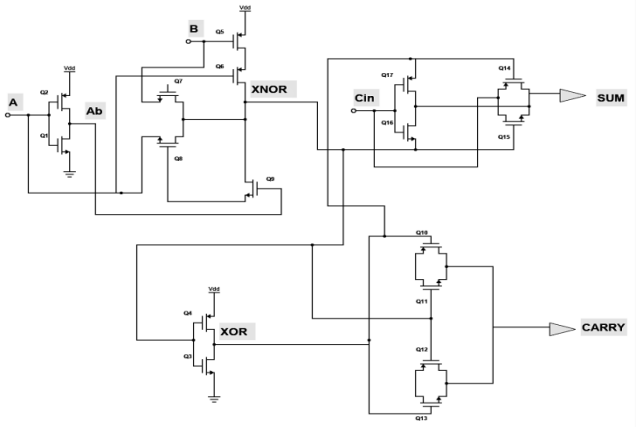

Fig. 4(a) N17T FA circuit

The first hybrid full adder is N17T FA. The N17T FA circuit consists of three stages and 17 transistors. On the first stage CMOS inverter is there that inverts the input A.

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The next stage uses low power XNOR circuit in which B input is applied. XOR is obtained by inverting XNOR in stage 2. Finally, at stage 3 GDI MUX produces output SUM while TG output produces COUT. The GDI MUX is connected with a TG for swing restoration. As we have studied GDI technique exhibit voltage drop, hence to restore it TG is attached at the output of GDI MUX.N17T FA circuit is shown in Fig. 4(a).

The second proposed full adder is N14T FA.In N14T FA circuit, fourteen transistors make a full adder in the form of cascaded output structure. The N14T FA is based on 4T-XOR function, CMOS inverter, TG and pass-transistor logic. In the N14T FA topology, XOR function is designed using four transistors as shown in fig. 1and subsequently, XNOR function can also be implemented using CMOS inverter. N14T FA circuit is shown in Fig. 4(b).

Two input 4T-XOR function H(A⊕B) is implemented with the four transistors (M1, M2, M3 and M4). Similarly, two input 4T-XNOR function is implemented by addition of CMOS inverter transistors (M5, M6) to the 4T XOR. The complementary outputs of the XOR and XNOR gates are used to control the transmission gate which together realizes a multiplexer circuit producing the Carry function. Aspect ratio of the inverter circuit must be high for high driving capabilities. The output logic of four transistor based XOR function followed by TG & PT based multiplexers are used to design Sum and Carry functions in the proposed full adder topology.

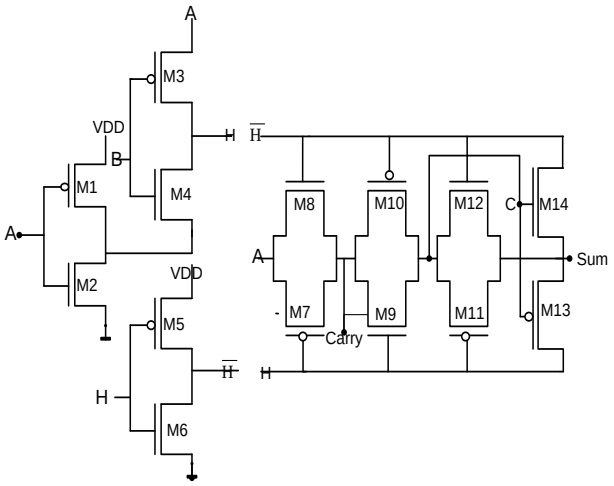

Fig. 4(b) N14T FA circuit

A. Simulation Results and Discussion of Hybrid Full Adder Topologies

For performance analysis of proposed hybrid full adders, three reference adders namely LPHS22T [17], LPHS18T [17], M19T [22] are simulated. The simulations of alladders'topologies are carried at 1V supply voltage in 45nm technology node. The simulation input-output waveforms of the proposed designsare shown in Fig.5(a) and Fig.5(b), that verify the digital logic operations of the adder circuit at all possible input logic combinations. The line chart shown in Fig. 6 to 8 compares the performance of the N17T and N14T proposed adders withother three references adders LPHS22T [17], LPHS18T [17], M19T [22] topologies. From the chart it may be inferred that the proposed N14T adders exhibit least power, it proves to be the best adder for implementing 4-bit RCA in regular and triplet approach.

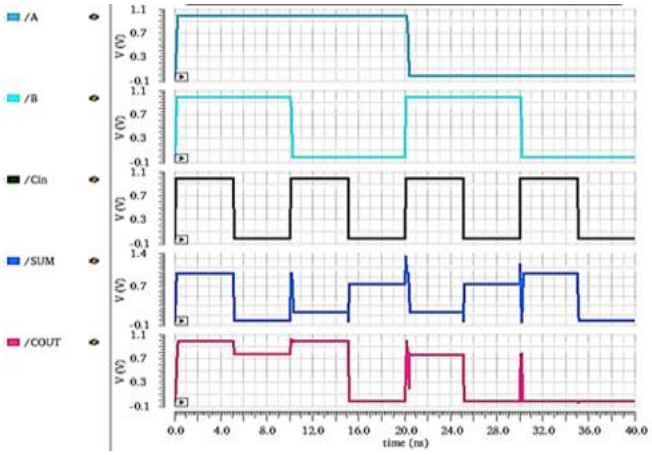

Fig. 5(a)Simulation input-output waveforms of the N17T FA V_{DD} = 1V

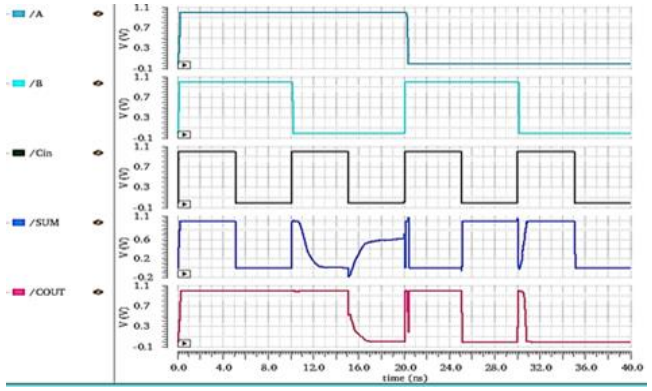

Fig. 5(b)Simulation input-output waveforms of the N14T FA V_{DD} = 1V

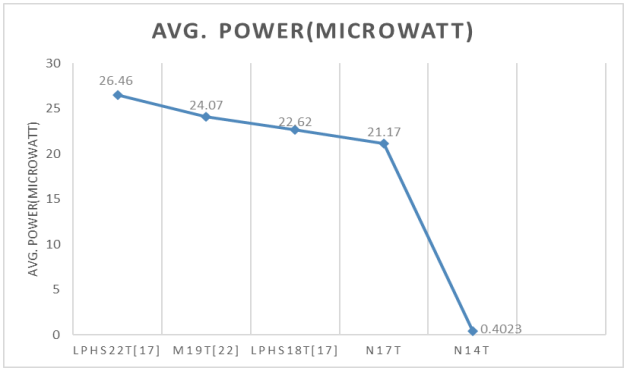

Fig. 6 Comparative Avg. power analysis of fiveadder topologies

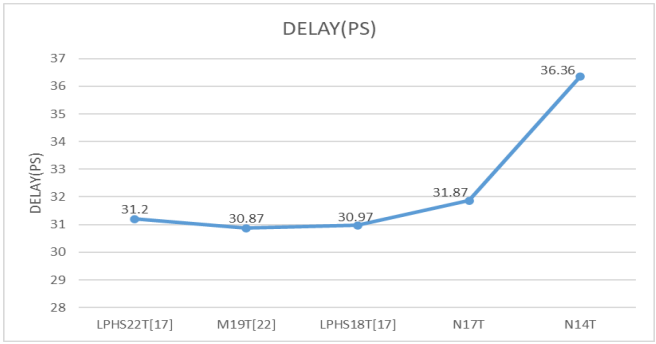

Fig. 7 Comparative delay analysis of fiveadder topologies

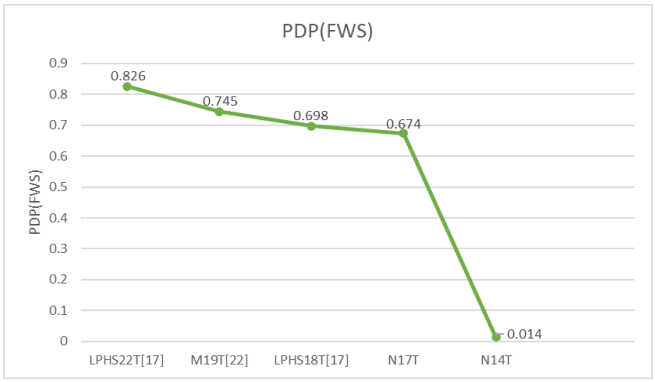

Fig. 8 Comparative PDP analysis of fiveadder topologies

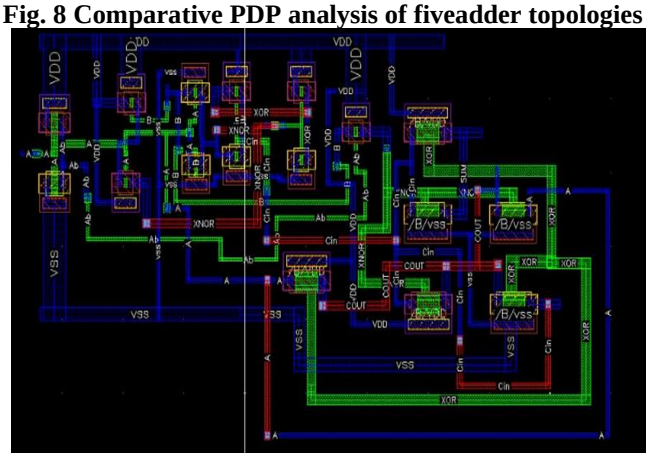

Fig.9(a) Layout of N17T adder

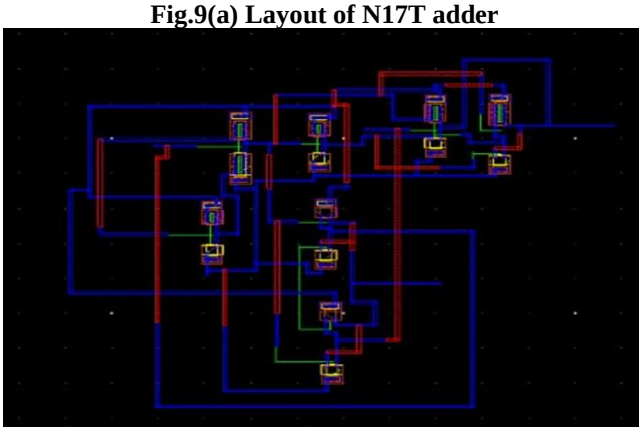

Fig.9(b) Layout of N14T adder

Out of the implemented five adders N14T adder has shown the least power dissipation of 0.4023µW. The simulation graph indicates that as transistors are decreasing, power is getting reduced. Hence transistor reduction not only decreases area, but also decreases average power. As the number of levels in a design increases, then delay gets increased. Here in N14T full adder we have 4 levels while in others we have 3 levels only. Hence delay of N14T is slightly more than the other adder topologies. Although the delay of the N14T adder is slightly more, but due to its very low average power, the overall PDP is lowest. The PDP of N14T is reduced to more than 90% compared to LPHS22T, LPHS18T and M19T adder topologies.Layout of the N17T and N14T hybrid full addersare designed in layout XL window in Cadence Virtuoso simulation software shown in Fig. 9(a) and Fig. 9(b) respectively.

III. REGULAR ANDTRIPLET LOGIC DESIGN APPROACH

Thetriplet design approach aims to improve the drive strength of adder by breaking the propagation path of input Cinthereby reducing loading problem.In this approach, we use the three different versions of the 1-bit full adder cell as presented in Fig. 10 [17].

- **Version 1**: It is basic adder where A, B and Cin act as input and Sum and Cout act as output.
- **Version 2**: It is an adder where A, B and Cin act as input and Sum and inverted Cout (Coutb) act as output.
- **Version 3**: It is an adder where A, B and inverted Cin (Cinb) act as input and Sum and Cout act as output.

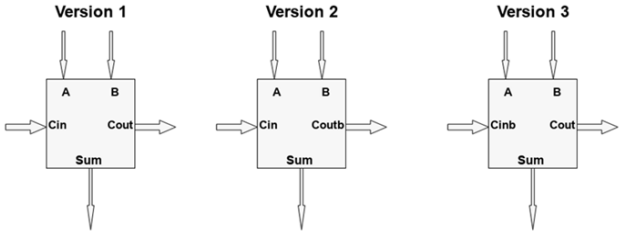

Fig. 10 Triplets FA design approaches [17]

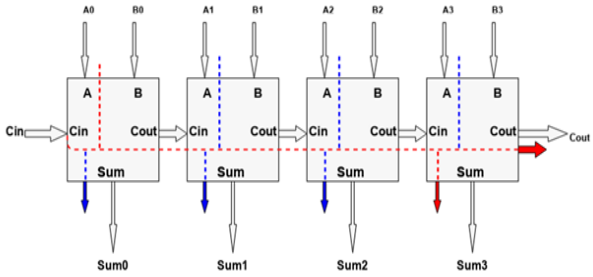

Fig. 11 4-bit RCA regular design [17]

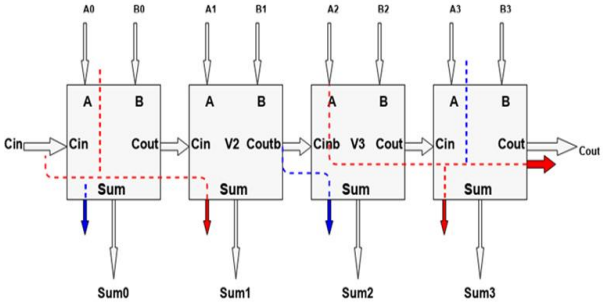

Fig. 124-bit RCA triplet design [17].

A. Conventional Ripple Carry Adder

The N-bit two operand adder is known as ripple carry adder (RCA). These are referred as chain structure. In the regular design approach, which is nothing but the conventional approach, the carry ripples from first (LSB) 1-bit full adder to last one (MSB). Hence there is a large loading on LSB input so that there is an increase in delay and PDP results. The Fig.11 depicts a basic flow diagram of 4-bit RCA in regular approach. Here the red dotted line shows the worst propagation path which is the possible longest path over which the input C0 travels to provide sum and carry at the output stage that results in large loading on the carry. While the blue dotted line shows the intermediate propagation path.

The worst propagation path starts from first adder cell till last which results in large loading on LSB input i.e. C0.

B. Triplet design of Ripple Carry Adder

Triplet logic design approach based 4-bit RCA drawn shown in Fig.12. Here, the first and fourth block of the adder are basic adders as discussed in Version1, whereas second and third block are Version 2 and Version 3 respectively. From figure, we notice that the longest critical path that is the red dotted line is reduced to only two stages unlike the regular where the critical path goes through all stages. The propagation path is cut because of the inverted carry output of version 2 adder at the second stage that results in independency of carry output of second stage on C0 and hence critical path reduces to only two stages. This reduces the loading problem and improves the driving strength of the adder without any additional buffer requirement.

IV. SIMULATION OF 4-BIT RCA HYBRID FULL ADDER TOPOLOGIES

For simulating 4-bit RCA first we have created individual blocks of the five adders and then cascaded in series to make it ripple carry adder. The schematic block diagram of regular (conventional) and triplet design 4-bit RCA by all 5adderstopology are shown in Fig. 13(a) and Fig.13(b) respectively.

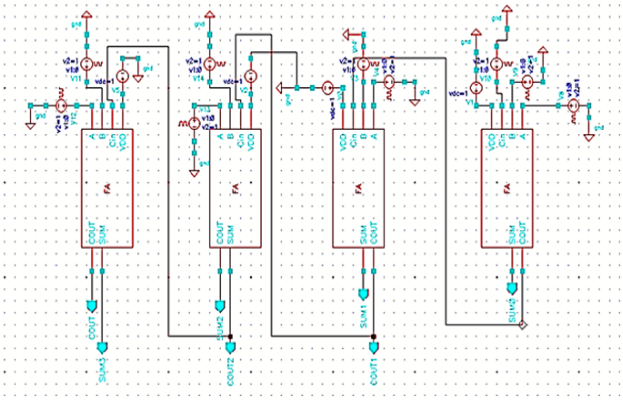

Fig. 13(a) Schematic diagram of 4-bit RCA regular design

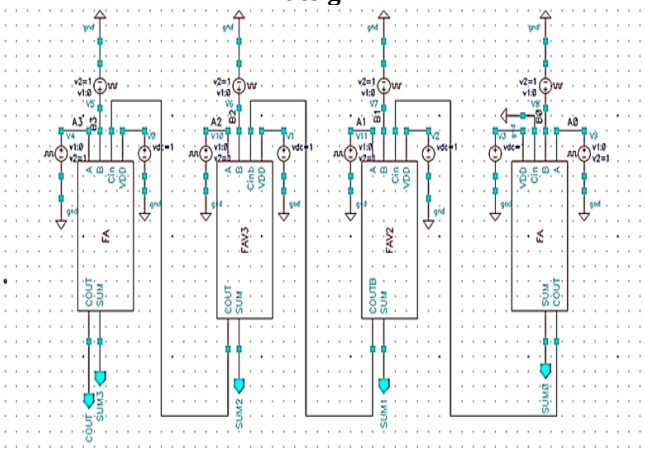

Fig. 13(b) Schematic diagram of proposed 4-bit RCA triplet design

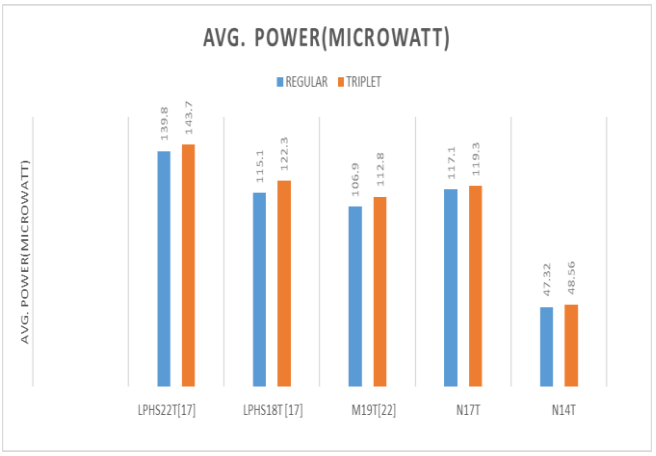

Fig. 14.Avg. Power of regular and triplet design 4-bit RCAFulladder topologies

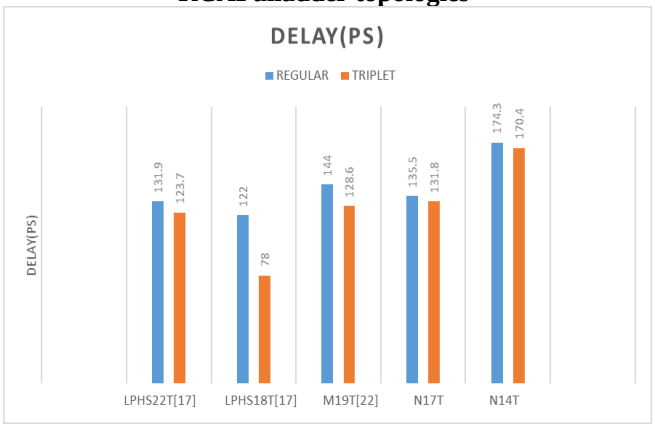

Fig. 15. Delay of regular and triplet design 4-bit RCA Fulladder topologies

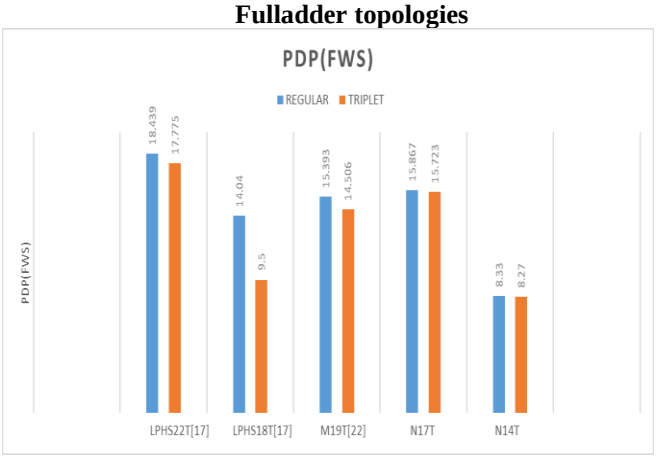

Fig.16. PDP of regular and triplet design 4-bit RCA Fulladdertopologies

A. Comparison of proposed 4-bit RCA Regular and Triplet Design

Circuits are design and simulated at T=27^{0}C and frequency=200MHz at 1V supply voltage. Performance parameters as Power, delay and PDP are analysed. The power dissipation slightly increases in triplet approach compared to regular design approach due to use of inverted Cin and Cout at the input and output of carry signal respectively. Out of all adder topologies N14T adder has shown least power in regular as well as in triplet design. The simulation comparative graph analysis shows delay is decreasing in triplet approach.

Hence triplet approach is highly efficient in designing RCA using TG MUX at the output. From delay analysis the M19T is showing least delay in regular approach also. But if we look at PDP of all FA topologies, N14T has shown least PDP. These simulation results are listed in table I and pictorially presentedin Fig.14, Fig.15 and Fig.16.

B. Simulation and Result Analysis of 4- bit RCA in Regular and Triplet Design Topology

An extensive simulation performance analysis hasbeen performed on Cadence environment using 45nm technology to evaluate the Sum (XOR-XNOR) function based full addertopologies. The **4-bit RCA Triplet (TP)** topologies based on hybrid-CMOS design styles with pass-transistor are presented here to achieve low PDP. The performance parameters viz propagation delay, power dissipation, PDP, voltage driving capability and layout area of the N14T full adder topology has been evaluated and compared with the reported design full adder topologies. The simulation results show that the performance of the **4-bit RCA Triplet** proposed designs is superior to the reported design of full adder circuits under different supply voltage conditions. Consequently, the **4-bit RCA Triplet** proposed topologies are appropriate for the realization of low-power high-performance VLSI design applications.

4-bit RCA is analysed in both the regular and triplet designs at 0.6, 0.8, 1 and 1.2 voltages using the adders topologies. The power, delay and PDP performance parameters are compared with previous adder circuits. These simulation results are listed in table II, III and IV respectively.

Table- I: Performance comparisons of 4-bit RCA in Regular (RG) and Triplet (TP) designtopologies at 1V.

NAME	LPHS22T [17]		LPHS18T [17]		M19T [22]		N17T		N14T	
	RG	TP	RG	TP	RG	TP	RG	TP	RG	TP
Average Power (µW)	139.8	143.7	115.1	122.3	47.82	48.56	117.1	119.3	47.82	48.56
Delay (ps)	131.9	121.7	112	78	174.3	170.4	135.5	131.8	174.3	170.4
PDP (fws)	18.439	17.775	14.04	9.5	15.393	14.506	15.867	15.723	8.33	8.27

Table- II: Power dissipation (µW) comparisons of 4-bit RCA in Regular (RG) and Triplet (TP) designtopologies for different set of supply voltages (0.6V-1.2V)

VOLTAGE(V)	LPHS22T [17]		LPHS18T [17]		M19T [22]		N17T		N14T	
	RG	TP	RG	TP	RG	TP	RG	TP	RG	TP
0.6	0.75	0.855	0.671	0.708	0.546	0.576	0.378	0.529	0.382	0.5
0.8	16.13	16.93	13.1	13.41	7.582	7.93	6.625	6.965	0.719	1.09
1.0	68.35	68.35	52.3	52.11	29.75	30.55	28.44	29.73	1.28	1.68
1.2	165.4	169.6	130.7	133.2	74.61	78.18	66.36	69.89	2.046	2.6

Table- III: Delay (ps) comparisons of 4-bit RCA in Regular (RG) and Triplet (TP) designtopologies for different set of supply voltages (0.6V-1.2V)

VOLTAGE(V)	LPHS22T [17]		LPHS18T [17]		M19T [22]		N17T		N14T	
	RG	TP	RG	TP	RG	TP	RG	TP	RG	TP
0.6	1688	25.32	736.6	22.74	25.48	22.71	27.09	20.56	349.9	101.1
0.8	723.2	19.11	360.6	19.71	26.53	19.67	19.22	18.39	152.2	38.11
1.0	476.1	13.62	212	13.92	13.71	13.11	13.3	12.66	121.1	25.65
1.2	417.1	10.57	106.6	10.89	9.739	8.36	9.871	8.969	82.2	20.2

Table- IV: PDP (fWs) comparisons of 4-bit RCA in Regular (RG) and Triplet (TP) designtopologies for different set of supply voltages (0.6V-1.2V)

VOLTAGE(V)	LPHS22T [17]		LPHS18T [17]		M19T [22]		N17T		N14T	
	RG	TP	RG	TP	RG	TP	RG	TP	RG	TP
0.6	1.266	0.021	0.494	0.016	0.014	0.013	0.01	0.01	0.1	0.05
0.8	11.675	0.323	4.723	0.264	0.201	0.155	0.13	0.13	0.109	0.04
1.0	32.54	0.93	11.08	0.725	0.407	0.4	0.378	0.376	0.155	0.053
1.2	68.996	1.792	13.932	1.45	0.726	0.653	0.655	0.626	0.168	0.052

V.CONCLUSION

In this paper hybrid full adderstopologies has been proposed for high speed and low power VLSI application. The proposed N14T adder has shown the best performance in terms of lowest PDP compared to its counterparts. There is a significant power reduction in the proposed adder circuits without affecting the other parameters. This is the plus point of using the hybrid design style technique, which reduces the power dissipation to great extent thereby improving the PDP. Thus, a pathway is created to use the hybrid low power techniques in other computational devices where power reduction is main requirement in nanotechnology application. 4-bit RCA hybrid full adders has been designed by regular design and triplet design approach using all five adders topologies and have been analyzed at from supply voltage V_{DD} 0.6 to 1.2V. From the simulation results analysis of 4-bit RCA, we see that N17T and N14T adder has shown least power and PDP from the other implemented reference circuits. The simulation results reveal that the Triplet logic approach design topology has topology has successfully improved the performance of RCA by breaking the propagation path in the chain structures. This design approach improves the drive strength of full adder and hence eliminates the requirement of buffers. This design achieves low PDP in all the cases compared to regular design making it very suitable to utilize it in battery operated devices.

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