Design of Test Pattern Generator for Testing Crosstalk Faults in TSVs

K. Praveen Kumar Reddy, P. Rangarajan

Abstract: ***Design of Test pattern generator to test crosstalk faults in Through Silicon Vias (TSV) in three dimensional integrated circuits presented in this paper. A well-known test pattern generation model for testing crosstalk called as Maximum aggressor fault model is adopted in the design. The finite state machine diagram for design of TPG presented in reference [1] is modified and the complete design of TPG is discussed in this paper. Verilog HDL Simulation and synthesis results of the proposed Test pattern generator is discussed.***

Keywords: crosstalk, through silicon via, Test pattern generation. Maximum aggressor fault model.

I. INTRODUCTION

Three-dimensional integrated circuit is one of the promising Network on chip technology which uses Vertical interconnects called as Through silicon via, which passes through different layers of silicon in the 3-dimensional network on chip technology and acts as the communication medium between the stacked layers. Due to the minimized pitch distance between them, TSVs are subjected to capacitive coupling and crosstalk[5] which is un avoidable. Though optimal distance is maintained between TSVs, post silicon validation and testing of this crosstalk talk faults is essential [3][4]. Different Built in self-test techniques are proposed to test crosstalk [1][2]. In this paper state machine model of TPG proposed in [1] is modified and complete design of TPG is discussed.

It's a well-known fact that crosstalk between interconnects (either horizontal interconnects on the die or vertical interconnects connecting different dies in 3 dimensional ICs) causes positive or negative glitches when one interconnect is in stable logic 1 or 0, and the neighbour interconnect is switching from 0 to 1 or 1to 0. The neighbour interconnect is called as aggressor and the one which is affected is called as victim. It also causes rise time and fall time delays of the victim signal when both interconnects are switching in opposite directions, also speed up or earlier arrivals of rising or falling signal on the victim when both victim and aggressor interconnects are transitioning in the same directions. These effects cause malfunctioning of the connected circuits in the next stage, as they cause a wrong signal other than expected one.

To test these cross-talk faults on interconnects, different test patterns making respective transitions on aggressor and victims needed to apply and observe any change in the expected or sent signal on victim.

A well-known test pattern generation method called as Maximum aggressor crosstalk model is used to test these faults [1], where two simultaneous test patterns with different types of possible transitions are applied to the victim and aggressor interconnect test the crosstalk effects. The test pattern transitions to be applied to victim and aggressor is summarised in table1.

Table.1. Patterns to apply for sensitizing cross talk

Present		Next		Fault sensitized
V	A	V+	A+	
0	0	0	1	Positive glitch on victim logic'0'
0	1	1	0	Victim rise time delay
1	0	1	1	Positive glitch on victim logic '1'
1	1	0	0	Speed up of victim fall time
0	0	1	1	Speed up of victim rise time
1	1	1	0	Negative glitch on victim logic '1'
1	0	0	1	Victim fall time delay
0	1	0	0	Negative glitch on victim logic '0'

II. DESIGN OF TEST PATTERN GENERATOR (TPG)

The design of automatic test pattern generator to generate these test patterns by using finite state machine is discussed in this section. Proposed design modifies the state machine given in [1].This state machine proposed in [1] is reproduced here in fig.1 for better understanding.

Revised Manuscript Received on 14 November, 2019.
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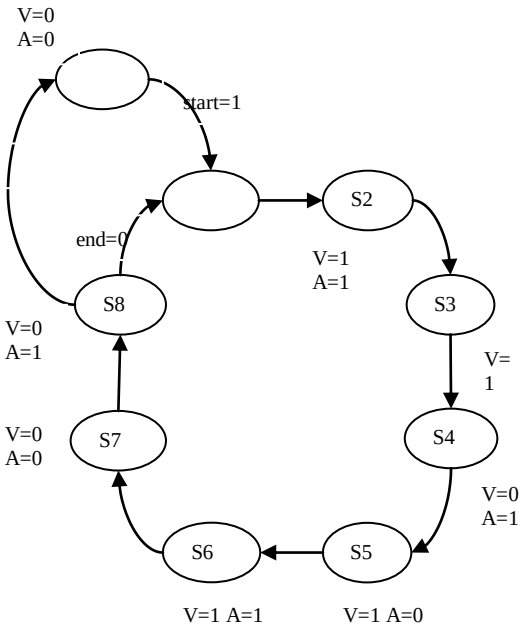

Fig.1. finite state machine proposed in[1]

From the state machine shown in fig.1 it can be observed that there are states transitions S1 to S2 and S7 to S8 i.e. from 00 -> 11 and 00 -> 01. S1 and S7 represents the same state of '00' and can be replaced by S1.To differentiate these two transitions,

An extra input 'X' is added. When X=0 the state transition S1 to S2occurs and when X=1 state transition S1 to S8.Similar transitions are observed for other states.

By Re-structuring the state diagram in fig.1 can be reduced to only four states S1, S2, S3,S4 representing '00', '01', '10', '11' respectively. Required eight transitions to sensitize the crosstalk faults can be obtained by using these four states and with an input X to differentiate the two sets sequences.

When X=0 the sequence 1 is S1->S2->S3->S4->S1

i.e. 00-> 01->10->11->00

When X=1 the sequence 2 is S1->S4->S3->S2->S1

i.e. 00->11->10->01->00

Output signal 'Z' is included to indicate the completion of sequence. The FSM starts with input X= 0 and completes the sequence 1. The output Z becomes 1 after four clock pulses indicating the completion of sequence 1. (Illustrated in fig.2)

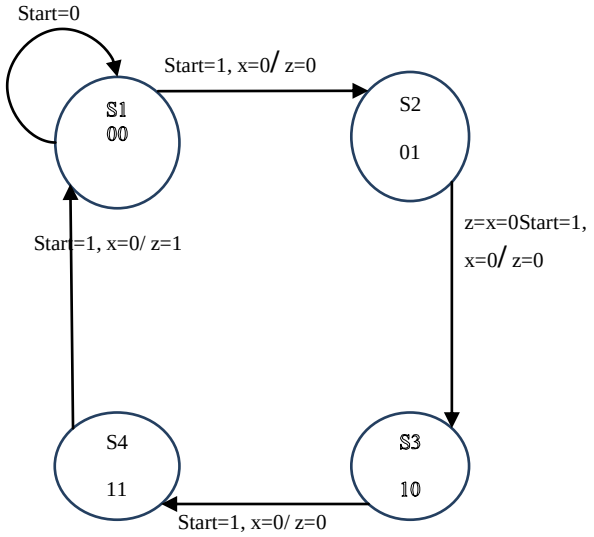

Fig.2. sequence 1 with input X=0

The second sequence starts by activating input X with logic '1' and goes around the sequence 2. Output Z becomes logic '0' after completion of second sequence.

The input X needs to be changed from '0' to '1' or vice versa after completion of each set of four states. This is done by connecting the output signal Z as a feedback to input signal X. After each four clock cycles i.e. after completion of producing a set of sequence the output Z toggles between '0' and '1' and it is connected as a feed back to input to X, which provides and automatic changeover of input X from '0' to '1' or '1' to '0'.

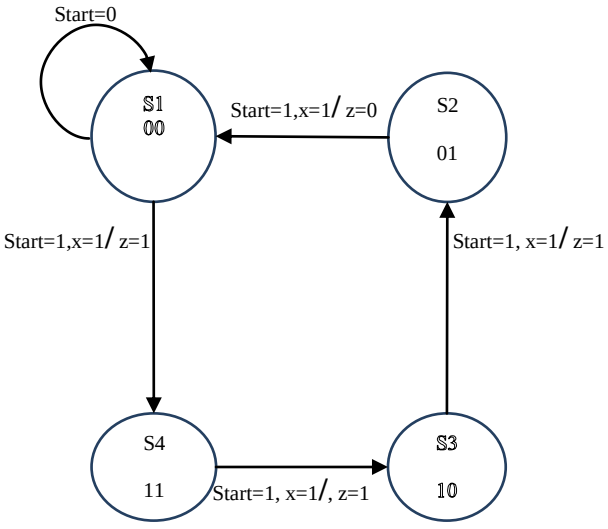

Fig.3. sequence 2 with input X=1

Design of Proposed Test pattern generator:

The block diagram and state transition diagram of the proposed FSM is shown in fig.4 and fig.5 respectively.

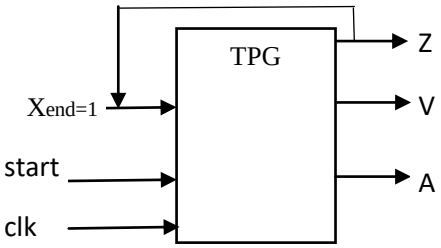

Fig.4. block diagram of proposed TPG

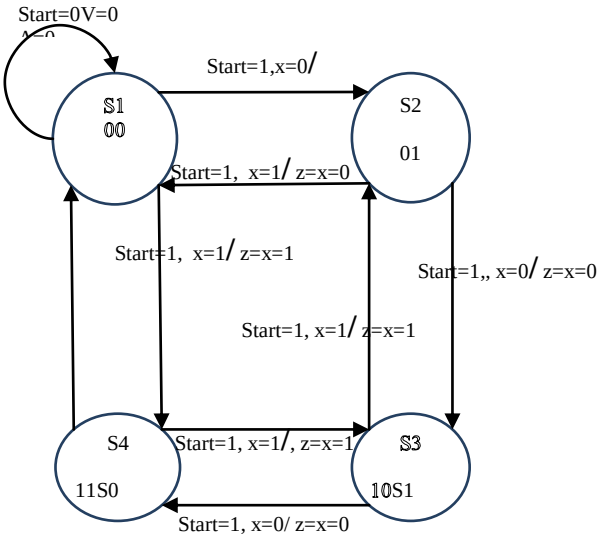

Fig.5. proposed FSM for TPG

The test pattern generator has two inputs Start, X(to select the test set) and three outputs V (victim) A (aggressor) and Z (which is connected back as feedback to input X). The output Z toggles from '0' to '1' or '1' to '0' to switch input X from set '0' to set '1' or vice versa. the TPG will start generating the test patterns once start='1' signal is assigned and generates the two sets of tests patterns and finally comes back to start='0' condition. The TPG is designed to automatically change from set'0' to set'1' by giving a feedback to input X from the output Z.

Table.2. state table of the state machine in fig.4.

	Start=1					
Present	Next state Output		inputs		Output	
	x=0	x=1	x=0	x=1	x=0	x=1
V A	V+ A+	V+ A+	D1 D2	D1 D2	Z	Z
00	01	11	01	11	0	1
01	10	00	10	00	0	1
10	11	01	11	01	0	1
11	00	10	00	10	1	0

$$D1 = X'(V'A+VA') + X(V'A'+VA)$$

$$= X \oplus A \oplus V$$

$$D2 = X'(V'A'+VA') + X(V'A' + VA')$$

$$= X'A'+ XA' \quad = A'$$

$$Z = X' VA + X(V'A' + V'A + V A')$$

$$= V(X \oplus A) + XV'$$

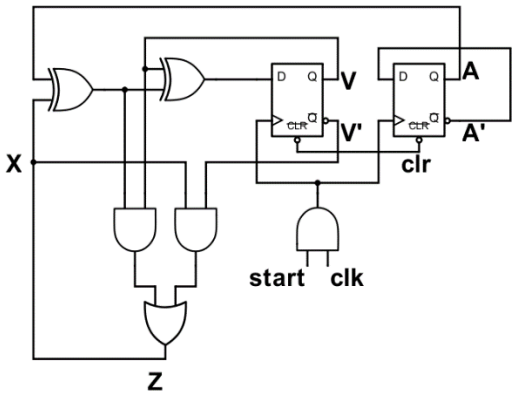

Fig.6 Circuit schematic diagram of proposed TPG

The sequential circuit design is done byconventional method of state tables as given in table.2. As there are four states only in the proposed design, only two D-flip flops are required for the design. The Boolean equations for the two inputs derived fromthe given state table, and the logic circuit is designed as shown in fig.6.

SIMULATION RESULTS:

The proposed circuit was simulated by using Mentor graphics ModelSim simulator and was synthesized with Xilinx ISE Synthesis tool. The simulation results are shown in fig.7 and fig.8 respectively

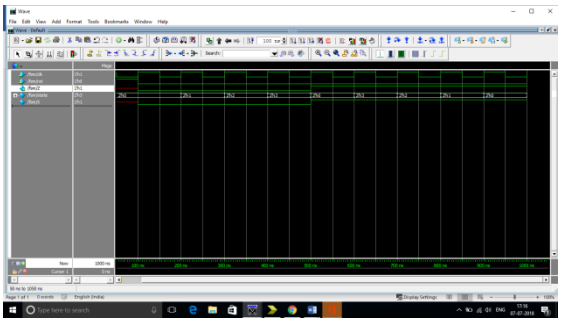

Fig.7. simulated output waveform

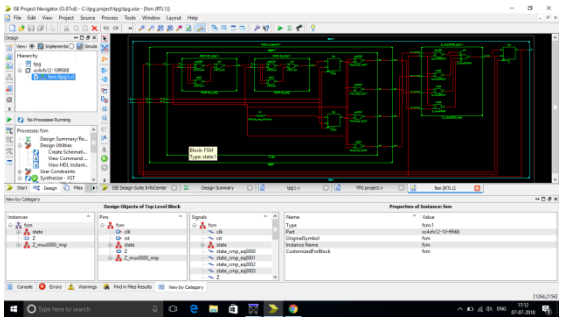

Fig.8.Synthesized circuit from Xilinx ISE

CONCLUSION & FUTURE WORK

The proposed Test pattern generator can be used in the BIST implementation for testing crosstalk faults in TSVs of 3DICs. Test access mechanisms to access the BIST controller to activate the TPG and to receive the test responses for analysis are needed to be developed which should be compatible with the IEEE P1838 and 1149.1 JTAG standards.

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