Design of a Single Phase H- Bridge Cascaded Multi Level Inverter (9 Level) for Solar Powered Utilities

P. Sathyanathan, P. Usha Rani

Abstract: Nine level inverter and converter which is used for solar powered utilities was proposed. The inverter has 7 switches in main circuit and 1 switch for high frequency switching for the generation of nine level output. The output in the inverter reduces overall THD, loss due to switching and improves the efficiency of the power in the output. In this paper the control circuit is simplified by using capacitors to balance the voltage automatically. Using MATLAB/Simulink simulation results are explained in detail.

Keywords: Converter, multilevel inverter, solar powered utilities and MATLAB/Simulink.

I. INTRODUCTION

In Multilevel inverter there are 3 types

- 1. Flying capacitor
- 2. Diode clamped and
- 3. Cascaded.

In first two types of multilevel inverter capacitor is used to build step voltage but not easy in capacitor voltage control. Power and output of voltage can be increase with increase in levels. For the proposed 9 level inverter there are 14 power electronic switches in both first two types but in cascaded type only 7 main switches are used. However in recent years, there are different type of techniques are used to develop a 9 level inverter. The switching devices in the multilevel inverter do not have any voltage shared in the circuit problems. Thus it has more advantages and the major application of this types are in large motor drives and utilities.

II. PROPOSED CIRCUIT CONFIGURATION & MODES OF OPERATION

The proposed multi level inverter with power converter shows in the configuration of Fig 1.

A solar cell utility is connected to power converter which transforms the power in the output into two voltage sources supplies to the inverter and the power converter which is a boost converter connected with a transformer turns ratio of 2:1. The proposed inverter consists of full bridge

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converter and the capacitor are in cascaded, the capacitor selection in the circuit which give four level DC output and the bridge converter convert this four level DC output to nine level AC output.

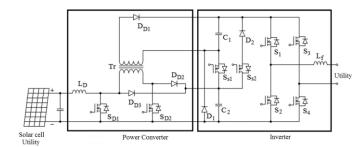


Fig 1. Multi Level Inverter with Power Converter

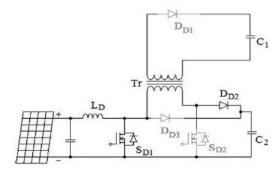


Fig 2a. Operation of Power Converter (S_{D1} is ON)

. A power converter combines current fed converter with a boost converter shows in the Fig 2a.

It consists of a diode, a inductor, a switch which charges C_2 & capacitor C_1 is charged by the current fed converter consists of diode, inductor, transformer and the switches.

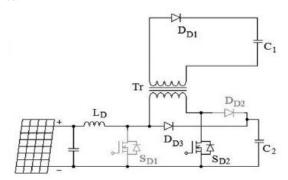


Fig 2b. Operation of Power Converter $(S_{D1} ext{ is OFF})$



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From the Fig 2b. when the switch S_{D1} is OFF position and S_{D2} ON position, the C_1 , C_2 capacitors are in parallel to the transformer, therefore energy in the inductor flows in the capacitor through diode D_{D3} and charge capacitor C_1 through the transformer and diode D_{D1} in the off state of switch S_{D1} . The capacitor voltage ratio C_1 : C_2 is same as that of the turn ratio 2:1 of the transformer because capacitors are charged with the help of transformer in parallel. The boost converter in the circuit which the conduction is continuous mode of operation.

Voltage in the capacitor C₂ is,

= Vs

And C₁ is,

= V_{s}

The working of 9 level inverter is splitted into positive half cycle & negative half cycle. In analyzing, the ideal switches in the circuit and the diodes, C_1 , C_2 constant which is equal to Vdc/4, Vdc/2, output is sinusoidal controlled and in phase voltage, the output current obtained in the 9 level inverter is also positive in first half cycle.

The working principle of the 9 level inverter in the first half cycle is divided into following modes in Fig3.

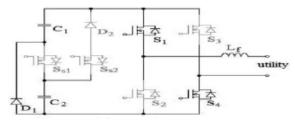


Fig 3a. Mode 1

Mode 1: Working principle is Switches S_{s1} and S_{s2} OFF, output is Vdc/4. S_1 and S_4 ON, then the voltage in the output of the inverter is Vdc/4.

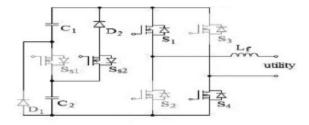


Fig 3b. Mode 2

Mode 2: S_{s1} is OFF and S_{s2} ON, the output is 3Vdc/4. S_1 and S_4 ON, then the output is 3Vdc/4.

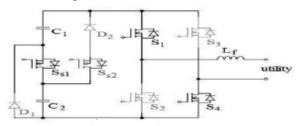


Fig 3c. Mode 3

Mode 3: D_2 reverse bias so S_{s1} is ON and S_{s2} either ON or OFF because the S_{s2} state cannot disturbs flow of the current, C_1 , C_2 is discharged is series in the circuit output is Vdc/2. S_1 and S_4 ON, output is Vdc/2.

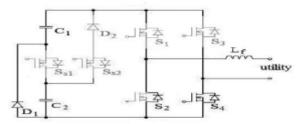


Fig 3d. Mode 4

Mode 4: S_{s1} and S_{s2} OFF, the output is Vdc. S_4 ON, the inverter output current is positive S_2 to switch ON forcibly for continuous conduction of filter with inductor current.

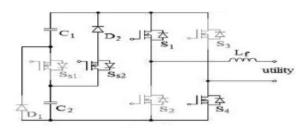


Fig 3e. Mode 5

Mode 5: S_{s1} and S_{s2} OFF, the output is Zero.

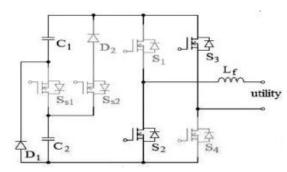


Fig 4a. Mode 6

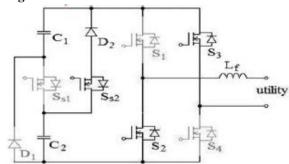


Fig 4b. Mode 7



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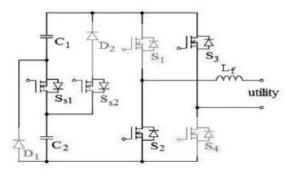


Fig 4c. Mode 8

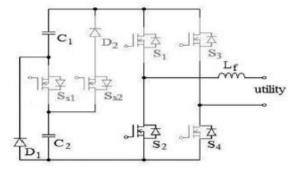


Fig 4d. Mode 9

Inverter another half cycle, the current obtained in the output is also negative. It is divided into the above modes and it is shown in the Fig 4. Compared with positive cycle, the negative cycle has the difference is Switch S_2 and S_3 ON during 5, 6, 7, 8 modes and S2 may ON or OFF during mode 9 of negative half cycle.

III. SIMULATION CIRCUITS AND RESULTS

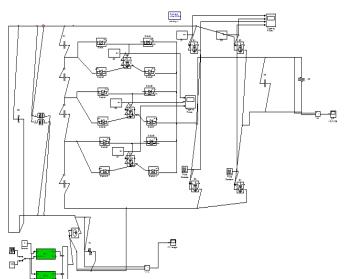


Fig 5a. MATLAB 9 level simulation circuit

MATLAB software is used for simulation to analyze and to verify the circuit operation, characteristics of the proposed system,. The Fig5a. shows the circuit diagram for nine level inverter consists of seven main switches and four balancing capacitors to balance the output of nine level.

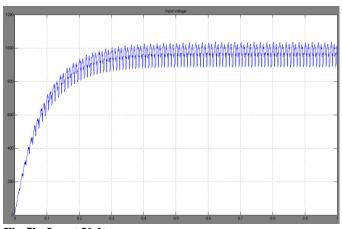


Fig 5b. Input Voltage

The voltage given as input is from the solar power closed loop irradiance level and the output is then to the inverter.

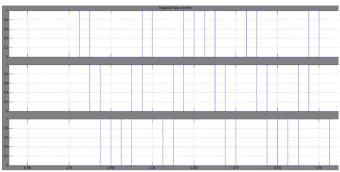


Fig 5c. Input Pulses (converter side)

It is generated for 20ms period by the pulse generating circuit and the phase delay is different for each switches to operate.

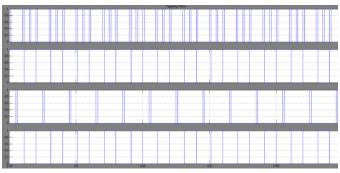


Fig 5d. Input pulses (inverter side)

It is generated for 20ms period by the pulse generating circuit and phase delay is different to obtain output of 9 level.



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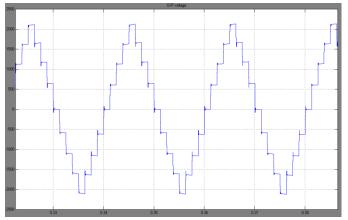


Fig 5e. Output 9 level Inverter voltage waveform

Fig5e. is the output of 9 level inverter (ie) Voltage waveform

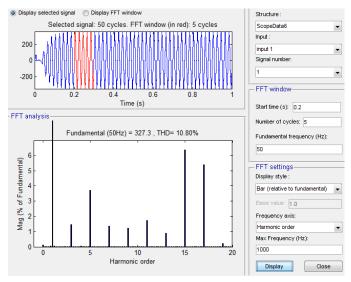


Fig 5f. THD Analysis of Nine level Inverter

Fig5f. THD analysis of 1\phi 9 level inverter where the THD level in the **9 level inverter is 10.80%**.

IV. CONCLUSION

The proposed inverter system consists of power converter with 9 level inverter. The existing 7 level inverter contains 6 switches and the 9 level inverter contains only 7 switch to create the stepped ac sinusoidal output waveform. The proposed inverter has reduced number of balancing capacitors to balance the voltage automatically. Simulation results in the proposed inverter generates the output of nine level and the output voltage, output current are in phase with voltage utility and also the THD reduces when increase in the number of levels.

REFERENCE

- R. A. Mastromauro, M. Liserre, and A. Dell'Aquila, "Control issues in single-stage photovoltaic systems: MPPT, current and voltage control," IEEE Trans. Ind. Informat., vol. 8, no. 2, pp. 241–254, May. 2012.
- M. Hanif, M. Basu, and K. Gaughan, "Understanding the operation of a Zsource inverter for photovoltaic application with a design example," IET Power Electron., vol. 4, no. 3, pp. 278–287, 2011.

- J.-M. Shen, H. L. Jou, and J. C. Wu, "Novel transformer-less grid connected power converter with negative grounding for photovoltaic generation system," IEEE Trans. Power Electron., vol. 27, no. 4, pp. 1818–1829, Apr. 2012.
- N. Mohan, T. M. Undeland, and W. P. Robbins, Power Electronics Converters, Applications and Design, Media Enhanced 3rd ed. New York, NY, USA: Wiley, 2003.
- K. Hasegawa and H. Akagi, "Low-modulation-index operation of a five level diode-clamped pwm inverter with a dc-voltage-balancing circuit for a motor drive," IEEE Trans. Power Electron., vol. 27, no. 8, pp. 3495–3505, Aug. 2012.
- E. Pouresmaeil, D. Montesinos-Miracle, and O. Gomis-Bellmunt, "Control scheme of three-level NPC inverter for integration of renewable energy resources into AC grid," IEEE Syst. J., vol. 6, no. 2, pp. 242–253, Jun. 2012.
- M. Chaves, E. Margato, J. F. Silva, and S. F. Pinto, "New approach in back-to-back m-level diode clamped multilevel converter modeling and direct current bus voltages balancing," IET power Electron., vol. 3, no. 4, pp. 578–589, 2010.
- P.Sathyanathan, Dr. P.Usharani (2015) titled "Multilevel current source inverter based on Inductor cell topology" in International Journal of Research in Science, Engineering and Technology ISSN(Print):2347 – 6710 ISSN (Online) 2319 – 8753.
- P.Sathyanathan, A.Haribasker, Dr. P.Usharani (2016), titled 'Design & Implementation of a New 7 & 15 multilevel inverter topology' in International Journal of Advanced Research in Management, Architecture, Technology and Engineering (IJARMATE), ISSN(online): 2454-9762, Volume 2, Special Issue 6, March 2016.
- J. D. Barros, J. F. A. Silva, and E. G. A Jesus, "Fast-predictive optimal control of NPC multilevel converters," IEEE Trans. Ind. Electron., vol. 60, no. 2, pp. 619–627, Feb. 2013.

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