Implementation of Low Power and Area Efficient Vedic Multiplier

Shobana Priya M S, Manikandan T, Joshua Kumaresan S, Satheesh Kumar S, Muruganandham A

Abstract*: Designing a low power consuming and area efficient Vedic Multiplier using Hybrid Full Adder. In this paper, Conventional CMOS (CCMOS) Full Adders involved in a conventional Vedic multiplier is replaced with Hybrid Full adders to achieve reduction in power consumption and area. In the proposed system ripple carry adders involved in Vedic multiplier are designed using Hybrid Full Adder. The design is done for 2-bit and it is extrapolated to 16-bit. Performance parameters such as power consumed and area between Vedic multiplier involving CCMOS and Hybrid Full Adder is done and a comparative study over them is made. Significant improvement is achieved in this implementation and the layout design is also implemented for the 2-bit, 4-bit, 8-bit and 16-bit Vedic multiplier for both Conventional CMOS and Hybrid Full-Adder logic styles. The implementation is carried out using Tanner EDA tool under 250-nm technology.

Keywords: **Multiplier, CMOS, Full Adder, Low Power, Small Area.**

I. INTRODUCTION

Arithmetic operations plays a vital role in many real-time applications. Specifically, for VLSI application it is the main building block. To improve the performance of the application, optimization of multipliers is carried out using adders. A multiplier is the main block in various applications such as Digital Signal Processing, Cryptography for the process of encryption and decryption and in other logics. Many experiments have been conducted to obtain optimized Multipliers which is Area, Power and Delay efficient. Vedic Multiplier is said to have may advantages over other multipliers.

The well-known and the basic structure of Vedic Multiplier used in almost many Digital Signal Processing system and they are designed with the complementary metal oxide semi-conductor. It has many Half-Adders and Full-Adders which leads to power dissipation and delay to the overall circuit . The delay and power optimization of the circuit is carried out by reducing the number of transistors employed in the basic adder level design. The conventional CMOS Full-Adder are replaced using Hybrid Full-Adders is used in this paper. The performance of these modified implementations is compared with those containing Conventional CMOS Full-adders and optimization with respective to area and power consumption is achieved in the proposed design.

II. VEDIC MULTIPLIER[6]

Vedic Mathematics forms the basis for Vedic Multiplier. Vedic Mathematics is a method of processing with efficient and speedy implementation of digital circuits with set of arithmetic rules Vedic Multiplier has an advantage of faster computation. Vedic Multiplier functions based on the Sutras, that are the Vedic multiplication formulas. There are 16 sutras present in order to carry out with the multiplication operation. The "Urdhva Tiryakbhyam" sutra (algorithm) is used in the proposed Vedic Multiplier. This multiplier was traditionally used in the multiplication of numbers in decimal number system. This formula is a general multiplication technique which forms the basis for all sorts of multiplication. The block diagram of n-bit Vedic Multiplier is given in Fig 1.

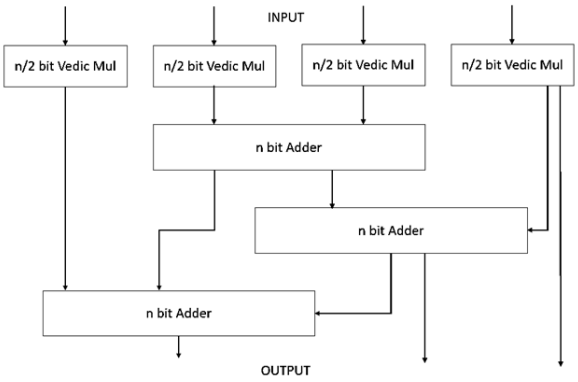

Fig. 1. n-bit Vedic Multiplier

The multiplier uses the algorithm Urdhva Tiryakbhyam (Vertical & Crosswise) of antique Vedic Mathematics. The conceptual meaning of Urdhva Tiryakbhyam is "perpendicularly and diagonally". The working of the algorithm is with the calculation of partial products. Simultaneous addition of partial products are carried out with this. The example of two numbers with this method is given in Fig 2.

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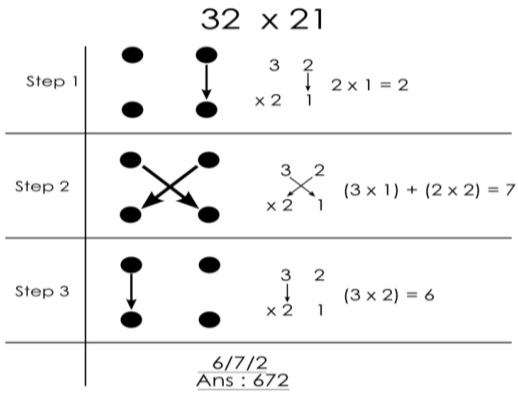

Fig 2. Model Calculation of Vedic Multiplier.

The 16-bit Vedic Multiplier structure consist of four 8-bit Vedic Multipliers and three 16-bit Ripple Carry Adders. The 8-bit Vedic Multiplier needs four 4-bit Vedic multipliers and three 8-bit Ripple Carry Adders. The 4-bit Vedic multiplier needs four 2-bit Vedic multiplier and three 4-bit Ripple Carry Adders. The structure of 16-bit Vedic multiplier is given in Fig 3.

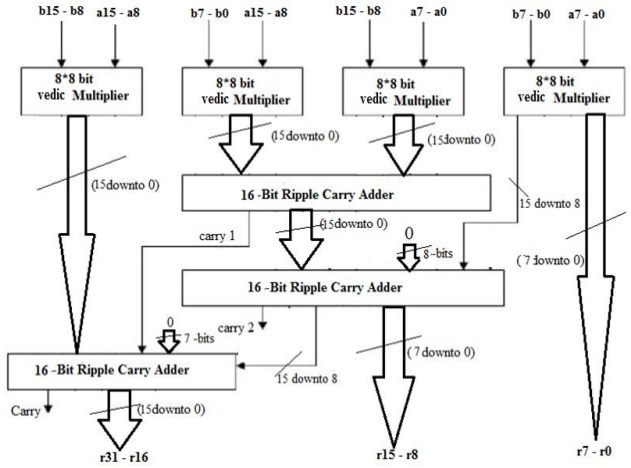

Fig 3. 16 bit Vedic Multiplier circuit.

III. HYBRİD FULL-ADDER [5]

The hybrid logic has a module for carry generation using modified XNOR. In hybrid logic (small c) conventional CMOS(CCMOS) and transmission gates are coupled together to obtain low power and high speed operation. The XNOR module is designed with Conventional CMOS and the module to generate carry is designed using transmission gates. Fig 4 shows the block diagram of Hybrid Full adder. There are two modules that are present in the design of Hybrid Full-Adder. One module is the Carry/Sum Generation Module and the other Module is the XNOR module. To achieve faster conduction, the Weak inverter is used. The weak inverter consists of smaller depletion layer that helps in quicker conduction.

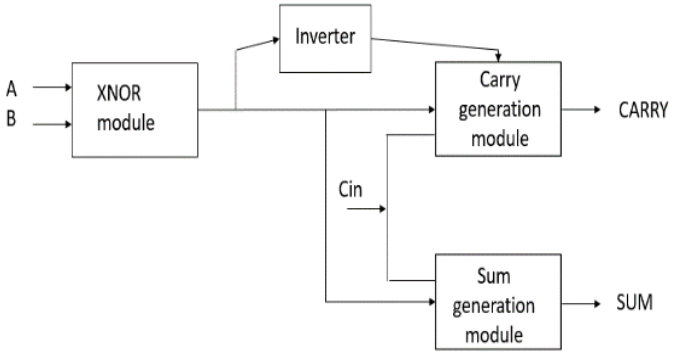

Fig 4. Hybrid Full-Adder

Fig 5 shows the transistor level diagram of Hybrid Full adder.

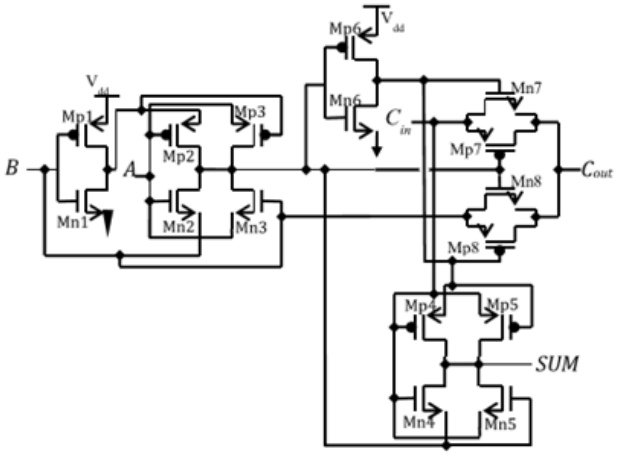

Fig 5. Hybrid Full-Adder (Transistor level)

In the place of normal Full-Adders, these Hybrid Full-Adders are used in Ripple Carry Adders of the Vedic Multiplier.

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IV. RESULTS AND DISCUSSION

The implementation of 16-bit Vedic Multiplier using CCMOS and Hybrid Full adders in Carry Save Adder block is carried out in Tanner EDA tool. The Area and Power Consumption calculations are done in in 180nm Technology. Figs 6 shows the schematics of the Multiplier design.

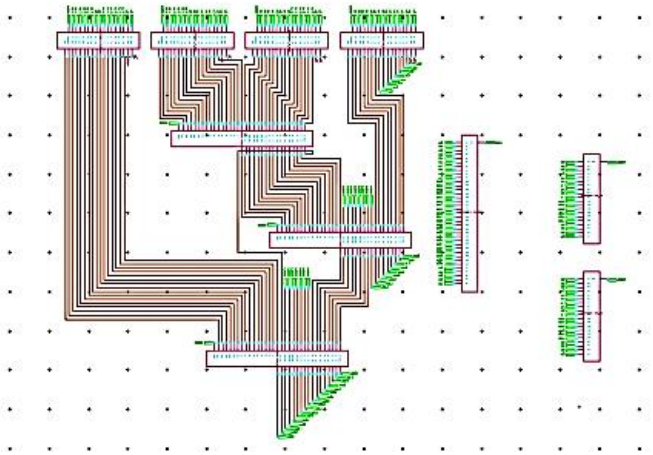

Fig 6. Schematic of Vedic Multiplier.

The Output of the 16-bit design is given in Fig 7. The Layout design is also done or the 2-bit, 4-bit, 8-bit and 16-bit Vedic Multipliers using both CCMOS and Hybrid Full-Adders. The Layout of 16-bit Vedic Multiplier using CCMOS and Hybrid Full-Adders is given in Fig 8 and Fig 9.

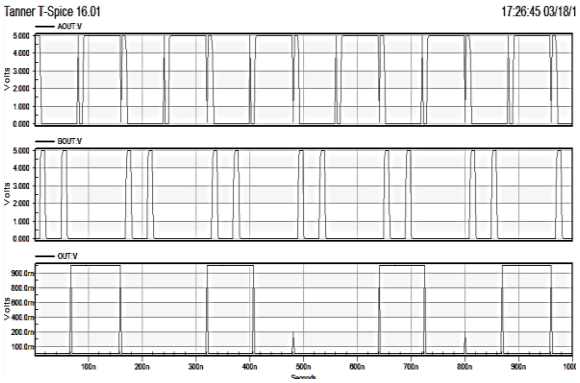

Fig 7. Output of 16-bit Vedic Multiplier

Fig 8. Layout of 16-bit Vedic Multiplier using CCMOS Full-Adder

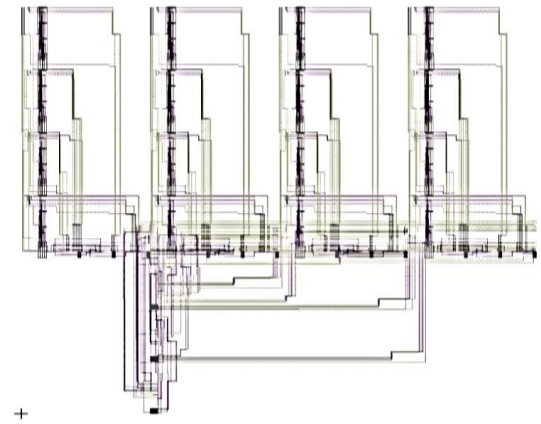

Fig 9. Layout of 16-bit Vedic Multiplier using Hybrid Full-Adder

The performance comparison of 16-bit Vedic Multiplier when executed by replacing Conventional Full-Adder with Hybrid Full-Adder has optimizes Area, Power Consumption. The bit size occupies are 2-bit, 4-bit, 8-bit and 16-bit. Table 1 shows the area and power Consumption of Vedic Multiplier with CCMOS and Hybrid Full-adders.

Table 1. Area and Power Consumption of Vedic Multiplier with CCMOS and Hybrid Full adders

Multiplier bit size	AREA		POWER(watts)	
	CCMOS	HYBRID	CCMOS	HYBRID
2-bit	58	58	3.1678 e-006	4.1566 e-007
4-bit	568	424	6.9876 e-006	8.14567 e-007
8-bit	2944	2080	1.23789 e-005	2.83456 e-006
16-bit	13900	9868	2.9876 e-004	4.56788 e-005

V. GRAPHICAL REPRESENTATION

Figs 10 and Fig 11 show the graphical representation of the result obtained in table 1

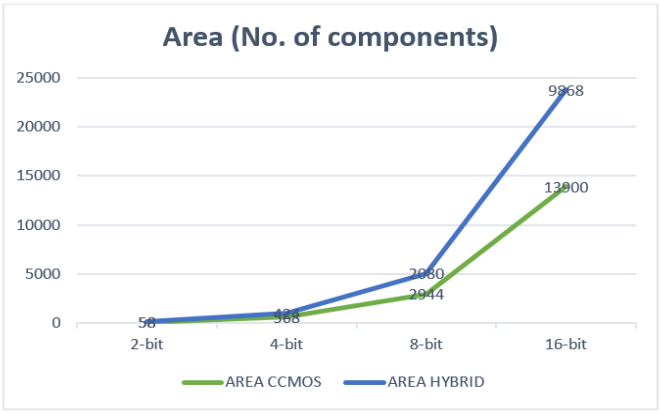

Fig 10. Area Comparison

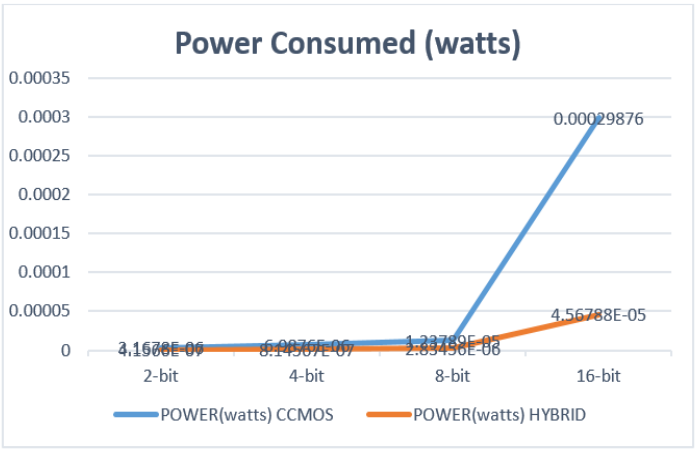

Fig 11. Power Consumption Comparison (in watts)

VI. CONCLUSION

In this paper, Analysis of Low-Power consuming Area Efficient Vedic Multiplier (16-bit) is done using Hybrid Full-Adder Circuit is proposed, designed and simulated in Mentor Graphics Tanner EDA tool. The output of the Multiplier

designed with proposed Hybrid logic is compared with the existing logic styles of Full-adders in 16 bit. The 2-bit, 4-bit, 8-bit and 16-bit Vedic Multipliers are designed in both Conventional CMOS and Hybrid Full-Adder logic styles.

From the simulated result using Tanner EDA tool the Power consumption of the existing logic styles are reduced by the proposed design by 87% for 2-bit, 89% for 4-bit, 78% for 8-bit and 85% for 16-bit when compared with the existing logic of C-CMOS to Hybrid Full-Adder and also the area (number of components) is also reduced by 36% for 4-bit, 30% for 8-bit and 30% for 16-bit when compared with C-CMOS logic to Hybrid Full-Adder logic design. The layout design is also implemented for the 2-bit, 4-bit, 8-bit and 16-bit Vedic multiplier for both Conventional CMOS and Hybrid Full-Adder logic styles.

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Dr. A. Muruganandham received the B.E. Degree in Electronics and Communication Engineering and M.E., degree in Communication systems from University of Madras and National Institute of Technology (NIT), Trichy in 1993 and 2000, respectively. He completed the Ph.D (Image Compression) degree in Anna University in the year 2013, Chennai. He is a life member of ISTE, FIEand member of IEEE. He is currently working as a Professor in the Department of Electronics and Communication Engineering, at Rajarajeswari College of Engineering, Bengaluru, Karnataka, India and has a teaching experience of 23 years. His-research interests includes Image processing and Bio Medical Engineering.