Design and Implementation of 15-Level Multilevel Cascaded Type Inverter with Reduced Switching Count

V.Tamilselvan, J. C. Vinitha, P. Usha Rani, S. Siva Subramanian

Abstract: ***In high and medium AC power applications, multilevel inverters (MLI) have significant importance in modern days. The architecture of multi-level cascaded type inverter is preferred because of reduced harmonic distortion, high quality AC output power, least switching loss and minimum switching stress. The existing method uses 8-number of switches to generate 11-level AC voltage. A new design of 15-level multilevel inverter with 6-switching devices is proposed in this paper and DC supply devices are similar to existing method, which outcomes in less switching loss, less complexity of circuit design and less cost. The DC supply for multilevel inverter is taken from solar panel with MPPT technique. The new 6-switch multilevel inverter circuit topology, switching pattern and gate pulse making is explained in this paper. The fast Fourier transform (FFT) analysis of the outputs of 11-level and 15-level of multilevel inverters are related. The new 6-switch 15 level cascaded type inverter circuit has been intended and modeled by using MATLAB software Simulink tool. The simulation outcomes are displayed with less total harmonic distortion and reduced switching loss has been achieved.***

Keywords: Multilevel Inverter (MLI), Flying clamped capacitor (FCC), T-type inverter, π-type inverter, T-type inverter, Criss cross MLI.

I. INTRODUCTION

Now a day, a huge number of industrialized applications have begun to demand high and medium power electronic appliances [1]. On the other hand, power electronic switching devices are undergoing the medium voltage applications haven't created still now. The supply devices for medium power applications are embarrassing to connect directly to the single switch using devices. For that reason, the cascaded type MLI method has been appeared as dissimilar choice for functioning with high power and medium power applications. The MLI technology not simply generates higher voltage levels, other than promotes renewable power generation devices in input side [2].

MLI (Multi level inverter) is one of the electrical power conversion strategies that produce AC type voltage as output side using input DC source [3]. Based on the connection methods of switches and supply device, MLI are classified into numerous types. Some of the recent topologies of multilevel inverter are explained in below section.

II. EMERGING TOPOLOGY OF MLI

Numerous emerging topologies of MLI have been resent in recent days which using low number of switches to make higher number of output voltage levels. They are π-type, T-Type, Criss cross type, RV type MLI, Nested type and E-topology MLI etc [4].

A. π-type MLI

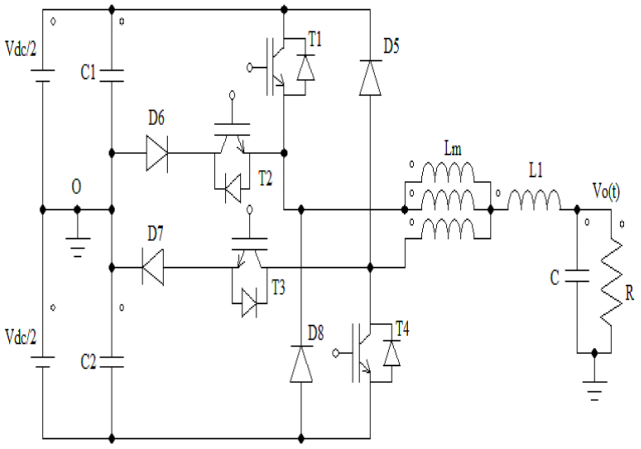

Fig. 1 π-type MLI

A 1φ, 5-level, three terminal , π topology MLI switching circuit is proposed by Yanshen Hu et al [5], as displayed in figure 1. It has proven to be a perfect option for making more level AC voltage conversion with 2- DC supply. This circuit obtains fewer harmonic and gets higher efficiency. This method offers best loss reduction and decrease the output side LC filter size. Yanshen Hu et. al. examined the current, voltage and switching loss and stress of 1φ, π topology, 5-voltage level MLI [6] has been analyzed.

B . T topology Inverter

A T type three level multilevel inverter has been introduced by M. Schweizer et al [7], which T-type MLI circuit is designed for medium power industrial devices. Figure 2 displays the circuit diagram of T- topology 3-level MLI. This 3-level circuit is the modification of 2- level inverter circuit by connecting a bi-directional switching device in dc link part for best output voltage. This circuit

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offers better efficiency when switching frequency is low for the reason that low switching loss related to neutral point clamped inverter.

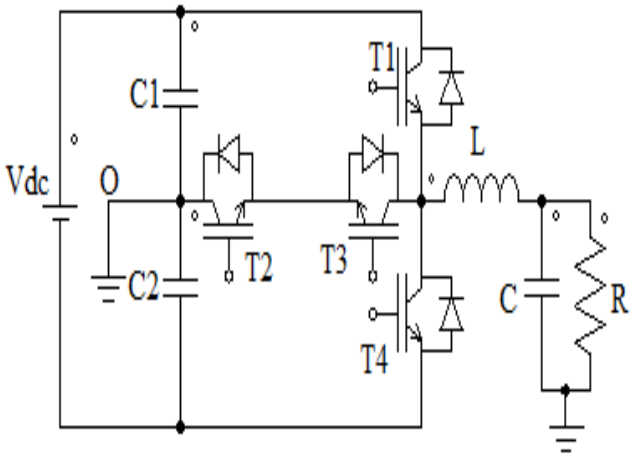

Fig. 2 T topology 3-level MLI

C. Cross switched Inverter

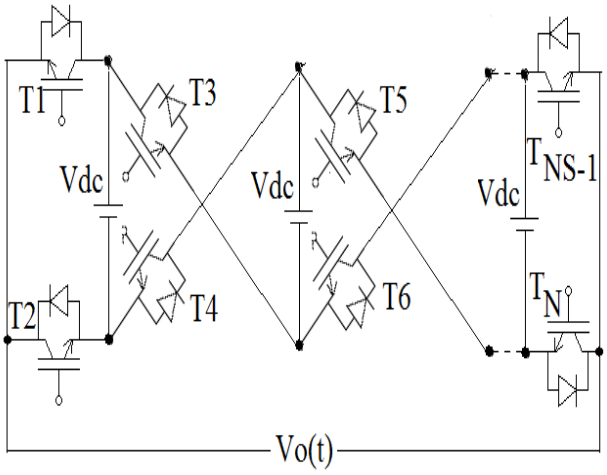

Fig. 3 Cross switched MLI

The cross switched multilevel inverter is introduced by Mahdi Toupchi, which goal as higher voltage levels by low switching device count as displayed in figure 3. Cross type circuit connection is not enhance the switching stress [8].

In this work, a new 15-level multilevel cascaded type inverter with 6-switching device and 3- DC voltage source has been presented. New circuit pattern, gate pulse and switching sequence have been discussed. The working possibility of this new method has been analyzed using MATLAB simulation results.

III. CONVENTIONAL MULTILEVEL INVERTER

A. 11-level 6-switch multilevel inverter has been explained in this section. The circuit of conventional 11-level MLI is shown in figure 4. This circuit contains 3-DC supply source, which is connected to the input of multilevel inverter that has capability to make 11-levels with 8 switches. Input voltage sources are selected as the ratio of 1:2:2 to the multilevel inverter. The input DC supply has been given to MLI from solar panel. The output voltage level of MLI is based on the switching sequence.

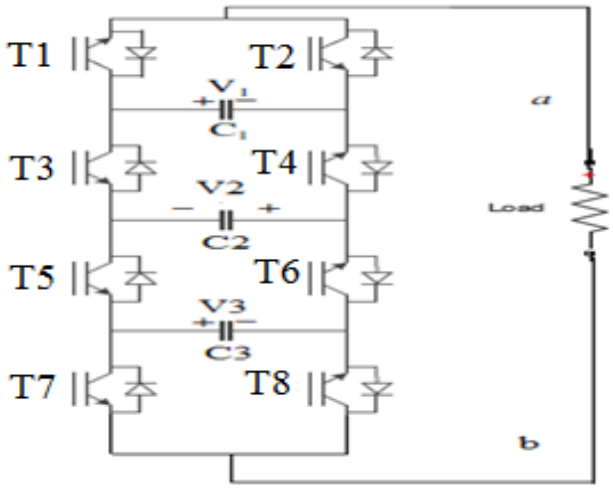

Fig. 4 Conventional multilevel inverter

B. Switching Sequence: The switching sequence used to generate 11-level AC output voltage from 3- DC source and 8 switches has been indicated in table 1 as shown below. The ON and OFF condition of switch to produce voltage levels in output side is given in table 1. Here input DC voltage ratio is 1:2:2 i.e, V1=5V, V2=10V and V3=10V. To get 5V as output, the switches S1, S4 and S5 will be present in turn on condition.

Table 1: 11-level MI Switching state

Switching state	T1	T2	T3	T4	T5	T6	T7	T8	Vout
1	1	0	0	1	0	1	0	1	V1 = 5V
2	0	1	0	1	1	0	1	0	V2 = 10V
3	1	0	0	1	1	0	1	0	V1+V2 = 15V
4	0	1	0	1	1	0	0	1	V2+V3 = 20V
5	1	0	0	1	1	0	0	1	V+V2+V3 = 25V
6	0	0	0	0	0	0	0	0	0
7	0	1	1	0	1	0	1	0	-V1 = -5V
8	1	0	1	0	0	1	0	1	-V2 = -10V
9	0	1	1	0	0	1	0	1	-V1-V2=-15V
10	1	0	1	0	0	1	1	0	-V2-V3=-20V
11	0	1	1	0	0	1	1	0	-V1-V2-V3=-25V

The switching sequence table clearly shows the three input voltage source has been used to produce 11-level AC output voltage with less total harmonic distortion.

IV. NEW 15-LEVEL 6-SWITCH MLI

The new 15-level MLI circuit contains 6-switching devices and 3-DC supply source. The conventional 11- level multilevel inverter used 8-switches and 3-DC source. Compared to conventional technique, the proposed technique generates 4-more levels by using 6-switches. Figure 5 shows the block diagram of proposed 15-level MLI.

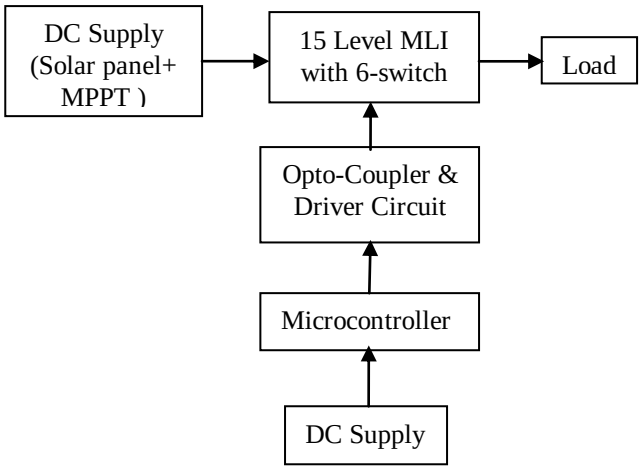

Fig. 5 Proposed block diagram

The components present in this proposed method are solar panel, 15-level multilevel inverter, AC load, microcontroller, opto-coupler and driver circuit. Each and every unit is explained in below sections.

a. SOLAR CELL AND PANEL MODELLING

Design and modeling of photovoltaic cell and panel can be derived by many methods in software like PSPICE & MATLAB etc. There are numerous schemes to symbolize a model as like Physical modeling, Mathematical modeling and Embedded Programming [10].

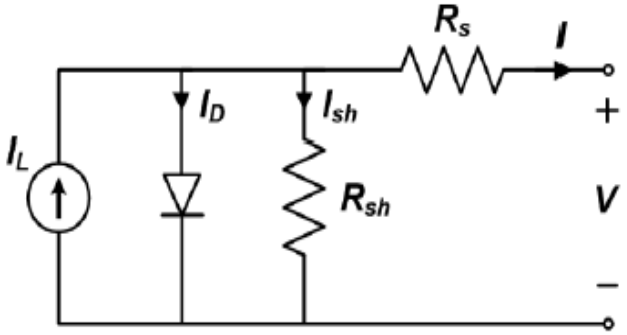

Fig. 6 Electrical equivalent of photovoltaic cell

Electrical equivalent circuit of single photovoltaic cell is displayed in figure 6. In the circuit diagram Rs indicates series resistance of P-N junction of solar cell and Rsh indicates shunt resistance. The voltage-current characteristics of solar cell depend upon series resistor [11]. I_d is current flows through diode and Ish is shunt leakage current. The output current I is calculated by applying KCL in equivalent circuit:

$$I = I_{ph} - (I_d + I_{sh})$$

From the equivalent circuit, output current is the sum of diode current and shunt resisitor current [12]. Hence the simplified equation is

$$I = I_{ph} - I_0$$

Photon current (I_{ph}) is produced on incorporation of solar irradiation by hotovoltaic cell therefore photocurrent (I_{ph}) value is directly linked to deviation in solar temperature and irradiance that is [13]:

$$I_{ph} = (I_{scr} + k_i \Delta T)\frac{G}{G_r}$$

The photovoltaic cell reverse saturation current (Irs) will be determined by [14]:

$$I_o = I_{rs}\left(\frac{T}{T_{ref}}\right)^3 \exp\left[\left(\frac{q\,E_{go}}{A\,K}\right)\left(\frac{\Delta T}{T_{ref}\,T}\right)\right]$$

Where, Irs - reverse saturation current.

Ego - band-gap energy of pn junction material.

The current values of Io and Iph will derived the value of current I as follows [15]:

$$I_{pv} = I_{ph} - I_0\left[\exp\left(\frac{q(V_{pv} + I_{pv}R_s)}{AKT}\right) - 1\right] - \frac{(V_{pv} + I_{pv}R_s)}{R_p}$$

The power output is exaggerated by weather constraint variations that are shading and temperature [16]. If temperature rises above insignificant value then voltage loss varies from 0.022 to 0.056 V/°. V-I and P-V waveform for dissimilar temperature and irradiance are shown in figure 7.

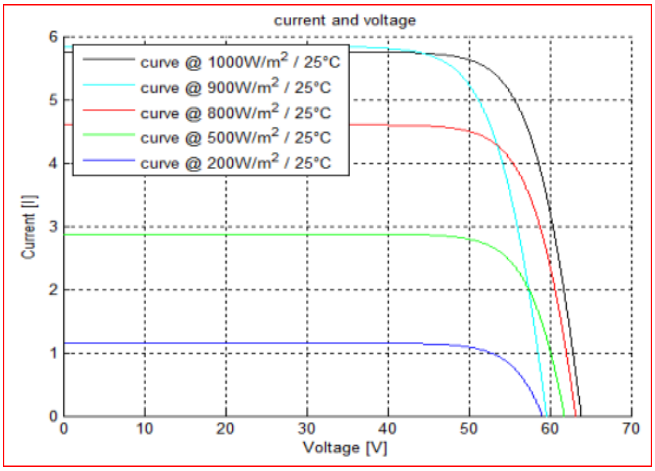

Fig. 7 Voltage and current curve for PV cell with different temperature and intensity

TABLE 2: SOLAR MODULE PARAMETER

VARIABLE	PARAMETER	VALUE
PV	Model	F-MSN-75W-R-02
Pmax	Maximum output power	75 W
Vin	Open circuit voltage	21.7 V
Isc	Short circuit current	5.0 A

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b. MPPT BY P&O TECHNIQUE

Power generation of solar panel depends upon climatic condition such as temperature and radiation. MPPT (Maximum Power Point Tracking) method is a technique used to regulate output DC voltage of solar panel. Perturb and observation algorithm is used to MPPT technique. Figure 8 displays flow chart of P&O. This algorithm senses the input voltage and current from photovoltaic panel using voltage and current sensors.

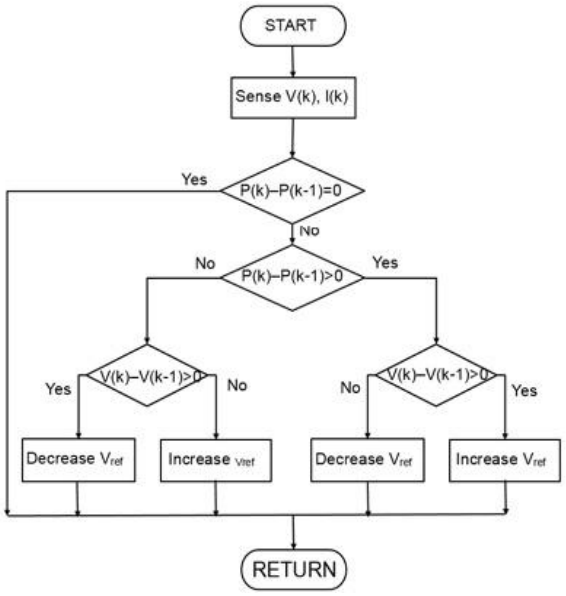

Fig. 8 Flowchart for P&O algorithm

C. PROPOSED 15-LEVEL MLI

The proposed multilevel inverter produced 15-output AC voltage levels without using capacitors and bidirectional switches. It contains 6 number of controlled switching devices (S1, S2, S3, S4, S5 and S6) and one diode (D) connected in between three supply DC sources (Vdc1,Vdc2 and Vdc3) as shown in figure 9.

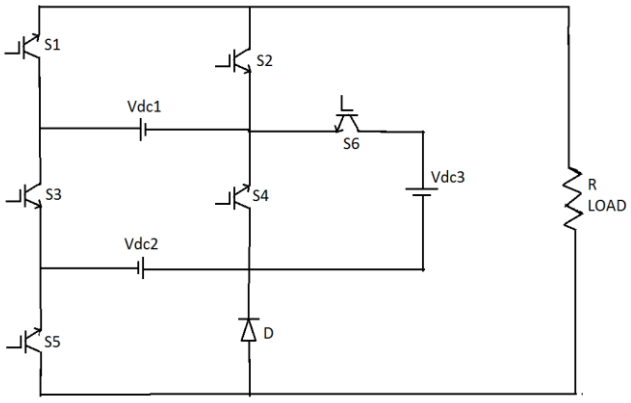

Fig. 9 Proposed circuit diagram

The supply devices Vdc1, Vdc2 and Vdc3 are give voltage to the load in the proportion of 1:2:4 respectively. Here, Vdc1=5V, Vdc2=10Vand Vdc3=20V is used. The voltage sources are connected or disconnected to load depend upon the ON and OFF condition of switches S1-S6, hence the alternating 15-level voltage appear across the load. The modes of operation of making all levels of AC output voltage is explained in below section.

d. MODES OF OPERATION

All current flow paths of all modes of operation is explained in this section.

Mode 1 (Vo = Vdc1 = 5V):

In this mode of operation, the voltage source Vdc1 is connected to load through the source Vdc1- S1- R load- D - S4 - Vdc1. Hence Vdc1=5v is appear across the load. This current flow direction is shown in figure 10.

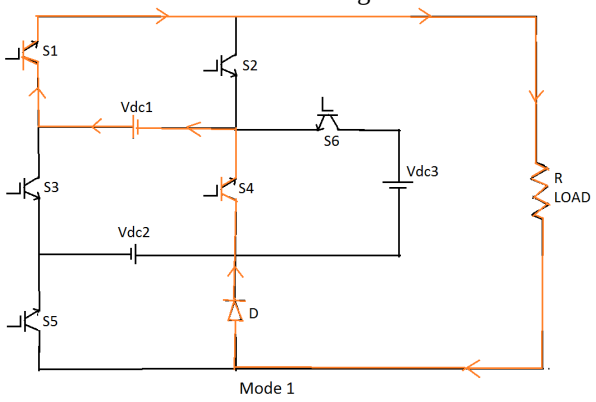

Fig.10. Mode 1 operation

Mode 2 & 3 (Vo=Vdc2 & Vo=Vdc1+Vdc2):

In mode 2 operation, the voltage source Vdc2=10V appear across the load. The current flow path in this mode of operation is Vdc2 – S4 – S2 – R load – D – Vdc2, as shown in figure 11.

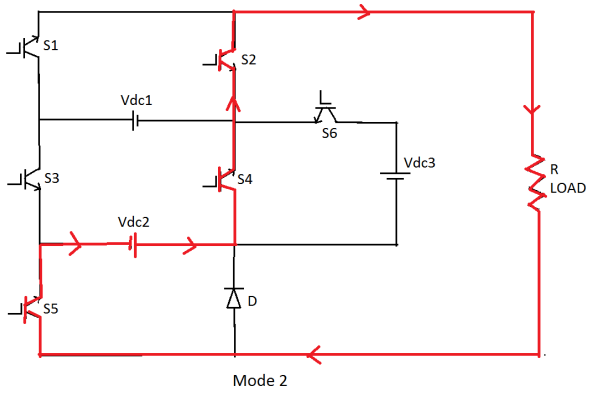

Fig. 11 mode 2 operation

Figure 12 shows the current flow path of 3rd mode operation. The circuit will close through source Vdc1+ Vdc 2=15V. the circuit is closed through Vdc1 - S4 - Vdc2 – S1 – R load – S5 – Vdc1.

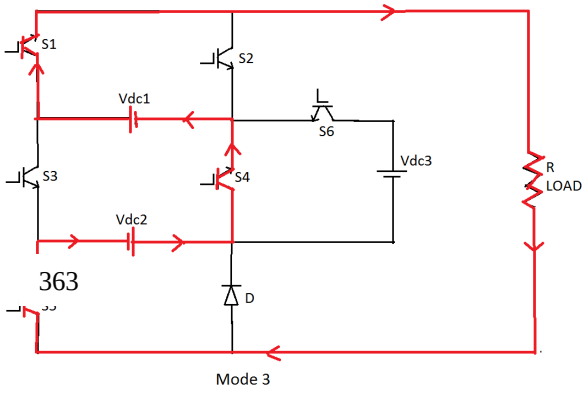

Fig. 12 mode 3 operation

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Mode 4 & 5 (Vo=Vdc3 & Vo=Vdc1+Vdc3):

In mode 4 operation, the voltage source Vdc3=20V appear across the load. The current flow path in this mode of operation is Vdc3 – S6 – S2 – R load – D – Vdc3, as shown in figure 13.

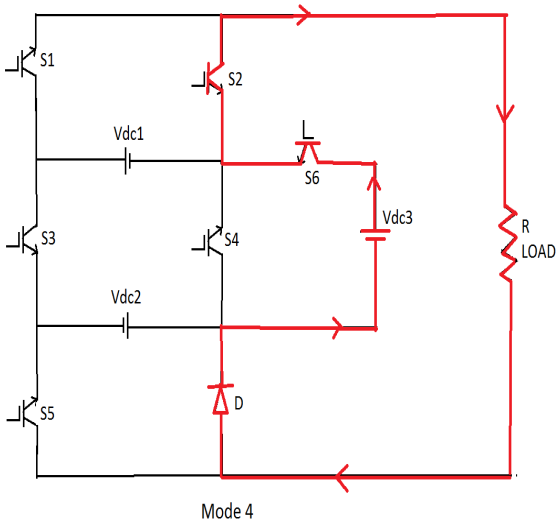

Fig. 13 mode 4 operation

In mode 5 operation, the voltage source Vdc3+Vdc1=25V appear across the load. The current flow path in this mode of operation is Vdc3 – S6 – Vdc1- S1 – R load – D – Vdc3, as shown in figure 14.

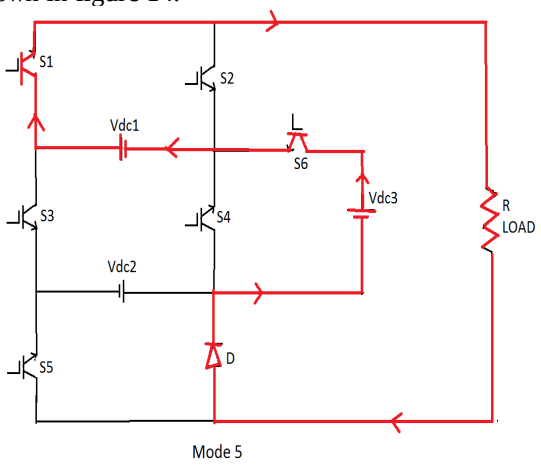

Fig. 14 mode 5 operation

Mode 6 & 7 (Vo=Vdc2+Vdc3 & Vo=Vdc1+Vdc2+Vdc3):

In mode 6 operation, the voltage source Vdc2+Vdc3=30V appear across the load.

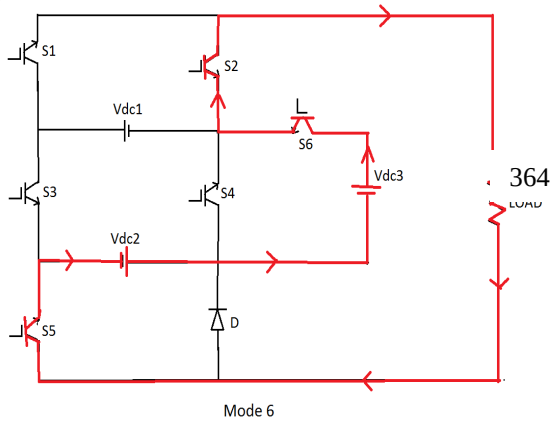

Fig. 15 mode 6 operation

The current flow path in this mode of operation isVdc2 - Vdc3 – S6 – S2 – R load – S5 – Vdc2, as shown in figure 15.

In mode 7 operation, the voltage source Vdc1+Vdc2+Vdc3=35V appear across the load. The current flow path in this mode of operation isVdc2 - Vdc3 – S6 – Vdc1 – S1 – R load – S5 – Vdc2, as shown in figure 16.

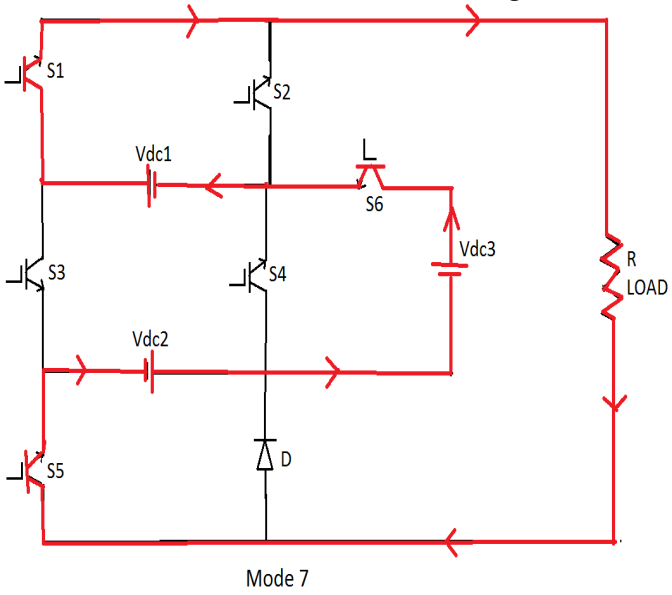

Fig.16 mode 7 operation

Mode 8 (Vo=0V)

In this mode of operation all switching devices are turn off condition to generate 0V as output across load.

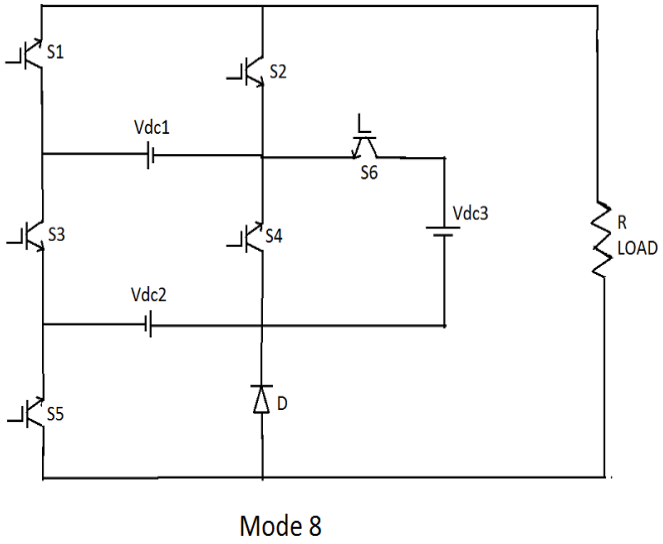

Figure 17. Mode 8 operation

The above modes of operation are written as table for easy understanding as shown in below switching state table 3. This table contains the On and OFF state switches to make each and every level of output voltage.

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Switching state	S1	S2	S3	S4	S5	S6	Vo
1	1	0	0	1	0	0	Vdc1
2	0	1	0	1	1	0	Vdc2
3	1	0	0	1	1	0	Vdc1+Vdc2
4	0	1	0	0	0	1	Vdc3
5	1	0	0	0	0	1	Vdc3+Vdc1
6	0	1	0	0	1	1	Vdc3+Vdc2
7	1	0	0	0	1	1	Vdc3+Vdc2+Vdc1
8	0	0	0	0	0	0	0

Table 3: Switching State Table

V. SIMULATION RESULT:

The working of new15-level circuit is analyzed by MATLAB software. Simulation circuit, gate pulse, output voltage, output current and THD waveforms are explained in this section.

SIMULATION CIRCUIT DIAGRAM OF PROPOSED MLI:

Figure.18 demonstrates the 15-level MLI circuit diagram drawn in MATLAB Simulink software. Gate pulses are given to all controlled switching devices and resistive load is used to measure AC output voltage. Voltage and current measurement blocks are used to display output AC voltage and current. FFT analysis block is present in MATLAB to measure THD present in AC voltage.

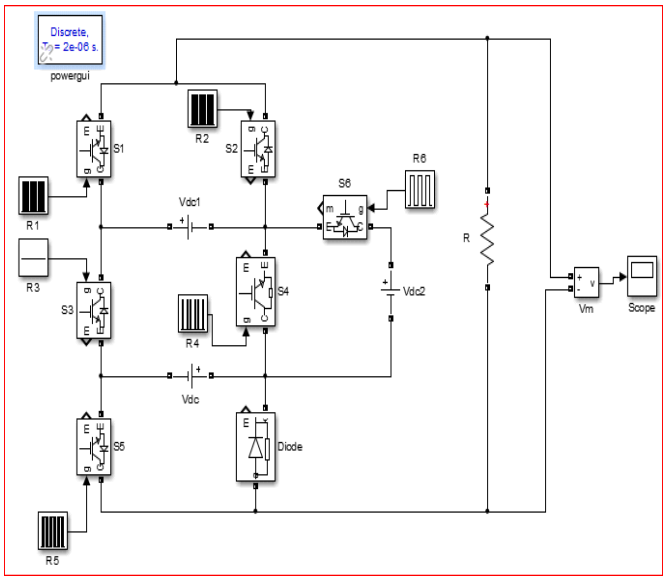

Fig. 18 Simulation circuit diagram

GATE PULSE:

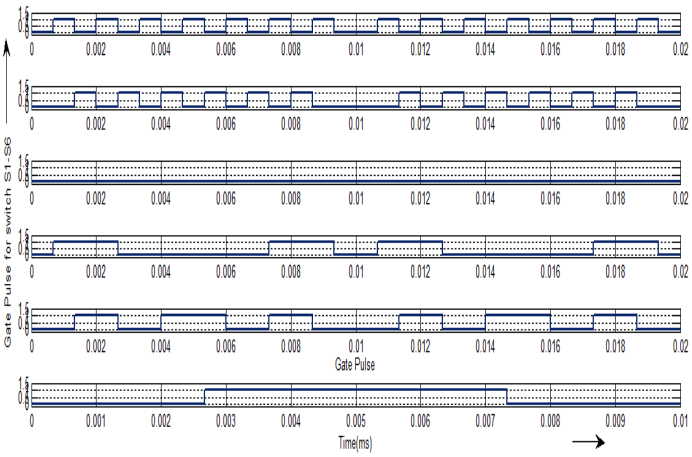

Fig. 19 Gate pulse given to switch S1 - S6

This proposed 15-level multilevel inverter contains 6 numbers of controlled switching devices (S1-S6). The amplitude of AC output depends upon ON and OFF condition of six switches. This gate pulses are generated based on switching sequence table. Figure 19 shows the gate pulse for S1-S6 switches.

OUTPUT VOLTAGE WAVEFORM

The number of levels produced across load has been demonstrated in figure 20. The amplitude of supply DC sources are Vdc1=5V, Vdc2=10V and Vdc3=20V. Hence the amplitude of AC output voltage is 32.5V; remaining voltage is dropped across switching devices. The frequency of AC output voltage is 50Hz. The magnitude of AC voltage has been varied based on the proportion of supply side DC source.

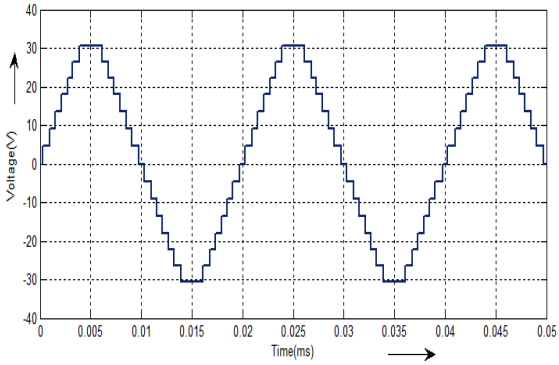

Figure 20. Output voltage and current

OPTOCOUPLER AND DRIVER CIRCUIT:

Most recent optocoupler strategies use a phototransistor as their input side; such device is commonly known as an ‘optocoupler’, because the input side LED and the output terminal phototransistor are optically attached. **Figure 21** displays the basic structure of an optocoupler, together with 18V driver circuit.

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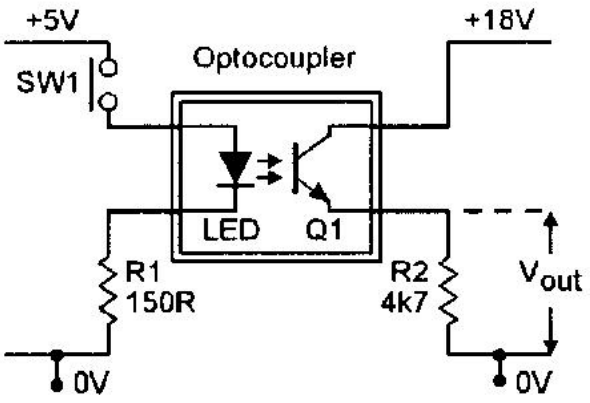

Fig. 21 Optocoupler and driver circuit

When SW1 switch is in open condition, no current will flows through the LED, hence no light fall on the phototransistor Q1; Q1 transmits virtually 0 collector terminal current under this situation, therefore 0 voltage is present across output terminal resistor R2. On the other hand, when switch SW1 is closed, current will flows to R1 resistor through the LED, and the resultant light falls on phototransistor Q1, therefore collector voltage (18V) will across R2 resistor (Vout). In this circuit, the output terminal current is regulated by its input terminal current, that a regulator circuit coupled to its input terminal can be isolated electrically from the entire output circuit. This 'isolating' property is the key attraction of this kind of optocoupler, which is commonly called as an isolating- optocoupler.

MICROCONTROLLER:

Microcontroller is used to generate gate pulse for controlled switching devices. In this proposed circuit, 6 controlled switches are used. So we need to generate 6 gate pulses. The Delfino Micro controller series of C2000 real time Controller is leading floating point presentation and analog combination to regulate applications. The Delfino microcontrollers have simplified development and offer world class dispensation for demanding, real time application. The main feature of this dual core microcontroller is operating at 200 MHz on each central processing unit and single core processors operat o 300 MHz. The pulse generation using this proc e very easy. These microcontrollers are directly interface to matlab software for generate gate pulse.

I.THD (HARMONIC DISTORTION):

THD is a computation of nearness value to waveform which is attain to the outline of the fundamental frequency waveform. It can be determined by using following equation

$$THD = \frac{1}{V_1}\sqrt{\sum_{n=2,3}^{\infty} Vn^2}$$

Where, V_1-Voltage with fundamental frequency and V_n-Voltage of n^{th} order frequency wave.

THD ANALYSIS OF SINGE LEVEL AC OUTPUT VOLTAGE:

THD analysis of one-level AC voltage obtained from single H-bridge MLI is illustrated in figure 22. This single level AC output voltage is generated by using single DC source and 4 switching devices. The THD value present in this output is: 48%.

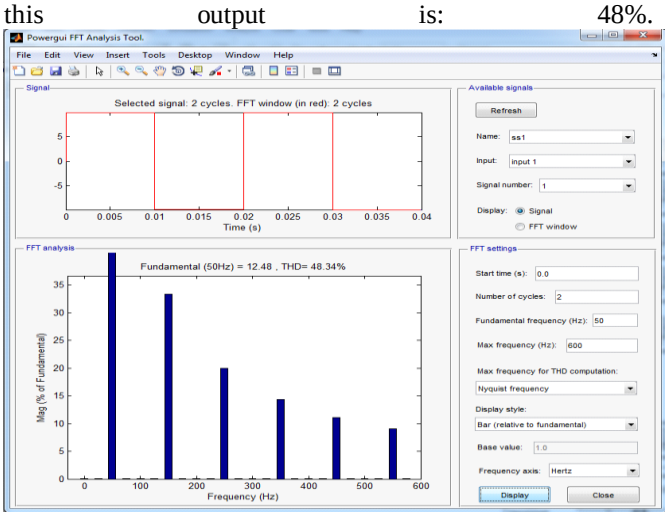

Figure 22: THD analysis of single level AC voltage

THD ANALYSIS OF CONVENTIONAL 11-LEVEL MLI:

The THD analysis of conventional 11-level multilevel inerter with 8-switching device is shown in figure 23. The total harmonic distortion resent in this waveform is around 9%.

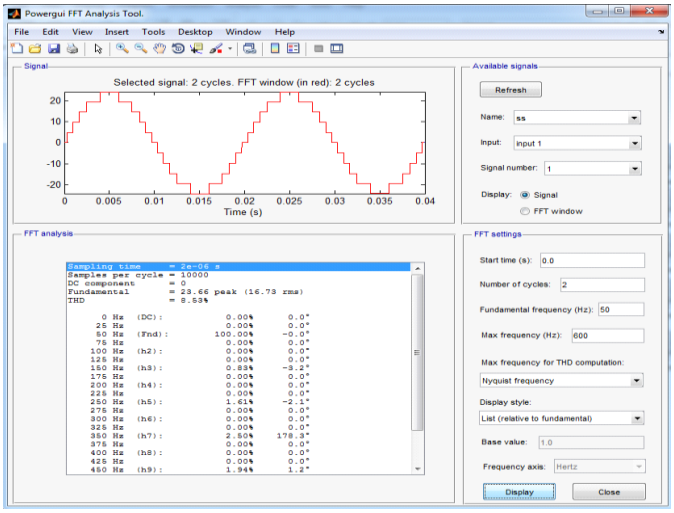

Figure 23: THD analysis of 11-level MLI

In figure the AC voltage is taken as input parameter for FFT analysis is done using the given sampling time, samples per second etc through which total harmonic distortion can be calculated.

THD ANALYSIS OF PROPOSED 15-LEVEL MLI:

Using MATLAB Simulink software FFT analysis is done by using nyquist frequency to find THD value, which is displayed by either bar chart or list of values.

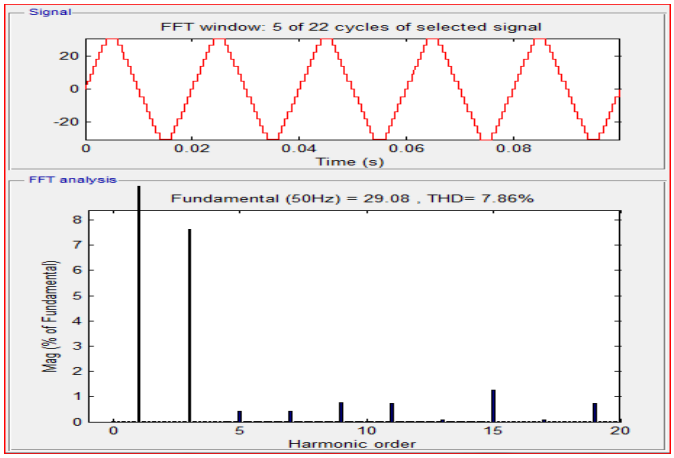

Fig. 24 THD analysis of proposed 15-level MLI

The THD value present in 15-level MLI is : 7.86% using FFT analysis method in MATLAB software as shown in figure 24.

COMPARISION

The THD value assessment of various AC voltage levels has been displayed in table 3.

Sl.No	Output voltage Level	Number of switches used	THD %
1	1 level	4	48.34
2	7-level	6	12
3	11-level	8	8.53
4	15-level	6	7.86

From this table, total harmonic distortion is reduced, when the voltage levels are increased. The switching count of proposed method is low compared to conventional techniques.

VI. CONCLUSION

Thus a new 15-level single phase AC voltage topology has been proposed with 6 power semiconductor switching device, less THD and low conduction loss and switching stress and loss. In consequence of using less switching devices, automatically reduce the circuit complexity, size and cost, which automatically decrease the conduction and switching and losses. The main advantage of this proposed method rather than existing scheme is huge drop of THD. The circuit configuration of proposed method is simple hence the gate pulse making and control strategy also very simple. The harmonic distortion of proposed 15-level AC output voltage has been reduced around 2% when compared to conventional 11-level AC output voltage method. These results are obtained from the simulation of MATLAB simulink software.

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