International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-9 Issue-2, December 2019

Design and Performance Analysis of Low Power High Speed CNTFET Binary Content Addressable Memory Cell for Next Generation Communication Networks

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Abstract: ***In this paper, Carbon Nanotube Field Effect Transistor (CNTFET) based Binary Content Addressable Memory (BCAM) cells are proposed. The adiabatic logic is integrated with the proposed BCAM cells to improve performance. The performance of proposed BCAM cells is presented for various CNTFET parameters such as number of tubes, chirality vector, pitch value, dielectric constant and dielectric materials. It also explores the optimum set of CNTFET parameters for low power and high speed characteristics of the proposed BCAM cells. Simulation results show an improvement in the average power and delay of proposed BCAM cells. The average power of the proposed BCAM cells is in the order of nano watts while the CMOS based BCAM cells is in the order of micro watts. The delay of the proposed BCAM cells is improved by 56.4 %. All simulations are conducted for both CMOS and CNTFET based BCAM cells in HSPICE at 32 nm technology.***

Keywords: carbon nanotube field effect transistor, content addressable memory, optimum parameter set.

I. INTRODUCTION

With unprecedented growth in wireless mobile devices and Internet of Things (IoT) applications, there is enormous demand for high performance circuits which consumes less power to support the wireless communication system. To achieve this, routing protocols use the cached routing information. With either static random access memory (SRAM) or Content-addressable memory (CAM), the routing information can be cached. CAM is a distinctive form of memory, as an expansion of SRAM, which compares input search information with stored information [1]. Consequently, it is appropriate for quick parallel search activities and is used in numerous communication associated circuits and network routers.

Content-addressable memory is a kind of memory that works as a human brain.

Revised Manuscript Received on December 30, 2019.
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In order to retrieve the information, it utilizes a portion of the information itself to access the locations. Binary CAM is the easiest type of CAM in information search phrases and uses purely 1s and 0s. CAMs are commonly used in the look-up tables, network routers and cache controllers. The CAM's structure is similar to that of normal RAM, but for its comparison operation it has additional circuitry [2]. The challenging job is to design new circuitry which can consume less power without compromising its performance.

At nanoscale CMOS faces challenges like short-channel effects, leakage current and source-to drain tunneling. Because of the high mobility of electrons movement near ballistic transport and high driving capacity and smaller area, the CNTFETs are become promising alternate for CMOS technology especially when the device scaled at nanometer range. The CNTFET outperforms compared to CMOS for logic circuits and transmission lines [3-8].

It is observed that adiabatic/ energy recovery techniques gaining popularity and show better performance compared to conventional techniques. An adiabatic clocking logic circuits were proposed and the simulative inquiry was carried out on the proposed 1-bit full adder, showing a substantial energy savings of 70 percent compared to the standard CMOS logic in the transition frequency range of 10 to 200 MHz. The authors described a PB-CAM parameter extractor based on Quasi-1n1p that reduces power consumption relative to other extractors of PB-CAM parameters [9-11]. In [12], a CAM cell was presented using a phase change memory (PCM). A memory core composed of a CMOS transistor and a PCM offered important benefits such as search power over other models observed in the technical literature. The authors provided a parallel search / search CAM in [13] and presented a novel pre-charge-free CAM. Post-layout simulations at 45-nm technology disclosed that the power is decreased substantially up to 93%. Many other techniques are presented to improve the performance of the CAM cells [14-21]. But all methods based on CMOS result in high energy consumption. While some of the works are presented with CNTFET-based CAM cells but not explored the optimal CNTFET parameter set for the efficient BCAM cells and adiabatic logic / charge recovery logic integration with CNTFET.

In this paper, we propose three types of BCAM cells based on CNTFET with integration of adiabatic logic / charge recovery logic.

We present the analysis of CNTEET for delay and average power with various device parameters such as number of CNT tubes, pitch, chirality vector, dielectric constant and dielectric material. We also determine the optimal CNTET parameter for the low power high speed BCAM cells. CNTFET with integration of adiabatic logic / charge recovery logic integration has shown good improvement in power consumption and delay. The rest of the document is arranged as follows. Section II presents the conventional BCAM operation and the proposed CNTFET based BCAM cells. Section III presents the result analysis and performance analysis of the proposed CNTFET based BCAM cells. Section IV concludes the paper.

II. CONVENTIONAL AND PROPOSED CNTFET BCAM CELLS

Conventional BCAM cell operation is presented to understand the proposed CNTFET based BCAM cells well. The following subsection presents the basic operation of conventional BCAM cells, proposed CNTFET based BCAM cells, basic operations include read operation, write operation and search operation

A. Conventional Binary CAM

Binary CAM (BCAM) can store either logic 1 or logic 0. Conventional BCAM comprises of a simple six transistor SRAM cell and comparison circuit. SRAM cell is used for data storage while the comparison circuit is used for search operation. Bit lines (BLs) and word line (WL) are used to perform READ and WRITE operations. In the search lines (SLs), the search bit is provided. Each cell (bit) connects to a match line (ML) in a data word. The logic level of ML depends on the match. There are two types circuitry for comparison: NAND and NOR-type. The conventional NOR type BCAM circuitry is shown in Fig.1. The basic SRAM cell to hold the either of the logic level and is composed with transistors M1-M6. The comparison circuit is designed with transistors M7-M10. The ML is at logic 0 if stored bit and search bit are different.

B. Write operation

The transistors M5 and M6 are called access transistors. These transistors are used for both data read operation and data write operation. The data read/ write operation is performed by enabling the WL. While WL is at high level, supply the data to be written on BL. For example, assume that internal node $Data$ is at low logic level. If we wish to make it logic high, set $WL = 1$ and $BL = 1$. Now, the internal node is set at logic high. This value is retained with the help of cross-coupled inverters. Suppose assume that internal node $Data$ is at high logic level. If we wish to make it logic low, set $WL = 1$ and $BL = 0$. Now, the internal node is set at logic low. This value is retained with the help of cross-coupled inverters.

C. Read operation

The data read operation can be performed with WL is made to high level. The stored data at internal nodes can be accessed through BL. For example, assume that internal node $Data$ is at low logic level. If we wish to read it, set $WL = 1$ and access the data present on BL. The values BL and $\overline{BL}$ are the complement to each other.

D. Search operation

CAM cells are used not only to store the data and is mainly designed to perform search operation. The data to be search is provided through SL. If data to be search is same on the search line and internal node , i.e., $Data = SL$, the value of the ML will be at logic high. If mismatch occurs, it is at logic low level. If ML is at high level means match found otherwise not found.

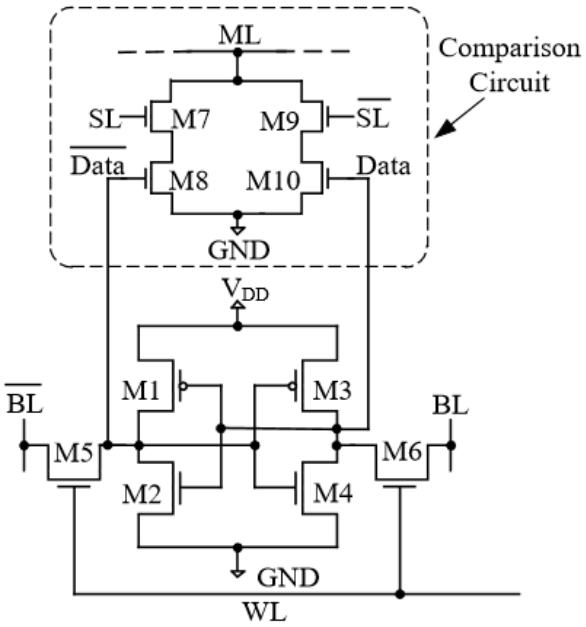

Fig.1 Conventional Binary CAM cell Circuit

III. PROPOSED CNTFET BASED IECRL CAM CELL

In this section, the proposed three CNTFET based BCAM cell circuitry and their operation with respect to search operation is presented. All the three BCAM cells are designed with CNTFET and based on adiabatic logic. These three BCAM cells are Improved Efficient Charge Recovery Logic (IECRL) BCAM cell, CNTFET based Improved Positive Feedback Adiabatic Logic (IPFAL) BCAM cell and CNTFET based Improved Pass Transistor Adiabatic Logic (IPAL) BCAM cell. The circuit diagrams of proposed CNTET IECRL, IPFAL and IPAL BCAM cells are shown in Fig 2, Fig.3 and Fig.4 respectively. The adiabatic logic/ charge recovery logic is integrated with CNTFET to improve the performance of the BCAM cells. Here, power clock (PC) signal acts as a WL. The sinusoidal signal is considered as a PC.

The search operation in CNTFET based IECRL is as follows. Input A acts search data. The stored values are considered as B and $\bar{B}$. If the input data A matches with the values of B, then ML goes high otherwise it is at low logic level. The search operation in CNTFET based IPFAL is as follows. Its output is used for driving the match line. Here also, input A acts search data and the stored values are considered as B and $\bar{B}$. If the input data A matches with the values of B, then ML will follow the power clock. If a mismatch is found, the ML value is found to be low. The search operation in CNTFET based IPAL is as follows. Input A acts search data and the stored values are considered as B and $\bar{B}$. If the input data A matches with the values of B, then ML will follow the power clock. If a mismatch is found, the ML value is found to be low.

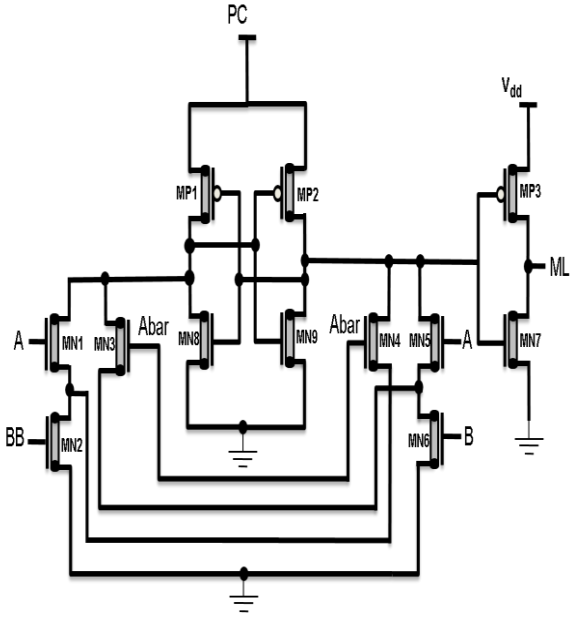

Fig.2: CNTFET based IECRL CAM cell

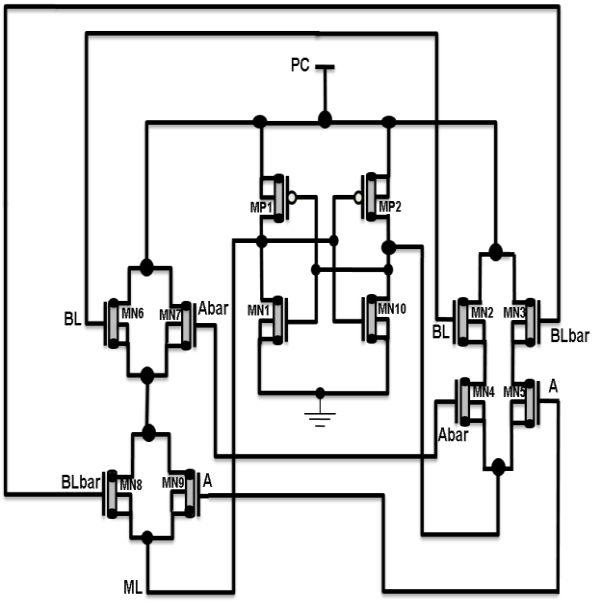

Fig.3: CNTFET based IPFAL CAM cell

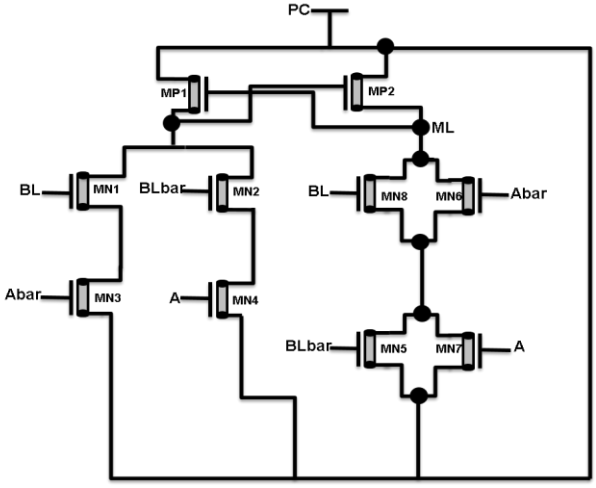

Fig.4: CNTFET based IPAL CAM cell

IV. RESULT ANALYSIS

This section presents the variations in the delay and average power of the proposed BCAM circuits with respect to carbon nano (CN) tube count, pitch value, chirality vector, dielectric constant and dielectric material. The simulations are performed using HSPICE. The Power clock is considered as a sinusoidal of amplitude 0.7 V and frequency 125 MHz. The logic 1 is considered as 0.7 V and logic 0 is considered as 0V for both A and B. All three proposed CNTFET based binary CAM cells are used the same logic levels and power clock signals. The technology used CMOS and CNTFET is 32nm Technology.

A. Average power and delay variations with CN Tube count

The chiral vector (n, m) defines whether CNT is semiconductor or conductor. The diameter of CNT is determined from Eq. (1)

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + nm} \qquad (1)$$

where $a_0 = 0.142$ nm. The parameter a_0 represents the interatomic distance between carbon atoms. The diameter of CNTFET changes with changes in chirality vector and is shown equation (1). The threshold voltage of a CNTFET is given by Eq. (2):

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{a\,V_\pi}{eD_{CNT}} \qquad (2)$$

where $a = 2.49A^0$ is the carbon to carbon atom distance, e is the charge on an electron, and $V_\pi = 3.033eV$ is the carbon π–π bond energy in the tight-bonding model. The width of the channel is related by

$$W = (N-1)S + D_{CNT} \qquad (3)$$

where N represents the number of CNTs and S represents the inter nanotube spacing.

The variations of the average power of the proposed CNTFET - IECRL-CAM, CNTFET -IPAL-CAM, CNTFET -IPFAL-CAM for different number of tubes is analysed and is shown in Fig.5. The power consumed by the proposed circuits is increases with the increase in the number of tubes of CNTFET. It is found that the proposed circuits consume less power when tube count of CNTTET is 03 compared to the other values of tube count. From Eq. (1), it is clear that the diameter and threshold voltage are inversely proportional. As tubes count increases the conductivity also increases which increases the average power consumption. Among the three proposed BCAMs IPFAL based BCAM consumes less power compared to IECRL and IPAL based BCAMs. The delay produced by the proposed circuits is decreases with the increase in number of tubes in CNTFET. It is found that the proposed circuits produce less delay when tube count of CNTET is 40. It is due to the fact that with the increase in CNT tube count increases the driving capacity hence delay decreases. Among the three proposed BCAMs IPFAL based BCAM produces less delay compared to IECRL and IPAL based BCAMs. The delay analysis of the proposed CNTFET - IECRL-CAM, CNTFET -IPAL-CAM, CNTFET -IPFAL-CAM for different number of tubes is shown in Fig.6.

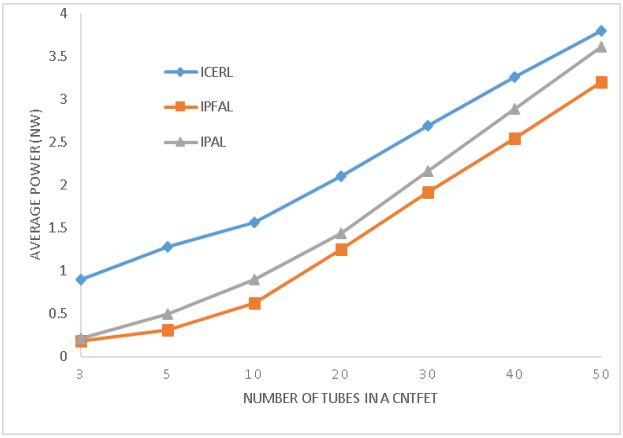

Fig.5: Average power versus tube count

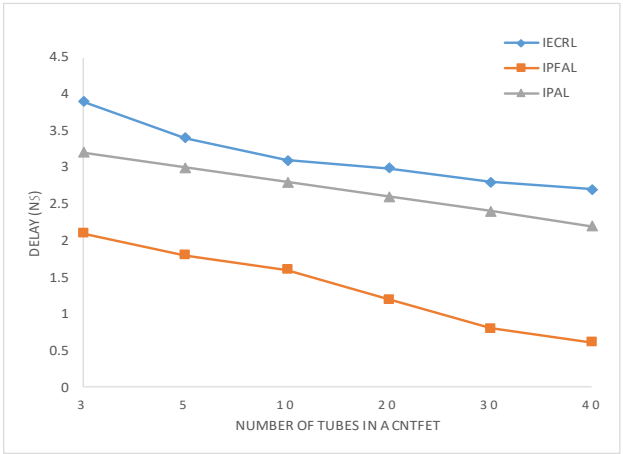

Fig.6: Delay versus tube count

B. Average power and delay variations with chirality vector

The average power variations of the proposed CNTFET - IECRL-CAM, CNTFET -IPAL-CAM, CNTFET -IPFAL-CAM for variations in the chirality vector is presented and is shown in Fig.7. It is clear from the figure that as the chirality vector value increases the power consumed by proposed circuits is increases. Among the three proposed BCAMs IPFAL based BCAM consumes less power compared to IECRL and IPAL based BCAMs. The delay analysis of the proposed CNTFET - IECRL-CAM, CNTFET -IPAL-CAM, CNTFET -IPFAL-CAM for different values of chirality vector is shown in Fig.8. The delay produced by the proposed circuits is decreases with the increase in chirality vector of CNTFET. It is found that the proposed circuits produce less delay when the chirality vector of CNTET is 20. Among the three proposed BCAMs IPFAL based BCAM produces less delay compared to IECRL and IPAL based BCAMs. As the chirality value increases the diameter of the CNTFET increases hence the average power increases and delay decreases.

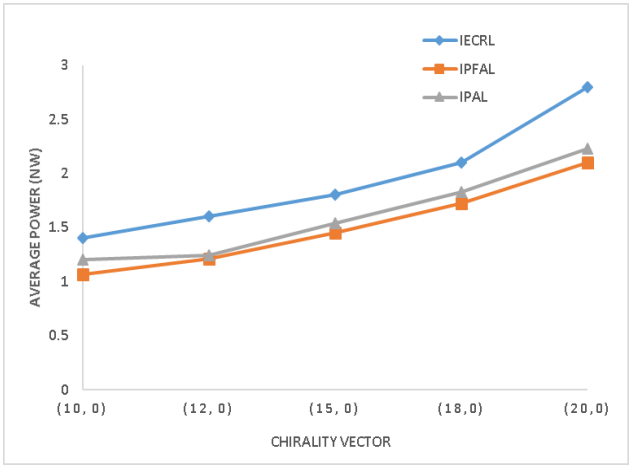

Fig.7: Average power versus chirality vector

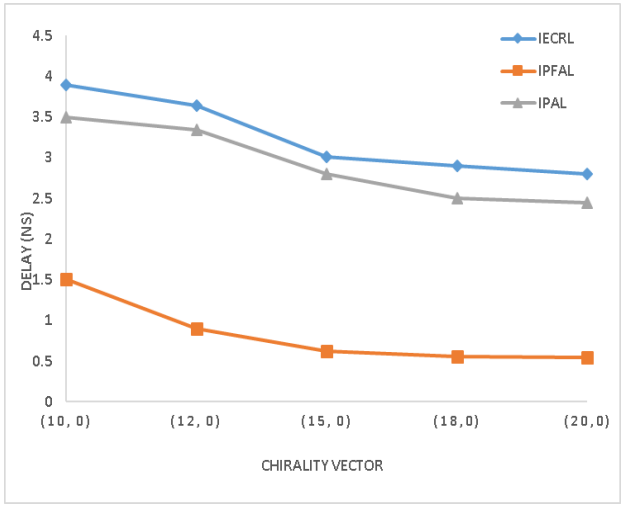

Fig.8: Delay versus Chirality Vector

C. Average power and delay variations with Pitch

The average power consumed by the proposed CNTFET - IECRL-CAM, CNTFET -IPAL-CAM, CNTFET -IPFAL-CAM for different values of pitch is shown in Fig 9. It is clear from the figure that as the pitch value increases the power consumed by the proposed circuits also increases. They consume less power when the pitch value is 5. Increase in pitch value the effective width of the channel reduces thereby degrading the device current. Hence, as the pitch value increases the average power decreases. Among the three proposed BCAMs IPFAL based BCAM consumes less power compared to IECRL and IPAL based BCAMs. The delay produced by CNTFET based IECRL, IPAL and IPFAL binary CAM cells for different values of pitch is presented and is shown in Fig.10. It is clear that as the pitch value increases the delay produced by the circuit is decreased. With increases inter tube spacing (pitch), the gate-to channel capacitance decreases and hence the delay is decreased. Among the three proposed BCAMs IPFAL based BCAM produces less delay compared to IECRL and IPAL based BCAMs.

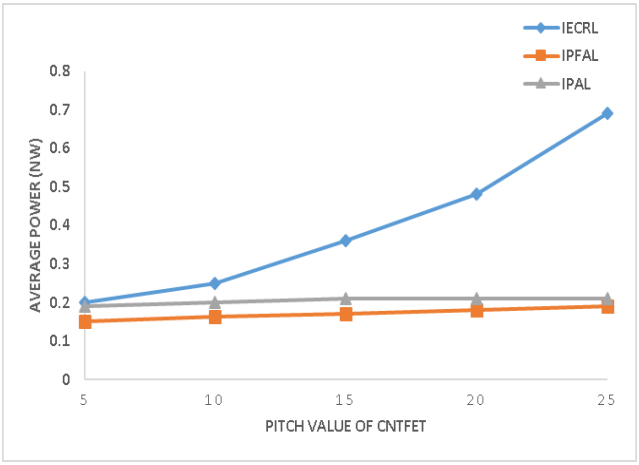

Fig.9: Average power versus Pitch Values

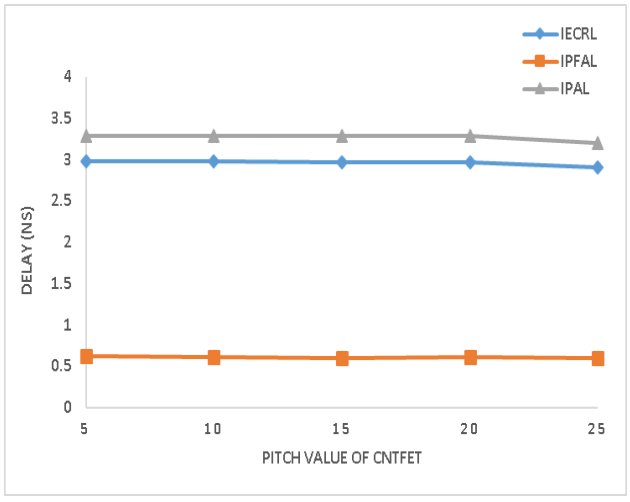

Fig.10: Delay versus Pitch Values

D. Average power and delay variations with Oxide thickness

The power consumed by the proposed CNTET based IECRL, IPAL, IPFAL CAM cells for different values of oxide thickness is presented and is shown in Fig.11. It is clear from the figure that as the oxide thickness value increases the power consumed by circuits is decreased. Among the three proposed BCAMs IPFAL based BCAM consumes less power compared to IECRL and IPAL based BCAMs. The delay produced by the proposed CNTFET based IECRL, IPAL and IPFAL binary CAM cells for different values of oxide is also presented and is shown in Fig.12. It is clear from the figure as the oxide thickness value increases the delay produced by the circuits increases. Among the three proposed BCAMs IPFAL based BCAM produces less delay compared to IECRL and IPAL based BCAMs.

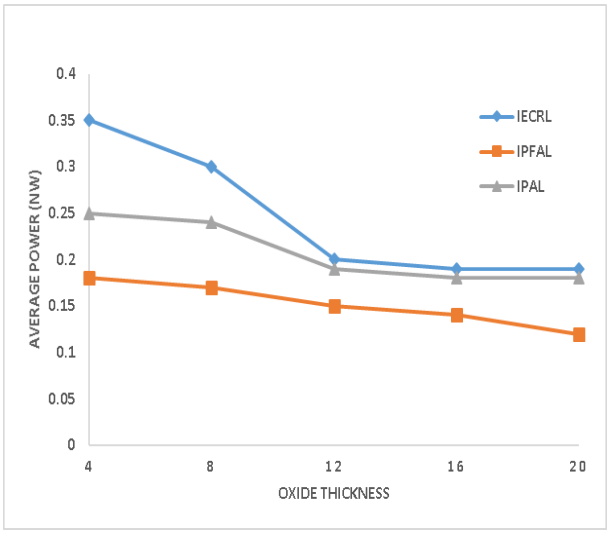

Fig.11: Average power versus Oxide thickness

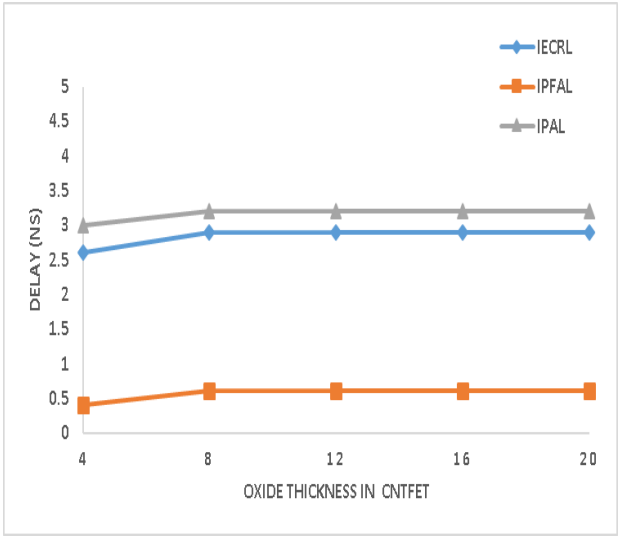

Fig.12: Delay versus Oxide thickness

E. Average power and delay variations with Dielectric material

The average power consumed by the proposed CNTFET based IECRL, IPAL and IPFAL BCAM cells for different dielectric material Si_3N_4, Al_2O_3, $HSiO_4$, TiO_2, ZrO_2 and is shown in Fig. 13. It is clear from the figure that they will consume less power when the material is silicon nitrate [$Si_3N_4(K_{ox} = 7)$]. Among the three proposed BCAMs IPFAL based BCAM consumes less power compared to IECRL and IPAL based BCAMs. The delay produced by proposed CNTET based IECRL, PAL, PFAL for different values of dielectric material is presented and is shown in Fig.14. It is clear from the figure that significant less delay is produced with the silicon nitrate [$Si_3N_4(K_{ox} = 7)$] as a dielectric medium. Among the three proposed BCAMs IPFAL based BCAM produces less delay compared to IECRL and IPAL based BCAMs.

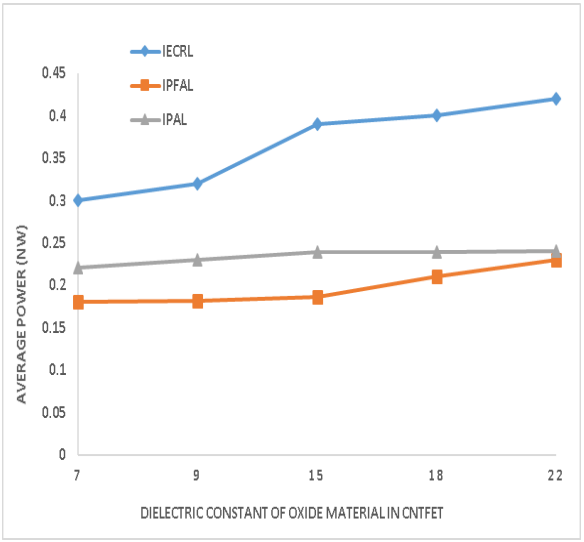

Fig.13: Average power versus Dielectric constant

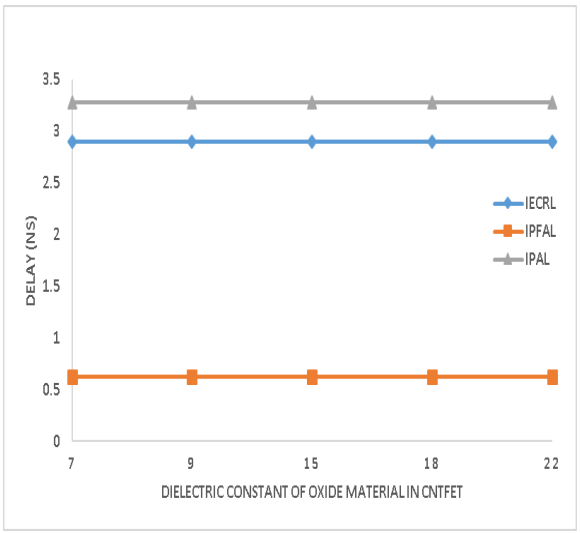

Fig.14: Delay versus Dielectric constant

F. Optimum Parameter set for CNTFET based BCAM Cells

From both the power analysis and delay analysis of the CNTFET based proposed IECRL, IFPAL and IPAL binary CAM circuits it is found that the CNTFET parameters yielding optimal delay and power consumption values. These optimum parameters are tabulated in Table I. With these CNTFET parameters the three proposed CAM cells are simulated and the results are compared to that of CMOS based binary CAM cells. It is found that significant performance improvement is achieved using CNTFETs. The values of power consumption and delay produced by the proposed circuits are tabulated in Table II and Table III respectively. The output waveforms of the three proposed BCAM cells are shown in Fig.13, Fig.14 and Fig.15.

Table I: CNTFET Optimized parameters for low power applications

S.No.	CNTFET Parameter	Value
1	Tube count	3
2	Chirality Vector	(10,0)
3	Pitch Value	5
4	Oxide Thickness	9
5	Oxide Material	$Si_3N_4(K_{ox} = 7)$

Table II: Power analysis of proposed binary CMOS and CNTFET based BCAM cells

S.No.	Type of the Binary CAM cell	Power consumed by the proposed binary CAM cells	
		CMOS Based Binary CAM cell (µW)	CNTFET based Binary CAM cell (nW)
1	IECRL	5.18	50
2	IPFAL	1.86	0.17
3	IPAL	1.85	12

Table III: Delay analysis of proposed binary CMOS and NTFET based BCAM cells

S.No.	Type of the Binary CAM cell	Delay analysis of the proposed binary CAM cells in (nS)		% Improvement of CNTFET over CMOS
		CMOS Based Binary CAM cell	CNTFET based Binary CAM cell	
1	IECRL	3.2	2.1	34.3
2	IPFAL	1.57	0.69	56.4
3	IPAL	4.8	3.3	31.2

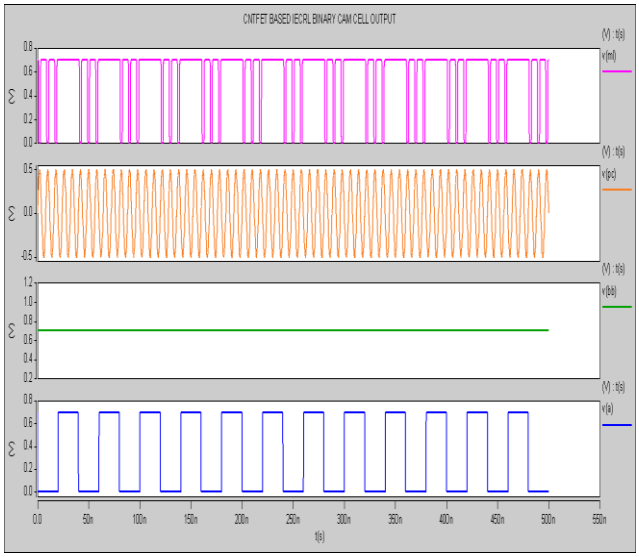

Fig.15 CNTFET based IECRL - BCAM Cell output

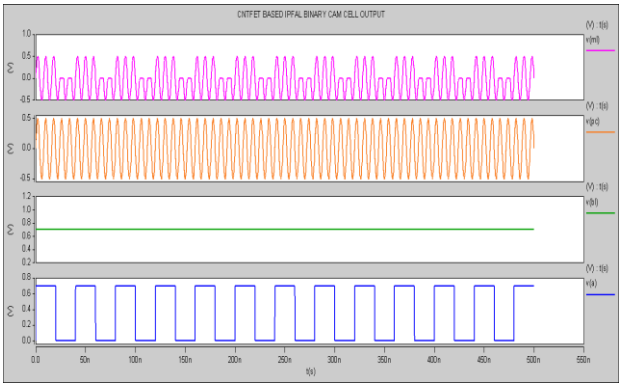

Fig.16 CNTFET based IFPAL - BCAM Cell output

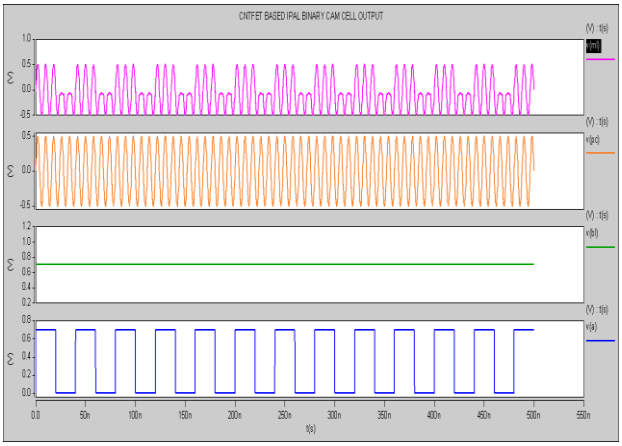

Fig.17. CNTFET based IPAL - BCAM Cell output

From the power analysis and delay analysis it is found that IPFAL- CNTFET based BCAM outperforms compared to IECRL and IPAL CNTFET based BCAM cells. The match line of BCAM follows power clock signal if search data is equal to stored data. The output of IPFAL based BCAM is shown in Fig.16.

V. CONCLUSIONS

In this paper, we proposed three CNTFET based BCAM cells. These are based on adiabatic/ charge recovery logic based BCAM cells. The integration of adiabatic/ charge recovery logic with CNTFET improved the circuit performance in terms of average power and delay. This work also found the optimum parameter set for CNTFET BCAM cells. The simulation results show an improvement in the average power and delay of proposed BCAM cells compared to CMOS-based BCAM cells. The average power of the proposed BCAM cells is in the order of nano watts while for CMOS based BCAM cells it is in the order of micro watts. The delay of the proposed BCAM cells is improved by up to 56.4% compared to CMOS based BCAM cells. It is also found that IPFAL- CNTFET based BCAM outperforms compared to IECRL and IPAL CNTFET based BCAM cells. All simulations are performed in HSPICE at 32 nm technology for both CMOS and CNTFET.

REFERENCES

1. K. Pagiamtzis, A. Sheikholeslami, "A low-power contentaddressable memory (CAM) using pipelined hierarchical search scheme", *IEEE Journal of Solid-State Circuits*, vol. 39, no. 9, pp. 1512-1519, 2004.
2. Kostas Pagiamtzis and Kostas Pagiamtzis, "Content-Addressable Memory (CAM) Circuits and Architectures: A Tutorial and Survey", IEEE Journal of Solid-State Circuits, Vol. 41, No. 3, pp. 712-727, March 2006.
3. C.Venkataiah et.al. "Analytical Study of Bundled MWCNT and Edged-MLGNR Interconnects: Impact on Propagation Delay and Area", IEEE Transactions on Nanotechnology, 2019. DOI 10.1109/TNANO.2019.2920679.
4. C.Venkataiah, K. Satyaprasad, T. Jayachandra Prasad, "FDTD algorithm to achieve absolute stability in performance analysis of SWCNT interconnects", Journal of computational electronics (Springer), 2018. DOI: 10.1007/s10825-017-1125-1.
5. C.Venkataiah, K. Satyaprasad, T. Jayachandra Prasad, "Insertion of optimal number of repeaters in pipelined nano interconnects for transient delay minimization", Circuit systems and signal processing (Springer), 2019. DOI: 10.1007/s00034-018-0876-7.
6. C.Venkataiah, K. Satyaprasad, T. Jayachandra Prasad, "Signal integrity analysis for coupled SWCNT interconnects using stable recursive algorithm", Microelectronics Journal (Elsevier), volume. 74, pp. 13-23, 2018.
7. C.Venkataiah, K. Satyaprasad, T. Jayachandra Prasad, "Crosstalk induced performance analysis of single walled carbon nanotube interconnects using stable finite difference time domain model", Journal of nanoelectronics and optoelectronics (American scientific publishers), Vol. 12, pp. 1-10, 2017.
8. C.V.S. Reddy, C.Venkataiah, V.R.Kumar, S.Maheswaram, N. Jains, S.D. Gupta and S.K. Manhas "Design and simulation of CNT based nano-transistor for greenhouse gas detection", Journal of nanoelectronics and optoelectronics, Vol. 12, pp. 1-9, 2017.
9. D. Jothi and R.Siva Kumar, "A completely efficient charge recovery adiabatic logic content addressable memory", International Conference on Computers, Communications, and Systems (ICCCS), 2-3 Nov. Kanyakumari, India, 2015.
10. A.Mishra, A.Jaiswal, A.Jaiswal, A.K.Niketa, "Design and analysis of conventional CMOS and energy efficient adiabatic logic for low-power VLSI application", International journal Eng. Adv. Technol. Vol.3, No.12, pp.295–299, 2014.
11. Chi-Chia Sun and Cheng-Chih Wang, "Adiabatic Logic Based Low-Power Precomputation Based Content Addressable Memory Parameter Extractor Design", Journal of Low Power Electronics, Vol.14, pp.439–447, 2018.
12. Pilin Junsangsri , Jie Han, Fabrizio Lombardi, "Design and Comparative Evaluation of a PCM-Based CAM (Content Addressable Memory) Cell, IEEE Transactions on Nanotechnology, Vol.16, No. 2, pp. 359 – 363, March 2017.
13. Mohammed Zackriya V and Harish M. Kittur, "Precharge-Free, Low-Power Content-Addressable Memory", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol.24, No.8, **pp.**2614 – 2621, Aug. 2016.

14. H. Jarollahi, V. Gripon, N. Onizawa, W. J. Gross, "Algorithm and architecture for a low-power content-addressable memory based on sparse clustered networks", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 4, pp. 642-653, Apr. 2015.
15. S. K. Maurya, L. T. Clark, "A dynamic longest prefix matching content addressable memory for IP routing", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, no. 6, pp. 963-972, Jun. 2011.
16. A. Bremler-Barr, D. Hendler, "Space-efficient TCAM-based classification using gray coding", *IEEE Transactions on Computing.*, vol. 61, no. 1, pp. 18-30, Jan. 2012.
17. S. I. Ali, M. S. Islam, "A match-line dynamic energy reduction technique for high-speed ternary CAM using dual feedback sense amplifier", *Microelectronics Journal*, vol. 45, no. 1, pp. 95-101, Jan. 2014.
18. A.-T. Do, S. Chen, Z.-H. Kong, K. S. Yeo, "A high speed low power CAM with a parity bit and power-gated ML sensing", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 21, no. 1, pp. 151-156, Jan. 2013.
19. C.-C. Wang, C.-H. Hsu, C.-C. Huang, J.-H. Wu, "A self-disabled sensing technique for content-addressable memories", *IEEE Transactions on Circuits Systems. II Exp. Briefs*, vol. 57, no. 1, pp. 31-35, Jan. 2010.
20. D. Jothi and R.Siva Kumar, “D. Jothi , R.Siva Kumar, “Design and Analysis of Power Efficient Binary Content Addressable Memory (PEBCAM) Core Cells”, Circuits, Systems and signal processing”Vol.37, No. 4, pp 1422–1451, April 2018.
21. M.Arulvani and M.Mohmed Ismail “Low power FinFET content addressable memory design for 5G communication networks”, Computers and Electrical Engineering, Vol.72, pp.606-613, November 2018.

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